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Dynamics of the Voltage Distribution Over Cascaded Diodes

Eden Tafa Tulu*(1), Jörn Hänel(2), Ulf Müter(2), Klaus Hoffmann(1), and Marcus Stiemer(1)
(1) Helmut Schmidt University / University of the Federal Armed Forces Hamburg, Holstenhofweg 85, 22043 Hamburg, Germany; e-mail: tulue@hsu-hh.de; m.stiemer@hsu-hh.de; klaus.hoffmann@hsu-hh.de
(2) Philips GmbH, Röntgenstr. 22, 22335 Hamburg, Germany; e-mail: joern.haenel@philips.com

Abstract

One state-of-the-art technology for high voltage (HV) generators consists of an LCC circuit with a symmetrical Cockcroft Walton (CW) voltage multiplier. A critical component of this design is a cascade of diodes connected in series that have to block a HV in reverse direction. It is a challenging task to obtain a sufficiently symmetric voltage drop over the diodes, which is influenced by parasitic capacitances, volatility of the reverse leakage currents, break through voltages, and recovery times from avalanching, as well as varying cooling conditions. An asymmetric voltage distribution can cause irreversible damage of individual diodes. Here, we present a detailed analysis of the dynamics of the voltage distribution over cascaded diodes and its technical implications. Hence, a model for the dynamic stress cascaded diodes are exposed to is presented in order to derive simulation methods that allow for an accurate prediction of the diodes' stress and, moreover, for designing frameworks for a stable long-term operation of cascaded diodes.

1 Introduction

A medical X-ray system requires a high frequency (HF), high voltage (HV) generator, which supplies regulated HV-DC power to the X-ray tube [1]. In addition to the demands of high power and small geometry or weight, i.e., maximization of the power volume ($\mathrm{kW/m^3}$) or the power-to-weight ratio ($\mathrm{kW/kg}$) power electronics for a medical X-ray tube also demands a high quality HV-DC feeding current, because noise in the power supply would reduce the image quality. Weight and volume minimization have for X-ray tubes for computer tomography a particular meaning, since the device moves at high speed in its usual operation. In addition, high energetic efficiency and reliability, a long service life and sufficient load cycle stability are vital for such devices. In such a situation, it is advantageous to combine the classical LCC resonant tank architecture with a multiplier such as, e.g., the CW multiplier. A downstream HV multiplier allows for downscaling the HV transformer in the usual LCC architecture (cf. [3]). This does not only lead to weight and volume reduction, but also reduces its turn ratio and voltage stresses as well as its winding capacitance and leakage inductance. Thus, employing a multiplier reduces the device's volume and weight and thus increases the movability of the device and may even help to make it portable and cost-effective compared to a high turn-ratio transformer. Fig. 1 shows a block diagram of a HF HV power circuit with a power supply, an inverter, HV transformer and a CW voltage multiplier. First, the rectifier con-

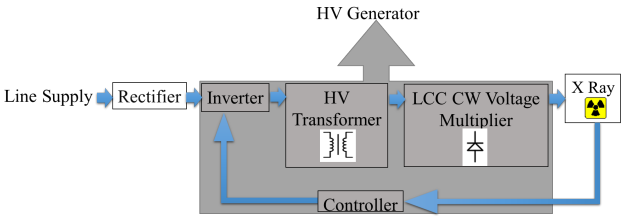

Figure 1. Block diagram of HF, HV X-ray generator.

verts an AC single or three phase input power into an intermediate DC source and feeds it to the HV generator. There, the inverter converts the DC input into the HF AC through fast power transistors. The HF AC current from the HV transformer is fed to the CW voltage multiplier. The HV generator delivers a rectified output voltage in the range 40 to 150 kV and a nominal current range from 10 to 1200 mA with output power range from 10 to 200 kW to the tube. In theory, the output voltage $V_\mathrm{o} = 2N_\mathrm{st}V_\mathrm{s}$, generated by CW voltage multiplier is proportional to the number of stages N_st at peak triggering voltage V_s. The close loop control circuit provides a fast response time and a stable output voltage. Nevertheless, non negligible parasitic capacitance occurred in the HV multiplier itself, which influences the circuit characteristics [2]. While the right capacitance on the secondary side is essential for a HV transformer to work efficiently as a resonant tank, it must not become too large. Moreover, spatially varying stray capacitances may influence the multiplier in an unfavorable way (see below).

A critical point in the operation of a HV multiplier comes from the fact that diodes have to block a current at an enormous voltage – e.g., up to 75 kV – for a certain period, which is much higher than one diode can block. Hence, a series connection of cascaded diodes is employed, dividing the reverse current born by the individual diodes. However, it is almost impossible to design a system with a completely symmetric voltage distribution over such a cascade, and a highly asymmetric distribution may cause one

or more diodes to fail: If a certain diode's break through voltage is reached it starts avalanching, which is at first a reversible process. However, it heats up during avalanching and if this process lasts too long and if the diode cannot be sufficiently cooled it will irreversibly be damaged. The result of an over-voltage test of a HV rectifier is exhibited in Fig. 2, where one diode has been destroyed due to an imbalanced reverse voltage distribution. During avalanching the diode's resistance is reduced, thus transferring the voltage stress to other diodes and giving the diode the opportunity to recover. Avalanching may affect several diodes one after the other – in the end the cascade may assume a steady state dividing the applied voltage.

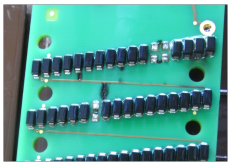

Figure 2. Damage of diodes in HV rectifier.

Several factors contribute to the voltage distribution over a cascade of diodes: Parasitic capacitances, different inverse leakage currents of the diodes, different break through voltages and recovery times from avalanching, and varying cooling conditions. Except of the parasitic capacities and the cooling strategy these quantities are given by the vendor of the diode, and hence only the first two parameters can be addressed through the design of the power supply.

In this work, an analysis of the dynamics of the voltage distribution over cascaded diodes and its technical implications are presented with the objective to provide a model for the dynamic stress cascaded diodes are exposed to in order to derive simulation methods that allow for an accurate prediction of the diodes' stress and, moreover, for designing frameworks for a stable long-term operation of cascaded diodes. After a review of the relevant physical relations in section 2, a typical HV diode is characterized (section 3), and preliminary simulation results obtained from section of the sought comprehensive model of the dynamical behavior cascaded diodes and multipliers are presented in section 4, before some conclusions are derived (section 5).

2 Reverse Voltage over Cascaded Diodes

Relevant effects for the diodes' dynamics are their forward and backward operation including the reverse current as described by Shockley's equation, the RC-time constants modeling the interaction with their environment, the break through voltage marking the transition to avalanching, the voltage-current characteristics during avalanching, the recovery times from avalanching, when the voltage stress has been removed, the temperature dependence of the above features, and boundary conditions resulting from the applied cooling. We start the discussion by describing the steady state: Using diodes as voltage dividers exploits largely their imperfection: If all diodes were perfect, the whole input voltage would drop over first one setting all other voltages to ground level. Just looking at the simplified cascade on the right hand side of Fig. 3, and setting the parasitic capacitance to 0, voltage division of the exemplary applied DC-voltage V_s yields

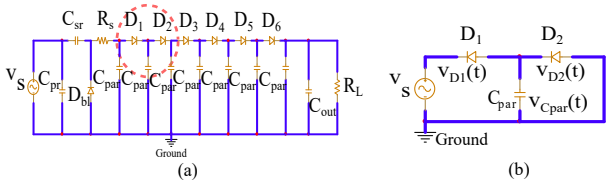

Figure 3. (a) Simplified circuit model of cascaded diodes; (b) Reduced model (two diodes with parasitic capacitance).

$$V_s = v_{D1} + v_{D2} \quad \text{and} \quad I_{D1} = I_{D2}, \tag{1}$$

where v_{D1}, v_{D2}, I_{D1}, and I_{D2} are the voltage and current at the two diodes, respectively. According to the Shockley diode equation, the diode current I_D can be expressed as

$$I_D = I_s \left(e^{\frac{v_D}{nV_T}} - 1 \right), \tag{2}$$

where v_D is voltage across diode, I_s the reverse saturation current, n the ideality coefficient, and V_T the thermal voltage in Volt. A possible transition to avalanching is not considered here. Combining Eq. 2 and Eq. 1 and assuming, $\kappa = \frac{1}{nV_T}$, $X = e^{\kappa v_{D1}}$, $Y = e^{\kappa v_{D2}}$, and $q = e^{\kappa v_s}$, equations in 1 can be solved for x and y:

$$\left.\begin{matrix} X \\ Y \end{matrix}\right\} = \left\{ \begin{matrix} \frac{1}{(2I_{s1})} \left((I_{s1} - I_{s2}) + \sqrt{(I_{s2} - I_{s1})^2 + 4qI_{s1}I_{s2}} \right) \\ \frac{1}{(2I_{s2})} \left((I_{s2} - I_{s1}) + \sqrt{(I_{s2} - I_{s1})^2 + 4qI_{s1}I_{s2}} \right) \end{matrix} \right. \tag{3}$$

Once the value X and Y are obtained, the voltage at the diodes can be computed as

$$v_{D1} = \frac{1}{\kappa} \log(X) \qquad \text{and} \qquad v_{D2} = \frac{1}{\kappa} \log(Y) \tag{4}$$

This implies that not even the steady state is symmetric, as the inverse leakage current is a volatile quantity: Fig. 4 provides measurement data of the reverse leakage current for 60 diodes. The observed variation implies a corresponding variation of the steady state voltage dropping over different diodes in the cascade. The diodes with the lowest leakage current will be mostly stressed.

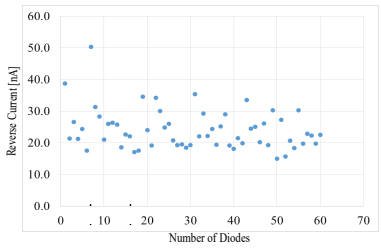

Figure 4. Variation of reverse leakage current over diodes.

Next, we consider the transient behavior of cascaded diodes, again studying the simple cascade in Fig. 3b triggered by a constant DC voltage, but now with a non-zero capacitance. To concentrate on the nature of the transient process, we simplify the system by setting the diodes' resistance to a constant value. To gain more accuracy, the Shockley equation could be employed and the resulting non-liner differential equation could be solved numerically. At time $t = 0$, when the capacitor is discharged, the voltages across the diodes and capacitor can be written as $v_{\mathrm{D}_1}(0) = V_\mathrm{s}$, $v_{D_2}(0) = 0$ and $v_{C_\mathrm{par}}(0) = 0$. At $t = \infty$, according to Kirchhoff's law, the voltages and the current in the circuit shown in Fig. 3b can be expressed as

$$\frac{\mathrm{d}v_{\mathrm{D}_1}}{\mathrm{d}t} + \frac{I_{C_\mathrm{par}}}{C_\mathrm{par}} = 0\,, \quad \frac{\mathrm{d}v_{\mathrm{D}_2}}{\mathrm{d}t} = \frac{I_{C_\mathrm{par}}}{C_\mathrm{par}}\,, \tag{5}$$

$$\frac{v_{\mathrm{D}_1}}{R_{D_1}} = \frac{v_{\mathrm{D}_2}}{R_{\mathrm{D}_2}} + I_{C_\mathrm{par}}\,. \tag{6}$$

Solving this equation yields the voltages across D_2 and D_1:

$$\left.\begin{matrix} v_{\mathrm{D}_2}(t) \\ v_{\mathrm{D}_1}(t) \end{matrix}\right\} = \left\{\begin{matrix} v_{D_2}(\infty)\left(1 - e^{t/\tau}\right) \\ V_\mathrm{s} - v_{D_2}(\infty)\left(1 - e^{t/\tau}\right) \end{matrix}\right. \tag{7}$$

with time constant $\tau = C_\mathrm{par}\dfrac{R_{\mathrm{D}_1}R_{\mathrm{D}_2}}{R_{\mathrm{D}_1} + R_{\mathrm{D}_2}}$, that determines how long D_1 is extra stressed. If τ is large, diode D_1 avalanches and D_2 is stressed due to the reduced resistance of D_1. If avalanching endures, the diode could break. This shows the importance of the parasitic capacitance.

The next effect to be considered is the switching time of the diodes: If a diode switches fast during the transition from forward to reverse current, the fastest diodes is more stressed as the slower one. For the other relevant effects such as the avalanching behavior measured values and phenomenological relations have to be considered (see below).

3 Diode Modeling

Due to their desirable properties and reasonable cost, commercial HV PIN-diodes, such as, e.g., produced by Fagor or Vishay, with a blocking voltage around 1 kV are dedicated for HV multipliers. To investigate the influence of the parasitic capacitance in a multiplier, we exemplary model the Vishay diode. To obtain the I-V characteristics and observe its reverse breakdown, a time domain analysis is performed. The maximum allowable reverse operating voltage per diode is supplied across the diode's terminals and the current that flows through the diode is computed. Fig. 5 shows the current across the Vishay diode in time domain. When the circuit is connected to the input source in the first positive half cycle, the diode starts conducting. In case of reverse bias, the diode blocks until it starts avalanching at 30 μs, and the reverse current flows across the diode in the negative half cycle.

Moreover, the approximative I-V characteristics of the Vishay BGY23M diode is illustrated in Fig. 6. The forward

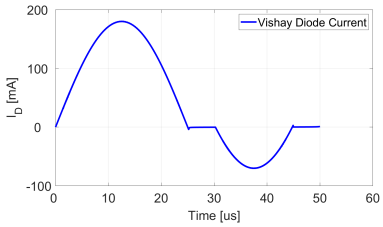

Figure 5. Time domain analysis

bias and the reverse-bias properties including the avalanche behavior of the diode are presented. To determine the I-V curve, the resulting voltage across the diodes is computed after applying the input source. In forward bias, as the voltage drops across the Vishay diode, the current flowing through the diode starts to rise. When it rises above the threshold voltage of 1.7 V the current flow through the diode rises up to some rated current value. In the reverse bias condition, when negative voltages are applied to the diode, the reverse current saturates on some close-to-zero constant. As the reverse bias voltage rises, a breakdown occurrs when the voltage gets higher than 1100 kV, and the reverse leakage current flows across the diode. This avalanche breakdown is mostly reversible before the diode overheats and thermal damages. Diodes may have various reverse recovery times when they switch from forward to reverse bias. An excessive reverse voltage applies across the fastest diodes that might destroy them. Therefore, the rise-time $\mathrm{d}v/\mathrm{d}t$ of the reverse voltage need to be controlled. Basically, the reverse saturation current is strongly dependent on temperature. As the product of the voltage and current is related to the generated heat, temperature rise imposes a limit.

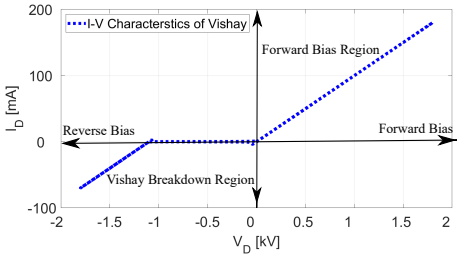

Figure 6. I-V characteristics of the Vishay diode.

4 Simulation Results

Voltage stress on diodes in case of two diodes placed in series with various reverse current has been numerically studied. Similar to the above analytic expressions, we modeled two Vishay diodes with various reverse current placed in series, and supply the input source with 2 kV. All other parameters of the Vishay diode remain constant while the I_s varies. As predicted, the plot in Fig. 7 shows that the highest voltage stress is on the diode with the lower leakage current (in red). The peak voltage across the diode with lower I_s is 0.85 kV and of the other is 0.3 kV.

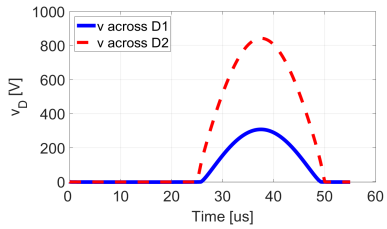

Figure 7. Influence of reverse current over Vishay diodes.

To analyze the voltage dynamics in the multiplier module, a simplified circuit of the multiplier has been modeled as shown in Fig. 3a. The model is built with six Vishay diodes, connected in series along other circuit elements. To compute the voltage across each diode, the AC source of 6 kV is supplied. Most of the system parameters are adapted from the measurements.

In case of symmetry, the parasitic elements are excluded and all other parameters of the diodes are kept constant. Furthermore, the reverse saturation current is assumed identical for all diodes. As shown in Fig. 8 the voltage across the diodes is distributed symmetrically. At the load, the output voltage of 6 kV with the rise time of 0.23 μs is computed.

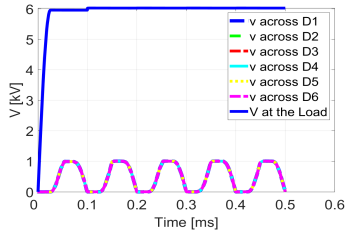

Figure 8. Symmetrical voltage over cascaded diodes.

Fig. 9 shows results for an asymmetric voltage distribution due to the parasitic capacitance over several cascaded diodes. The voltage stress on the first diode is very high compared to the remaining diodes. The voltage across the last four diodes is around 30 V while across the first and the second diodes 900 V and 170 V.

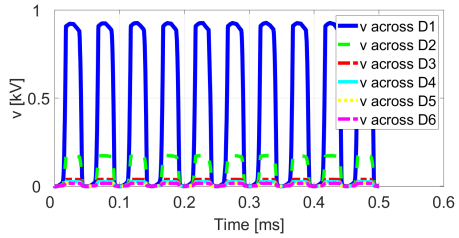

Figure 9. Assymetric voltage over cascaded diodes.

5 Electromagnetic field model

The role of the parasitic capacitances in the HV tank will be determined over numerical field simulation (see, e.g., [2]). The computational model includes junction capacitances as well as structural related capacitances, such as component package, layout and the module construction. The ladder of series connected diodes and capacitors in multiplier demands a large area of packages and connecting conductors. Therefore, the parasitic capacitance caused by the structure become crucial. These capacitances can be extracted using an electrostatic field problem. Thus, to capture the parasitic capacitance associated with the spatial structure of the module a 3D finite element (FE) field simulation will be performed. The mutual capacitances between different parts of the 3D computational domain are then transferred into an extended schematics of the multiplier to be able to consider its influence on the diodes' dynamics.

6 Summary

Over-voltage tests of HF rectifiers repeatedly lead to the damage of individual series-connected diodes in a cascade. The corresponding thermal stress results from a too long avalanche breakdown which itself is a consequence of an asymmetric voltage distribution over the cascade. The evolution of the voltage distribution depends on several transient phenomena including the *RC* time constant resulting from various ambient parasitic capacitances charged via the non linear resistances of the diodes, inverse leakage currents, break down voltages and transition times for avalanching and reverse recovery. The here presented approach to model to these phenomena gives rise to a framework for accurate simulation of the voltage multiplier in its environment. For the time being we present simulation results for subsystems that give insight in the relevant phenomena, such as the role of the capacitance on the voltage distribution across the diodes.

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