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# FFT and Beamforming Development for BURSTT

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We are developing digital backend for a project called "Bustling Universe Radio Survey Telescope for Taiwan" (BURSTT) in Taiwan[1]. A 16 channels input digitizer unit has been tested and implemented. We employed a Xilinx's RFSoC FPGA board, ZCU216[2], as the hardware platform, and using the firmware library developed by CASPER collaboration. The unit can accommodate 16 channel ADC inputs, sampling date rate at 1600MHz, bandwidth is 800MHz. 16 inputs of signals are processed independently with poly-phase filter bank (PFB) then fast Fourier transfer (FFT). After frequency domain data existed, we combined all 16 channels data then sent to the computer server by one one-hundred giga bit(100Gbps) Ethernet for the cross correlation and beam forming calculation.

Fast Radio Bursts (FRBs), bright millisecond-duration radio transients are happening thousands of times per day. FRBs' astrophysical mechanisms are still puzzling. BURSTT is optimized to discover and localize a large sample of bright and nearby FRBs. BURSTT will have a large field-of-view (FoV) of ~104 deg2 for monitoring the whole visible sky all the time, a 400 MHz effective bandwidth between 400-800 MHz, and the sub-arcsecond localization capability with several outrigger stations hundreds to thousands of km away. Initially, BURSTT will equip with 256 antennas at first phase, which we will test different designs and improve the system performance. Through the scalable features, BURSTT could equip with more antennas and eventually optimized designs. We expect that BURSTT initially would detect and localize ~100 bright (≥100 Jy ms) and nearby FRBs per year to sub-arcsecond precision.

Variety of in laboratory tests has been carried out, such 100G data rate transmission, finding optimal input power, multiple boards synchronization by 1 pulse per second (PPS) and 10MHz.

We will add beamforming in the FPGA platform before quantitation, the block diagram is as the Fig. 1 depicted. Since there are 16 inputs in one FPGA platform, we will beamform the 16 inputs as 16 beams aiming at 16 different directions. The beamforming needs store parameters in the block memory (BRAM) in the FPGA, the proposed method will be 256 units of the BRAM block, that might lead to overwhelm the FPGA resource. We are thinking the sampling the data from 400 to 800MHz only by taking advantage of the digital down converter (DDC) function provided by the radio frequency system on chip (RFSOC) chip. The simulation showed that it can save 20% of the BRAM.

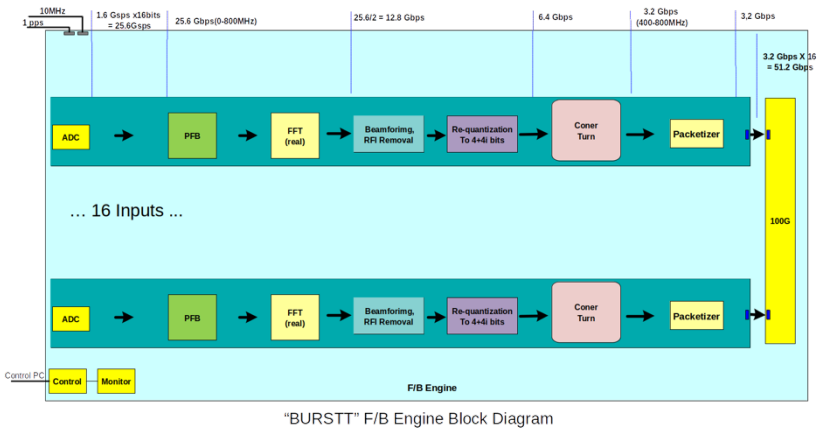


Figure 1. Block diagram of BURSTT's F engine, Sampling rate is 1600MHz, 800MHz bandwidth. At the end, 0-400MHz data will be discarded that reduces the data rate to 51.2 G bit/s.

## References

[1] “BURSTT:Bustling Universe Radio Survey Telescope in Taiwan”. Hsiu-Hsien Lin et al 2022 PASP 134 094106

[2] www.xilinx.com