Fast Index of Eye Diagram for Multiple Lines in DDR under Weak Coupling

Kai Li(1), Ruey-Beei Wu (1)
(1) National Taiwan University, Taipei, Taiwan; e-mail: r10942017@ntu.edu.tw; rbwu@ntu.edu.tw

When designing the PCB, the quality of the signal after passing through the channel is confirmed by the eye diagram. In practical cases that there are many channels, it is very time consuming to use pseudorandom binary sequence (PRBS) to simulate the eye diagram. The ISI of FEXT and NEXT caused by different channels on the main signal needs a specific bit pattern to generate the worst eye diagram. If we use PRBS, it is very difficult to get the worst bit pattern of different lines at the same time. Take N coupled transmission lines as an example. In the length of PRBS for a single line is 2^18-1, then we have to consider 2^(18*N) combinations to find the worst bit pattern, which is quite inefficient. Therefore, in the case of many channels, it is highly desired to extend peak distortion analysis (PDA)[1][2] by single bit response to get the worst bit pattern for multiple lines.

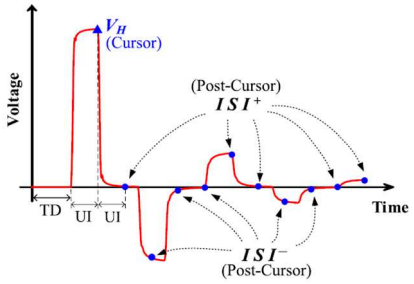

Figure 1. Single bit response with mismatched boundary & ISI.

Figure 2 shows the Single bit response of the transmission line, we can define V_H as the main cursor, then define a post cursor every unit interval (UI). The post cursor can be divided into two types, respectively ISI^+ and ISI^-, and the coupling caused by other channels is also considered, then the index for the worst eye height can be listed:

$$\text{Index} = \text{Main cursor} - \sum|\text{Post coursor}| - \sum\sum\left|\text{xtk coursor}^j\right| \quad (1)$$

In this paper, the transfer function for multiple coupled transmission lines with mismatched boundary conditions is derived, and the transfer function of the crosstalk term is also derived by decoupling the crosstalk aggressor and the victim under the assumption of weak coupling. Since the transfer function has been derived, a single bit response can be obtained easily by inverse Fourier transform, and the eye height and eye width can be obtained very quickly, saving time in the simulation and achieving high accuracy for the design of high speed DDR modules.

References

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[2] B. K. Casper, M. Haycock and R. Mooney, "An accurate and efficient analysis method for multi-Gb/s chip-to-chip signaling schemes," 2002 Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No.02CH37302), Honolulu, HI, USA, 2002, pp. 54-57, doi: 10.1109/VLSIC.2002.1015043.

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