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Design and implementation of tunable RF modules for reconfigurable metastructures that perform mathematical computations

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Abstract

In this work we report the design process of tunable RF modules and their implementation towards specialized network architectures that are able to perform mathematical operations such as matrix inversion.

1 Introduction

Analog computations using electromagnetic waves is a topic of emerging interest in the field of hardware-enhanced computations [1]. In particular, wave-based metamaterial devices offer a new class of devices that enable ultrafast, low consumption, distributed computing for application specific tasks, especially for solving mathematical equations [2, 3]. In this presentation we report the idea of a device that is able to perform mathematical computations, such as matrix inversion, in a tunable manner. The architecture of such device can be implemented either via well-known Mach–Zehnder interferometer-based (MZI) approaches, such as the "Miller" architecture [4, 5], or via an "alternative" architecture that we introduced [6, 7], as a generalization of a beamsteering/beamforming network.

Both reconfigurable networks can be implemented using the MZI module as their constituent component. MZI is a composite device that consists of two 3dB couplers and two waveguiding branches with phase tuning capabilities. The introduction of an amplifier stage at the output of the phase shifting branches enable a larger tunability over the input signal. Such a device consisting of a phase shifting stages followed by an amplification stage can be seen as a multiplier, a device that for a given arbitrary (in phase/amplitude) input creates a desired output. As part of the implementation process for the aforementioned architectures we discuss the design process of this basic module, followed by experimental implementation and measurements. Finally, we demonstrate the implementation of a simple 2×2 matrix utilizing the alternative architecture.

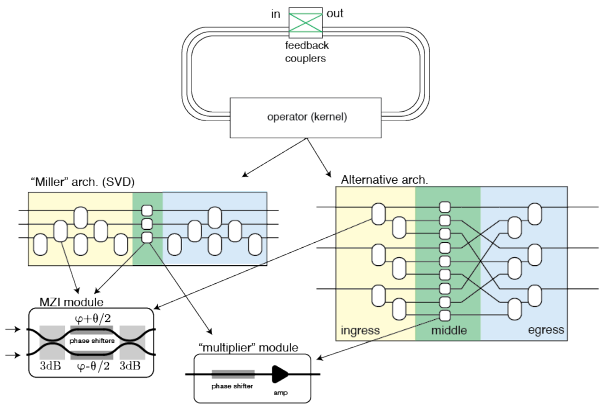

Figure 1. The ability to invert a given matrix requires an operator (kernel) stage connected with a feedback loop via a set of directional couplers. The operator can be implemented either via the "Miller" architecture or our "Alternative" architecture. The Miller architecture requires the singular value decomposition of the operator and can be implemented as a collection of MZIs. Our alternative architecture can be implemented utilizing the multiplier modules. Note that an MZI can be perceived as a combination of two multiplier units connected with two 3dB couplers and with no amplification. Therefore, the key component for the implementation of these architecture is the multiplier module.

2 Network Architectures

As has been recently demonstrated [2], a metastructure can exhibit equation solving (matrix inversion) capabilities assuming that we can properly engineer a matrix operator (kernel), and create a properly designed feedback path. The operator can in general be expressed as an $N \times N$ matrix. Figure (1) depicts the conceptual schematic of such device. From a mathematical standpoint such feedback essentially implements the Jacobi method for matrix inversion [8]. Although the presented inverse-designed metadevice can indeed perform a given matrix inversion, its reconfigurablity is significantly limited. For this reason we explore the possibility of materializing the main operator using a tunable and reconfigurable device.

Inspired by the photonic domain, one can find plenty examples of tunable architectures using MZI modules. Miller introduced such architecture with self-configuring capabilities [4, 9]. Assuming a matrix operator, this particular architecture (Fig. (1)) requires the singular value decomposition of the operator, i.e., an a priori mathematical decomposition of the required matrix. Mathematically, this decomposition can be equally computationally intensive as finding the inverse of the same matrix, therefore a question occurs: can we implement a given matrix operator without the need of any a priori calculations?

As a possible answer to the aforementioned question, here we discuss the details of an "alternative" architecture that enables this possibility. Such architecture can be seen in Fig. (1), and consists of three stages: the ingress, the middle, and the egress stage. Both the ingress and egress stage require the power split into N channels. This can be achieved either by a cascade of MZIs, or specially designed couplers. Once this stage is implemented, each of the N^2 outputs/inputs of the ingress/egress stage is connected via one dedicated multiplier module. As mentioned above, this module can give a desired complex output for a given arbitrary complex input. While this architecture could be potentially be built with MZIs, the ingress and egress stages introduce a total power factor $1/N$ to the propagating signals. For this reason one need to implement an extra amplification stage that will give the required amplitude to the output signal. For these purposes the middle stage of the alternative architecture can be implemented by a component that allows both the phase and amplitude control of the input signal. This multiplier module is essentially a collection of a phase shifting and an amplification module. Interestingly, an MZI can be considered as a device that consists of two 3dB couplers and two multipliers (assuming only their phase shifting capabilities).

3 Design and Implementation of the Multiplier RF Module

It is clear that the multiplier can be the main constituent for both architectures. Therefore, the precise performance of any matrix operation or matrix inversion relies heavily on the successful design and implementation of this module. Here, we describe the basic steps towards the design, implementation and characterization of such a device.

The multiplier module consists of a phase shifting stage and an amplification stage (Fig. (2)). The main operating frequency for this device is dictated by the availability of the phase shifting module. For this design we choose the JSPHS-51+ Phase Shifter (PS) module, a commercially available PS RF module that utilizes lumped element technology with central operating frequency at 45MHz. This PS is voltage controlled, offering 180+ degrees of phase shift at the 0-12V range. Therefore, the multiplier is designed to include two PS modules for covering a full 360-degree phase shift. The modeling of this device was done in AWR Microwave Office® using a realistic measured S parameter touchstone file provided by the manufacturer. Note that the PS stage introduces a total of up to 4dB losses to the input signal depending on the chosen phase offset.

After the PS stage, the propagating signal is fed into the amplification stage (Amp) (Fig. (2)). This stage is designed based on the commercially available AD603 variable gain RF amplifying module. This RF amplifier is able to give almost 45dB of dynamic voltage range for input voltages at the $[-0.5, 0.5]$V range.

Both the PS and the Amp module input voltages are generated by control circuitry which creates a common $[0, 5]$V input interface for both. The inputs are controlled by two external pins so that they can be set using one of two secondary piggy-backed board. In one design, this secondary board consists of potentiometers for manual operation and in the other, it consists of a networked Micro Controller Unit (MCU) with two 10bit outputs for automated reconfigurability. The networked MCUs can be controlled and programmed through a custom-build Python interface on a central computer.

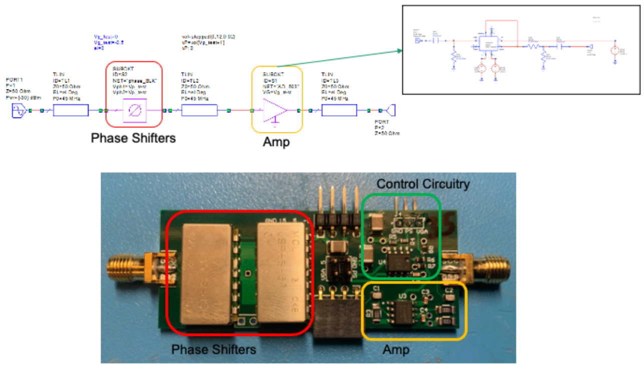

Figure 2. The multiplier module design (top schematics) and implementation (bottom photo). The basic stages are visible, i.e., the phase shifting (PS) and amplification (Amp) stage, and the control circuitry. For a given arbitrary complex input this device offers a 360 degree phase shift and 45dB voltage gain range.

4 Discussion

After describing the design and implementation process for the basic multiplier module, we proceed to the measurement and the characterization of the module and, as an example, the implementation of a simple 2×2 operator (kernel) using our alternative architecture. In Fig. 3 (subfigures (a),(b), and (c)) we can observe the output signal (voltage) behavior of the multiplier module at the range 40-50MHz, for three different voltages, i.e., (a) $V_{PS} = 0$ and $V_{Amp} = -0.5$, (b) $V_{PS} = 6$ and $V_{Amp} = 0$, and (c) $V_{PS} = 12$ and $V_{Amp} = +0.5$. These results are compared with a realistic system simulation with AWR Microwave Office ® simulator. The comparison between the simulated (blue line) and measured results (orange line) indicates that there is a good agreement between the designed and measured system. Small discrepancies are introduced mainly due to component tolerances and deviations. As an example, the PS module has $5-10\%$ variation over its designed values. This issue can be possibly solved through the characterization of each of the module, or through the development of more accurate models that will take into consideration the small component deviations. Since the control over the voltages of the PS and Amp modules is automated, a proper calibration scheme is implemented for addressing small discrepancies between the ideal and measured performance. Key observation of the above results is that we can

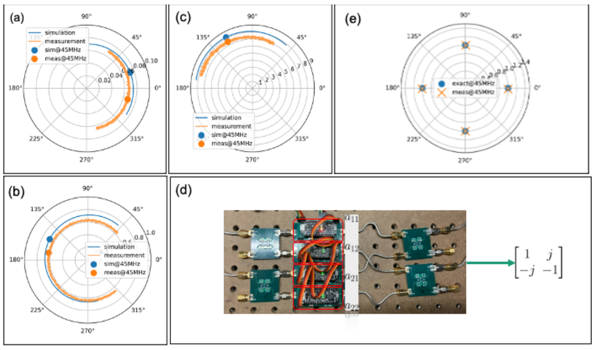

Figure 3. Voltage measurements of the multiplier unit at the $40-50$MHz range for three different test cases: (a) $V_{PS}=0$ and $V_{Amp}=-0.5$, (b) $V_{PS}=6$ and $V_{Amp}=0$, and (c) $V_{PS}=12$ and $V_{Amp}=+0.5$. A simple 2×2 matrix operator is implemented (d) and the results (e) demonstrate excellent agreement with the exact matrix.

indeed verify that the multiplier module can have a 360+ phase shifting range, while providing $45dB$ dynamic voltage range for the required signals, allowing us with a large parametric space for the programability and reconfigurability of the main operator. Again, either of the matrix inverting architectures can be built as a collection of multiplier modules. Therefore, for the development of our main idea it is important to experimentally verify the performance of this RF device.

Finally, as a step towards the realization of the aforementioned architectures, Fig. (3) depicts the implementation (Fig. 3 (d)) and measurement (Fig. 3 (e)) of a simple $2x2$ matrix using our alternative architecture. The ingress and egress stages are implemented with simple 3dB couplers, while the test operator was chosen to be

$$A=\begin{bmatrix} 1 & j \\ -j & -1 \end{bmatrix} \tag{1}$$

Note that agreement between the measured and the exact operator is remarkable. For this, each multiplier unit is calibrated accordingly, giving the desired value despite the small deviations that are observed in the above characterization results.

The above measurements pave the way towards the experimental implementation of any required kernel for the performance of mathematical operator (off-loop operation) and the performance of matrix inversions (on-loop operation), in a compact and tunable manner. Undoubtedly, this device will most likely be used for purposes beyond solving mathematical equations, such as general beamsteering, computational imaging and other antenna/RF hardware-enhanced concepts.

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