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Worst-Case Coupled Voltage Analysis of Printed Circuit Board Traces

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Abstract

A detailed worst-case coupled voltage study on various printed circuit board (PCB) trace shapes has been carried out. Different trace lengths and trace shapes have been considered to explore the response from worst-case coupled voltage under external electromagnetic field. As a first step, the coupled voltage to loads of a straight PCB trace is analytically calculated and compared with existing full-wave electromagnetic (EM) solver over a particular frequency spectrum. The worst-case coupled voltage, which is derived using the Parseval's theorem averages out the frequency dependent coupled voltage for a certain trace length. The final comparative results indicate that a specific PCB trace shape couples less to EM field irrespective of its length.

1 Introduction

External electromagnetic (EM) field coupling analysis to printed circuit board (PCB) traces is vast and complex. The copper traces are one of the important blocks in the design of an efficient PCB. These traces often suffer from spurious signals and external fields that could jeopardize the intended performance. It is evident that crosstalk issues gets highest priority in such densely packed boards, however, the external EM field coupling to these traces cannot be neglected due to increase in unintentional coupling through different radio frequency spectrum radiators. Therefore, the focus of this paper is to report some findings on the EM field coupling to loads, in the form of worst-case coupled voltage as the shape of the PCB trace changes.

The worst-case radiation emissions is a well-known concept and has been applied to various problems. This phenomena was recently applied for cables above ground [1]. The importance of worst-case envelope of differential pair cable harness located above metal plate was also understood through circuit simulations [2]. Furthermore, the radiated power from a differential pair trace has been analyzed using characteristic mode theory [3]. In addition, quadrangle tabs have been introduced in the differential pairs to reduce the near end and far end crosstalk [4]. Asymptotic equations were developed and reported to accommodate impedance discontinuities in the form of trace shape [5]. However, this paper reports some

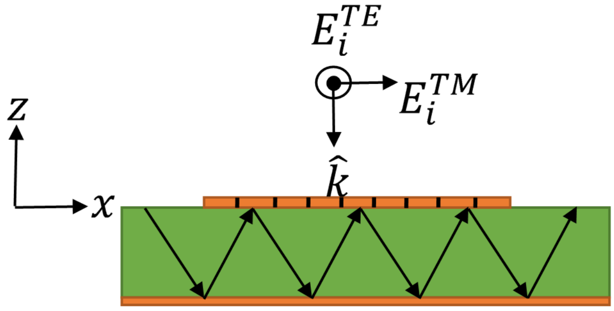


Figure 1. A conductive trace (top orange) located above dielectric (green) backed by ground plane (bottom orange).

interesting results related to non-straight PCB traces, which presents some new insights to future design layout rules.

2 Worst-Case Coupled Voltage

A straight PCB trace is considered as reference point whose analytical equations were derived in [6]. Fig. 1 shows the front view and typical configuration of a PCB trace. The arrows inside dielectric in Fig. 1 represent the transmitted and reflected fields caused by external EM field. The analytical formulas were developed considering the substrate and ground plane infinite in size compared to trace. The coupled voltage to the loads is given as [6]:

$$V_{0,L}(f) \cong \mp E_i \frac{e^{j\beta(x_{2,1}-L)}}{2} \frac{e^{j(\mp\beta-k_x)L}-1}{j(\mp\beta-k_x)} \left(f_x(\theta,\phi,\gamma) - j(\mp\beta-k_x) f_z(\theta,\phi) \frac{1-e^{-jk_{2z}h}}{jk_{2z}} \right) \quad (1)$$

The above expression was developed using the Baum-Liu-Tesche (BLT) formulation accounting for both horizontal electric field on the substrate surface and the vertical electric field in the substrate layer. Once the coupled voltage is calculated from (1), the worst-case coupled voltage is given as:

$$V_{LP} = \sqrt{2Z_0 W \int_{f_1}^{f_2} |L_w(f)|^2 df} \quad (2)$$

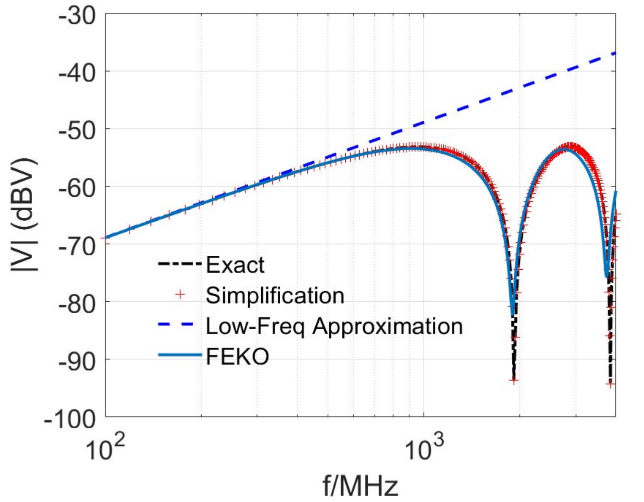


Figure 2. Coupled voltage (in dBV) to load of a straight trace with change in operating frequency. Other input parameters are : trace length (L) = 85.6 mm, trace width (W_s) = 3. 81752 mm, dielectric thickness (h) = 2 mm, ϵ_r = 4.4, tan δ = 0.02, $\theta = \phi = \gamma = 0°$.

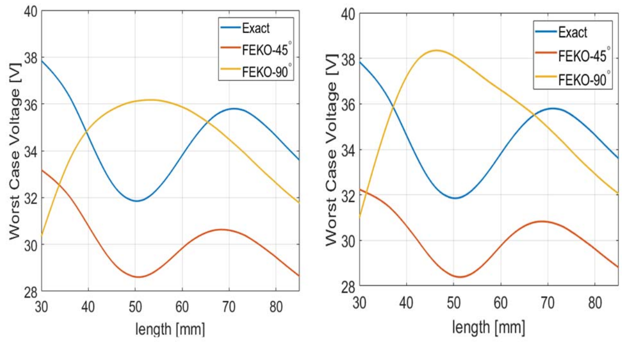
Where Z_0 is the free space impedance, W is the energy density. The worst-case coupled voltage must be integrated numerically or analytically over the simulated/calculated over the limits of frequency spectrum. The lower and upper bounds of frequency values are given by f_1 and f_2. The parameter $L_w(f)$ is given as:

$$L_w(f) = \frac{V_{0,L}(f)}{E_i} \tag{3}$$

Where $V_{0,L}(f)$ is the frequency dependent coupled voltage to loads given by (1) and E_i is the amplitude of incident electric field strength (V/m).

3 Results and Discussion

In this section results for three different PCB trace shapes are presented. Besides a straight trace, a 45° bent symmetrical trace, and a 90° bent symmetrical trace were considered. As discussed earlier, (1) calculates the exact coupled voltage to loads of a straight trace. This expression does not work for non-straight traces such as the 45° or 90° bent traces. To calculate the worst-case coupled voltage for the non-straight traces, we have used the commercial EM simulator Altair FEKO. To validate our designs, we have modeled and simulated for coupled voltage to loads of a straight trace and compared it with (1). Fig. 2 shows coupled voltage (in dBV) comparison of a straight trace simulated using FEKO and calculated using (1). The low-freq approximation in Fig. 1 is an approximated equation valid for only electrically small traces ($L \ll \lambda$). The exact is shown in (1), the simplification ($h \ll \lambda$) and the result from FEKO are in good agreement with each other.



(a) (b)

Figure 3. Worst-case coupled voltage vs length of the trace for three different trace shapes at (a) Load 1 and (b) Load 2.

The worst-case coupled voltage was calculated over a particular frequency spectrum for three different trace shapes of equal length and width. Fig. 3 plots worst-case coupled voltage versus various trace lengths for three different trace shapes. Both ends of the traces are matched with 50 Ω loads and a normal plane wave incidence has been used with a 1 V/m incident electric field strength. The lower and upper frequency values are 0.1 GHz and 4 GHz, respectively. Fig. 3a and 3b plots worst-case coupled voltage for both load ends, i.e., load 1 and load 2 of the traces, respectively. The worst-case coupled voltage for straight and 45° trace observes an oscillating pattern as the trace length increases. The oscillating pattern is similar to the behavior of Bessel function of zeroth order of first kind due to its decaying pattern. Furthermore, the straight trace couples more to the external EM field than a 45° trace. Moreover, one can also observe that the smaller the trace lengths are more prone to the external EM field coupling. The frequencies from lower side of the spectrum contributes most to the overall coupling to the loads. However, the 90° trace follows a unique pattern. Due to small impedance change at the sharp corner, some of the signal reflects back to both loads thus contributing constructively at some frequencies while destructively at other frequencies.

Other studies such as change in load and source impedance, incidence angles, relative permittivity, dielectric thickness, width of trace and frequency spectrum are currently being performed. These results will also indicate interesting behavior, which is significantly useful in understanding the EM field interaction with various properties of PCB traces with different shapes.

4 Summary

The worst-case coupled voltage to loads of realistic PCB trace shapes has been calculated, simulated and compared. The results indicated that on average straight trace couples more to an external EM field than a 45° trace. However, the 90° has a half sine-wave type length versus worst-case coupled voltage relation. More investigation on such problems will yield interesting results, which in turn are helpful to introduce new trace layout design rules to minimize external EM coupling.

5 Acknowledgements

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