Capacitive Coupling Analysis of TSV Array in 3D Packaging

Luo Guang-Xiao[1], Li Er-Ping[2], Wei Xing-Chang*[2], Cui Xiang[1]*

[1] North China Electric Power University, Beijing, China, e-mail: guangxiao.luo@ncepu.edu.cn

[2] Cyber Innovation Joint Research Center, Zhejiang University, Hangzhou, China, e-mail: *weixc@zju.edu.cn*

Abstract

In 3D-TSVs (through silicon vias) interposer layer, the capacitive coupling effects of TSV array are modeled and analyzed for signal transmission. To consider the semiconductor characteristics, the multi-conductor model is presented to model the TSV array by combining the MOS capacitance with the passive RLGC parameters. After that, the values of MOS capacitance and RLGC are extracted. Finally, by using model order reduction, the capacitive coupling characteristic of TSV array is simulated and analyzed for the signal transmission.

1. Introduction

The 3D chip stacked package with through silicon via (TSV) technology is a promising solution to overcome the density and size limitation of conventional single-chip package, and has shown its advantages of power distribution network and signal transmission[1]. Recently, there has been a great interest in TSV interposer layer, where the CPU, DRAMs and RF dies can be flipped on this layer, and the mixed signal is switched by TSVs array. A great deal of research has been done to model and analysis TSV[2-4], but these works are mainly focused on the single TSV pair, and few works had been done for modeling the multiple TSVs array in the interposer layer.

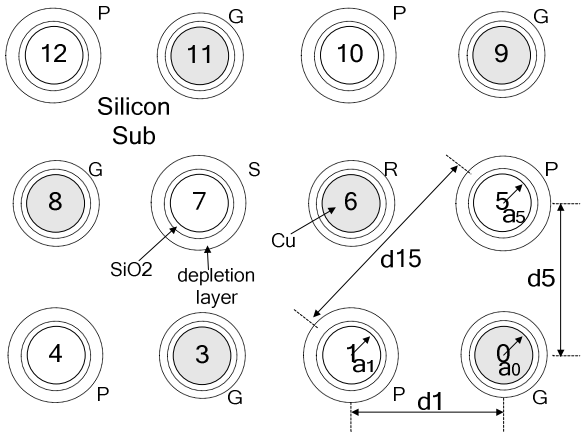


Fig.1 Signal-Reference TSVs and Power-Ground TSVs Array on interposer layer

In this paper, the capacitive coupling effects of TSVs array are modeled and analyzed for signal transmission. By considering the semiconductor characteristics, the depletion width and the metal-oxide-semiconductor(MOS) capacitance is calculated with lambert W function. Furthermore, the multi-conductor model is presented for TSVs array by combining the MOS capacitance with the passive RLGC matrix, and a calculation method is proposed to extract the parameters in the model. Finally, by using model order reduction, the capacitive coupling characteristic of TSVs array is simulated and analyzed for the signal transmission.

2. Multi-conductor Model for TSV Array

TSV array in the interposers and chips can be modeled by using multi-conductor transmission lines method. With the bias voltage V_{TSV}, the MOS capacitance needs to be used for the analysis of the metal-oxide-semiconductor structure as shown in Fig.1, where a is the radius of Cu, b is the radius of Cu plus the thickness of oxide layer, and W is the depletion width of p-type silicon.

The whole MOS capacitance is consisted of oxide layer capacitance C_{ox} and the depletion layer capacitance C_{dep} in the silicon substrate. Supposing the depletion width of p-type silicon is W, which is depended on the bias

978-1-4673-5225-3/14/$31.00 ©2014 IEEE

voltage V_{TSV}. For a positive bias voltage, the lambert W function[5] can be used to get the solution in the static field. Let $k_1 = \frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}} \ln(\frac{b}{a}) - 0.5$ and $k_2 = \frac{2\varepsilon_{S_i}\varepsilon_0}{qN_A b^2}$, where N_A is the doping concentration, q is the electron charge, ε_{S_i} and $\varepsilon_{S_iO_2}$ are the relative dielectric constants for p-type silicon and SiO2. The depletion width W can be obtained as below,

$$W = (e^{0.5*lambertw\left(2*(k_1+k_2*V_{TSV}-k_2*V_{FB})*e^{2k_1}\right)-k_1} - 1)*b, \tag{1}$$

where the solution to the lambert W function can be got from the programmed code or mathematical tools such as mathematica or matlab. When increasing the bias voltage, the silicon enter the inversion region, but the inversion region of p-type silicon is difficult to form because of the slow generation speed of minority carriers at the surface of silicon substrate. Therefore, at high frequency, the depletion width reveals its maximum value, is given as

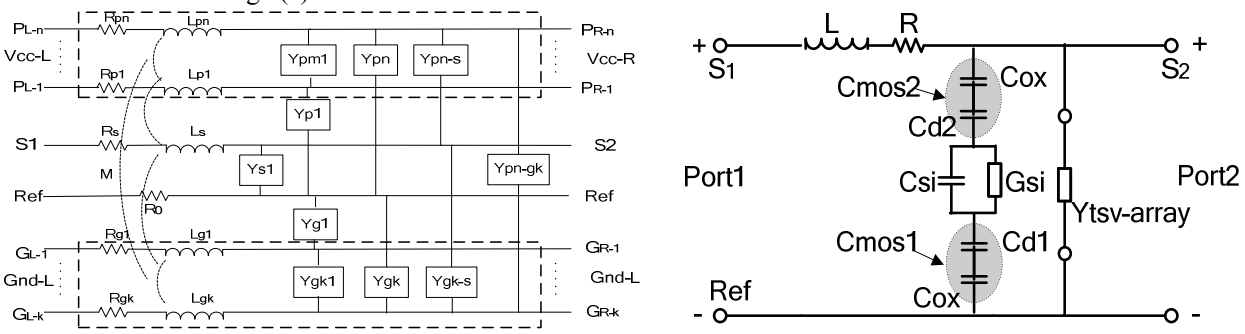
$$W_T = (e^{0.5*lambertw((4k_2*\phi_F-1)/e)+0.5} - 1)*b. \tag{2}$$

In the inversion regions, the threshold voltage $V_{Threshold-TSV}$ is related to the maximum depletion width W_T by

$$V_{Threshold-TSV} = V_{FB} + 2\phi_F + \frac{\varepsilon_{Si}}{\varepsilon_{SiO_2}} \ln(\frac{b}{a}) \frac{qN_A}{2\varepsilon_{S_i}\varepsilon_0}[(b+W_T)^2 - b^2], \tag{3}$$

thereafter, the per-unit-length depletion layer capacitance C_{dep} is obtained by using the analytical formulas of coaxial cable, then the MOS capacitance can be get by connecting C_{ox} and C_{dep}.

It is difficult to get the equivalent lumped circuit by directly using the numerical results for the reason of the oxide and depletion layers. But considering the thickness of the silicon oxide and depletion layers is very thin in comparing with the distance between and radius of TSVs, the capacitance of the oxide and depletion layers can be get by using the coaxial cable formula, which is based on the calculation of depletion width in the p-type silicon. As shown in Fig.1, the conductor "Ref" is selected as the reference ground in the multi-conductor method, connecting the inductance matrix of multiple TSVs and conductance matrix of the resistive layer in the silicon, the equivalent circuit model is created as in Fig.2(a).



(a) (b)

Fig. 2 Equivalent circuit for power TSVs array and S-R TSVs (a) MTL model (b) S-R TSVs model

Based on the calculation of depletion width, the capacitance and conductance matrix is modeled with multi-conductor method, the wide-separation approximation method can be used to get the inductance, the inductance matrix is gotten by

$$L_{cnn} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_n^2}{(b_n+W_n)(b_0+W_0)}\right) * h_{TSV}, \tag{4}$$

and

$$L_{cmn} = \frac{\mu_0}{2\pi} \ln\left(\frac{d_m d_n}{d_{mn}(b_0+W_0)}\right) * h_{TSV}, \tag{5}$$

where b_n is the radius of Cu plus the thickness of oxide layer for each TSV respectively, d_n is the center distance to the reference TSV, d_{mn} is the center distance between *m*th and *n*th TSVs, and W_n is the depletion width around TSV. When W_n is not equal to zero, the inductance matrix L_{cmn} is used to calculate the capacitance and conductance matrix; when W_n and the thickness of SiO2 are equal to zero, L_{cmn} becomes the inductance matrix of the multi copper cylinders without the MOS effect. The capacitance matrix and conductance matrix are calculated by $C = \mu_0 \varepsilon_{Si} L_c^{-1}$ and

$G = \frac{\sigma}{\varepsilon_{Si}} C$ in the silicon resistive layer. After that, the following admittance matrix can be used to describe the circuit in Fig.3 as

$$\begin{bmatrix} I_L \\ I_R \end{bmatrix} = \begin{bmatrix} Z^{-1} & -Z^{-1} \\ -Z^{-1} & Y + Z^{-1} \end{bmatrix} \begin{bmatrix} V_L \\ V_R \end{bmatrix} , \tag{6}$$

where I_L and I_R is the current into the left and right nodes respectively, and V_L and V_R is the voltage of left and right nodes respectively. The size of matrix Z and matrix Y is $(n+k+1)*(n+k+1)$, and $Z = R + j\omega L$. Y matrix is

$$Y = (G + j\omega C) \,||\, (j\omega C_m) \quad , \tag{7}$$

where C_m is $(C_{mos2} \,||\, C_{mos1})$ for the power-ground TSV, power-reference TSV and signal-reference TSV, $0.5C_{mos1}$ for the ground-ground TSV and reference-ground TSV, $0.5C_{mos2}$ for power-power TSV and signal-power TSV.

3. Coupling Coefficient and Signal Transmission Model

3.1 Model Order Reduction

For the power-ground TSV's array, model order reduction method of common voltage can be used to simplify the calculation. When the common voltage V_{CC-L}, V_{CC-R} and G_{nd-L}, G_{nd-R} are used to excite all power-ground ports in this multi-port network, the admittance matrix can be reduced to simplify the model order. The incidence matrix of the all ports can be used to reduce the orders of the admittance matrix as

$$Y_k = A^T Y_j A , \tag{8}$$

where Y_j is the original admittance matrix from equation (6), Y_k is the new admittance matrix, and A is the incidence matrix. After the mode order reduction, the matrix size of Y changes from $2(n+k+1)*2(n+k+1)$ to $6*6$. Thus, a multiport network model with six ports is obtained, and it can be used to get the noise coupling characteristics between the power networks and signal TSV in the interposer layer.

Furthermore, let the ports of power and ground is open for capacitive coupling analysis of power TSV array. The impedance matrix Z_k can be transformed from the admittance matrix Y_k, where the relative rows and column in the impedance matrix can be deleted for the opened power and ground ports. After that, the two-port network parameters Z_f are obtained. This two-port network is equivalent as a lumped circuit as depicted in Fig. 3, the capacitive coupling coefficient $Y_{tsv-array}$ can be extracted from the self-impedance Z_{f22}, the Cm is $(C_{mos2} \,||\, C_{mos1})$.

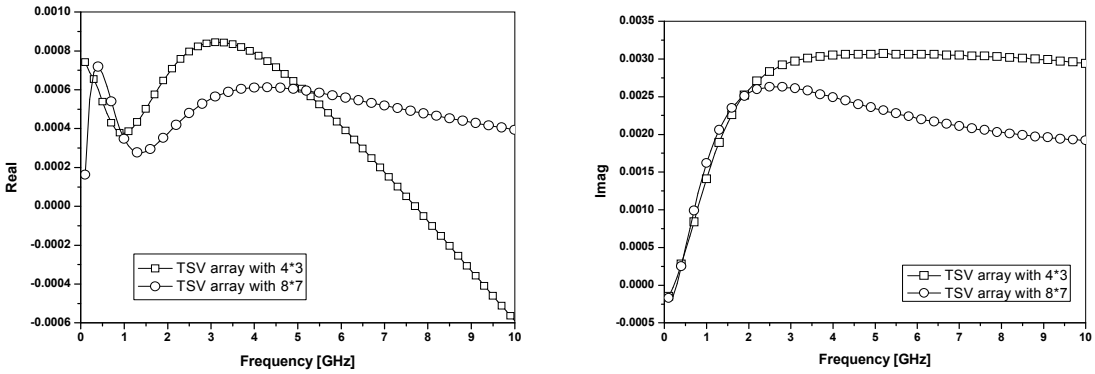
$$Y_{tsv-array} = 1 / Z_{f22} - (G_{Si} + j\omega C_{Si}) \,||\, (j\omega C_m) . \tag{9}$$

The transmission characteristic of the signal-reference TSVs in the TSVs array can be obtained by using the equivalent lumped circuit, where the effect of TSV array is considered in this model. As shown in Fig.2 (b), C_{d1} and C_{d2} are the depletion capacitors, and $Y_{tsv-array}$ is the capacitive coupling coefficient.

3.2 Simulation Results

Considering the TSV with the metal radius of $10\mu m$, a height of $90\mu m$, the center distance d between two parallel TSVs is $50\mu m$, the thickness of oxide layer is $0.1\mu m$, N_A is $2e15/cm^3$, the resistivity of silicon substrate is $6.86\Omega.cm$, and the resistivity of Cu is $(1.77E-8)\Omega.m$. Supposed the DC bias voltage V_{TSV} is $1V$ for power and signal TSVs, and $0V$ for ground TSV and reference TSV, then the depletion width W is obtained as $0.635\mu m$ and $0.184\mu m$ respectively. Thus, we get that $L = 57.94pH$, $C_{ox} = 1.96pF$, and $G_{si} = 2.64mS$, $C_{si} = 18.94fF$, $C_{mos2} = 0.648pF$, $C_{mos1} = 1.226pF$ in the Fig.2(b), and the value of resistor changes with frequency for considering the skin effect in circuit simulation.

For TSVs arrays with 4*3 and 8*7 dimension sizes, the proposed method is used to analysis the capacitive effects of TSV array on signal transmission, the capacitive coupling coefficient is shown in Fig.3(a) and (b). The transmission characteristics for different array are simulated as Fig.4, the effects of TSV array is an important factor for signal transmission. Further simulation work reveals that the capacitive effects of TSV array can be neglected for the no-doping silicon. For active layer with heavy-doping silicon, the capacitive effect is serious, because the capacitive coupling increases the loss of silicon substrate.



(a) (b)

Fig. 3 Coupling coefficient *Ytsv-array* (a) real part (b) image part

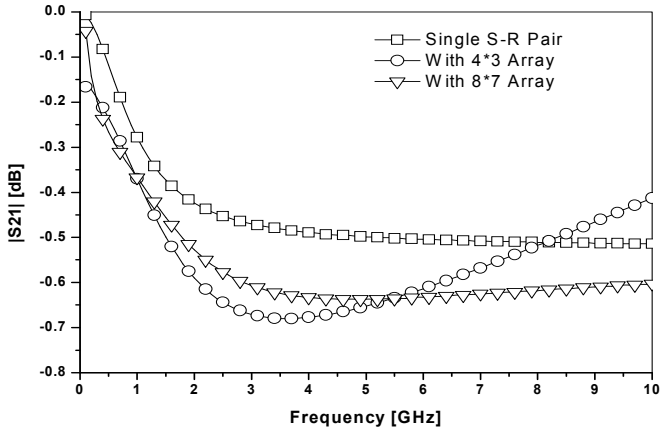


Fig. 4 Capacitive effect of power TSVs array on signal transmission

4. Conclusion

The capacitive coupling effects of TSVs array are modeled for the analysis of signal transmission in this paper. By considering the semiconductor characteristics, the multi-conductor model is presented to model the TSVs array by combining the depletion width, MOS capacitance with RLGC matrix, and the calculation method is suggested to get the model parameters. Finally, by using model order reduction, the capacitive coupling characteristic of TSVs array is simulated and analyzed for the signal transmission.

5. Acknowledgement

This work was supported by the Fundamental Research Funds for the Central Universities of China (12MS125), National Science Foundation of China (61274110 & 61371031), Zhejiang Provincial Natural Science Foundation of China (LZ12F04001 & Z1110330), and National Science and Technology Major Project of the Ministry of Science and Technology of China(2014ZX02501).

6. References

1. E.-P. Li, *Electrical Modeling and Design for 3D System Integration:3D IC and Packaging , Signal Integrity, Power Integrity and EMC,* Wiley-IEEE Press, New York, 2012.
2. G. Katti, M. Stucchi, K. De Meyer, and W. Dehaene, “Electrical modeling and characterization of Through Silicon via for three-dimensional ICs,” *IEEE Trans. on Electron Devices,* vol.57,no.1, pp.256-262, Jan. 2010.
3. J. Kim, JS Pak, J. Cho, and J. Kim, “High-frequency scalable electrical model and analysis of a Through Silicon Via (TSV),” *IEEE Trans. on Comp., Packag. and Manuf. Techn*., vol. 1, no. 2, pp. 181-195, Feb. 2011.
4. Tapobrata Bandyopadhyay et al., “Rigorous electrical modeling of Through Silicon Vias (TSVs) with MOS capacitance effects,” *IEEE Trans. on Comp., Packag. and Manuf. Techn.,* vol.1, no.6, pp.893-903, June 2011.
5. R. M. Corless, G. H. Gonnet, D. E. G. Hare, D. J. Jeffrey, and D. E. Knuth, “On the Lambert W Function,” *Advances in Computational Mathematics*, vol.5, pp.329-359, 1996.