

Package Design Methodology in Consideration with Signal Integrity, Power Integrity and Electromagnetic Immunity

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Abstract

A design concept and methodology for package with consideration on signal integrity, power integrity and electromagnetic immunity is proposed in this paper. Each part of the package such as bonding wire, via or bump has a significant influence on the performance of entire chip-package-board system, and these effects to signal, power integrity prosperities are discussed based on the numerical analysis method and SPICE-like simulator. Furthermore, a novel design for filter in package is proposed for enhancing immunity of integrated circuits. Finally, the methodology for design optimization can be achieved based on the analysis results.

1. Introduction

The advance in semiconductor field induces a series of problems and challenges in the signal integrity (SI), power integrity (PI) as well as electromagnetic immunity range. In particular, electrical properties of package are crucial to the semiconductor system, and package is more than often adopted to achieve better performance for a chip-package-board combination. Interconnects of package are discontinuities for signal and power transmission, and they are easily affected by many factor such as cross-talk, parasitic coupling, impedance mismatch, simultaneous switching noise (SSN) and electromagnetic interference. Many publications have discussed the SI and PI issues for the package. A review of electromagnetic compatibility (EMC) analysis technologies for packages, printed circuit boards, and novel interconnects has been proposed in [1]. SI and PI issues and electromagnetic interference effect to the system on package have also been investigated with regard to the package as a part of chip-package-board system [2]–[3]. Generally, SI, PI and EMC analysis have achieved a lot for a given package model. However, people need a principle for providing assistance to obtain good SI, PI and EMC properties during a package design process.

In this paper, we proposed a design concept and methodology for package with consideration on SI, PI and electromagnetic immunity. The arrangement of this paper is described as follows. Section 2 discussed the effect to the SI and PI with changing the number and relative location of different elements in package. Furthermore, in section 3, a novel design and implementation for the miniature filter in package can enhance the electromagnetic immunity under interference.

2. Design Methodology for Signal and Power Integrity

2.1 Designs in Consideration of Variation of Ground/Return Paths Number

A typical package is composed of the bonding wire, via or through-silicon-via, lead frame, bump ball and routed trace as shown in Fig.1. The ground plays a role as a return path for the signal and power in electronics equipment and a well-designed return path is a necessary element in high speed and high frequency circuits. The number of the return path becomes a problem during a semiconductor circuits design. As shown in Fig. 2, the number of ground bonding wires which locate around signal or power wires varies and depends on the quality requirement of the signal and power transmission.

In this section, we discuss the effect of the ground conductor number to signal and power integrity based on the parameter variation since the values of inductance and capacitance have significant relationship with the SI and PI performance. The derivation of the capacitance is implemented for a N —conductor system. Once the i th of N conductors is assigned to the ground, the column and row of the C_{ii} is eliminated for its ground property [4] and the remaining self-capacitance C_{jj} becomes the new expression in (2), where $j \neq i = 1, 2, \dots, N$. As increasing the ground conductor number, the self-capacitance of remained conductors would become larger while the mutual capacitance did not change as (1). A four-conductor model was established in Q3D simulator for verification and the result is shown in Table I.

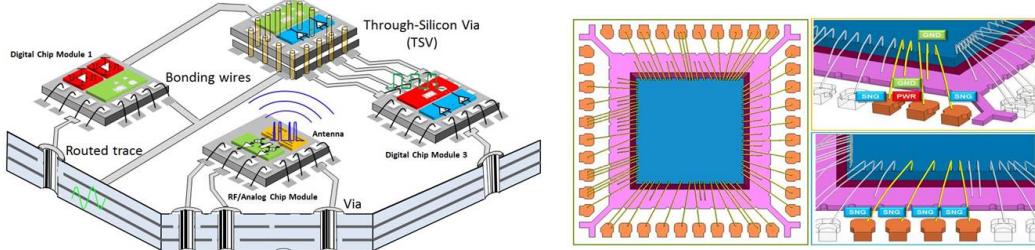


Fig. 1. (left) A typical physical configuration for package compositions.

Fig. 2.(Right) Ground trace arrangement strategy for improvement of SI and PI in package design process.

$$C_{jj_new} = C_{jj_old} + C_{ji_old} \quad \text{and} \quad c_{ij_new} = c_{ij_old} = \mathcal{C}_{ij} - \frac{\left(\sum_{m=0}^n \mathcal{C}_{im} \right) \cdot \left(\sum_{m=0}^n \mathcal{C}_{mj} \right)}{\sum_{l=0}^n \left(\sum_{m=0}^n \mathcal{C}_{lm} \right)} \quad (1)$$

TABLE I
RELATIONSHIP BETWEEN CAPACITANCE/INDUCTANCE AND GROUND NET NUMBER

# of Ground Net	C_{II} (pF)	C_{33} (pF)	C_{I3} (pF)	L_{II} (nH)	L_{33} (nH)	L_{I3} (nH)
0	0	0	0.5777	3.5618	3.4087	1.2951
1 (wire 2)	0.2631	0.2381	0.5777	3.0828	3.0304	0.8664
2 (wire2 &4)	0.3341	0.5004	0.5777	2.7863	1.9600	0.3031

When one of the N conductors is changed to be the return path for the others, the mutual inductance caused by the opposite direction current induces and reduces the loop inductance. The relationship between the new and old self and mutual inductance in N conductors system can be expressed in (2), where $j \neq k \neq i = 1, 2, \dots, N$.

$$L_{jj_new} = L_{jj_old} + L_{ii_old} - 2L_{ji_old} \quad \text{and} \quad L_{jk_new} = L_{jk_old} + L_{ii_old} - L_{ji_old} - L_{ki_old} \quad (2)$$

As seen from the equation above, the self and mutual inductances are varying with the number of return path. A simulation results based on four conductors model in Q3D is also shown in Table I and validate the derived equation. In addition, the lower case c in (1) represents the coefficient, and c_{ii} and c_{ij} are the coefficient of capacitance and coefficient of induction, respectively.

The discussion in this section has shown the effect of changing ground net or return path number to corresponding electrical characteristic by influencing the lumped value. The inductance and capacitance variation could affect the crosstalk and S parameter in SI and impedance in PI. During the design procedure, the SI and PI can be controlled by means of the number adjustment for the conductor with special property.

2.2 Designs in Consideration of Locations of the Package Elements.

Besides the number of ground property conductor, the relative location of nearby conductors is also a crucial factor for the performance of package. In particular, in package system, the distance between the ground and signal/power bonding wires, via, and routed trace affects the inductance and capacitance and therefore results in enhanced or deteriorative scattering parameters. As shown in Fig. 3, we established a signal-ground-signal partial package model to describe the location effect.

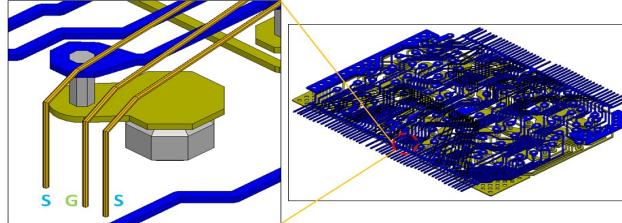


Fig. 3. The signal-ground-signal partial package model for location arrangement consideration.

Not only influencing the signal integrity, the location variation also affects the power integrity. Since the inductance and capacitance value has changed with the location condition, the self and transfer impedances also vary to follow it. The effects on the power and ground traces with different gap are shown in Fig. 4. Lower target impedance is always regarded as the good performance for PDN, and the enhancement of return path could add the capacitance elements and then reduce the target impedance. In general, to obtain a better power integrity, the safe approach is to design enough return paths as close as the power transmission trace.

Above all, in this section, the design methodology of package for considering signal and power integrity has implemented by the optimization of ground elements number and return path location.

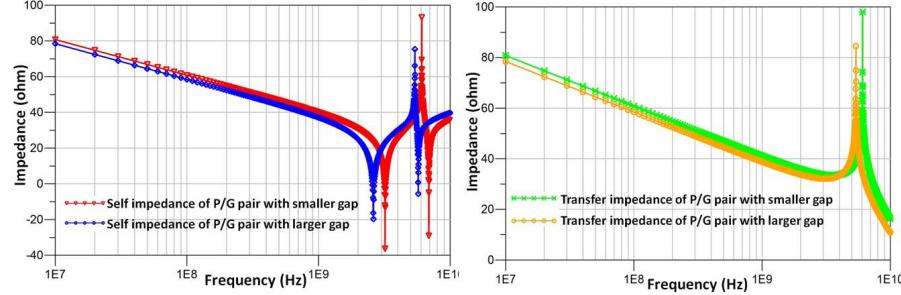


Fig. 4. Self and transfer impedances for different gap between power and return path.

3. A Novel Filter in Package Design for Electromagnetic Immunity Enhancement

There is a typical trend that the complexity of integration and speed of operation in modern electronic system is continuing to increase. Therefor the immunity of ICs is crucial to the performance of the relative electronic device even the entire operating system. As shown in [5], the immunity of integrated circuits was extracted by the comparison between simulation and measurement based on direct power injection method. To improve the immunity, a plenty of useful methods about chip or board optimization have been introduced in [6] – [7]. However, in most cases, the designers for the ICs and board are separate and both of them only consider the SI, PI and EMC in their own level. Here we proposed a design concept of novel filter in package to enhance the immunity for ICs. In the design approach, the filter is integrated in the package and the chip-filter-package system is regarded as a unit. Therefore, it does not take extra space and it also does not influence the function elements in core and board. The application of the filter reduces the noise in specific frequency ranges and the weak points of immunity are strengthened.

The filter in package design is a challenge since the large enough value for inductance and capacitance used in megahertz to a few gigahertz range is hard to achieve in such limited available space. For solving this problem and make full use of the miniature area, we proposed a filter structure which is composed of meander line and large pad configuration shown in Fig. 5. This filter structure is compact but could achieve the large inductance and capacitance in limited space which locates on the top side of package layers. The red parts just below the die in Fig. 6 upper and lower describe the filter positions in ball grid array (BGA) and quad-flat no-leads (QFN) packages, respectively.

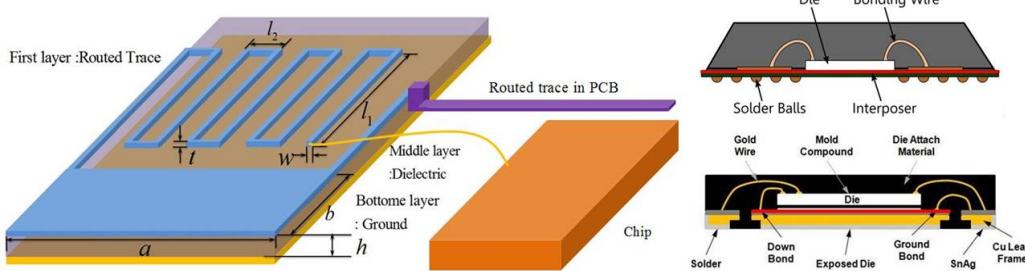


Fig. 5. (left) Proposed filter in package structure with meander line and large pad.

Fig. 6. (right) Position for the designed filter in different type packages

As shown in Fig. 6, the undesired signal has been obstructed in the filter path when the signal propagates from the board to chip. For a filter structure with physical description as in Fig. 5, if the number of the longer transmission line is N , the total inductance and capacitance is depicted in (3) and (4). They both include the meander line part and large pad part and derived based on the partial element calculation method.

$$L = \left(\frac{\mu_0 a}{2\pi} \left(\ln \frac{2a + 3a + 2b}{6a} \right) - 2 \times 10^{-7} \frac{t}{b} a \right) + N \cdot \left(\frac{\mu_0 l_1}{2\pi} \left(\ln \frac{2l_1 + 1}{w} + \frac{w}{2} + \frac{l_1}{3l_1} \right) - 2 \times 10^{-7} \frac{t l_1}{w} \right) + (N-1) \cdot \left(\frac{\mu_0 l_2}{2\pi} \left(\ln \frac{2l_2 + 1}{w} + \frac{w}{2} + \frac{l_2}{3l_2} \right) - 2 \times 10^{-7} \frac{t l_2}{w} \right) \\ + (N-1) \cdot \frac{\mu_0 l_1}{2\pi} \left\{ \ln \frac{2l_1}{\sqrt[4]{[t^2 + l_1^2][t^2 + (2w + l_1)^2]}} + \frac{13}{12} - \frac{1}{3} \frac{l_1^3}{w^2 t} \tan^{-1} \frac{t}{l_1} - \frac{1}{3} \frac{t l_1}{w^2} \tan^{-1} \frac{l_1}{t} + \frac{2}{3} \frac{(w + l_1)^3}{w^2 t} \tan^{-1} \frac{t}{w} \right. \\ \left. + \frac{2}{3} \frac{t (w + l_1)}{w^2} \tan^{-1} \frac{(w + l_1)}{t} - \frac{1}{3} \frac{(2w + l_1)^3}{w^2 t} \tan^{-1} \frac{t}{2w + l_1} - \frac{1}{3} \frac{t (2w + l_1)}{w^2} \tan^{-1} \frac{2w + l_1}{t} - \frac{1}{2} \frac{a}{w} \ln \frac{t^2 + (2w + l_1)^2}{t^2 + l_1^2} \right\} \quad (3)$$

$$+ (N-2) \cdot \frac{\mu_0}{4\pi} \left[\left(\ln \frac{4l_2}{l_1} - 1 \right) - 2l_2 \left(\ln \frac{2l_2}{l_1} - 1 \right) \right] + (N-3) \cdot \frac{\mu_0}{4\pi} \left[\left(\ln 2 \left(\frac{4l_2}{w+t} \right) - 1 \right) - 2l_2 \left(\ln \frac{4l_2}{w+t} - 1 \right) \right] \quad (4)$$

$$C_{Total} = \frac{\epsilon_r \epsilon_0 a \cdot b}{h} + \left[N \cdot \frac{\epsilon_r \epsilon_0 w \cdot l_1}{h} + (N - 1) \cdot \frac{\epsilon_r \epsilon_0 w \cdot l_2}{h} \right] (F) \quad (4)$$

From the equation above, the parameters are determined by the physical configuration of the meander line and large pad structure. Once arrange the physical parameter properly, the desired filter effect could be obtained. In [5], the immunity of designed ICs extracted based on direct power injection method is vulnerable around 70MHz, 200MHz and 400MHz. A band stop filter which has stop band at those weak points was designed to reduce the injection noise and thus enhance the immunity at the sensitive range. The comparison between the immunity with or without filter is depicted in Fig. 7. It is obvious that the implementation of the band stop filter enhanced the immunity in the vulnerable immunity ranges. The property of the filter could also vary for multi-purpose for a improvement of the IC immunity.

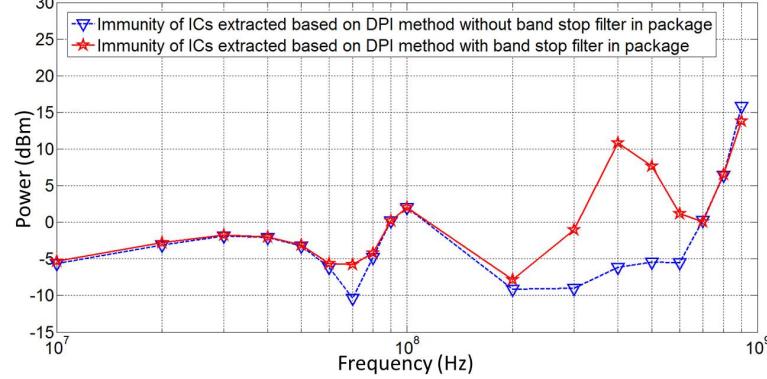


Fig. 7. Comparison between the immunity with or without band stop filter.

4. Conclusion

The design concept and methodology for package with desired signal and power integrity as well as the immunity has been described in this paper. The effects of the ground elements number and relative location between signal/power and return paths were discussed based on their influence on the inductance and capacitance values which determine the performance of package. Furthermore, a novel design of filter in package to enhance the immunity of ICs based on meander line and large pad was also introduced. As a result, the discussion in this paper could be a guidance and assistant for package design with consideration on signal, power integrity and electromagnetic immunity.

5. References

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