A Broadband FPGA Digital Beamformer for the Advanced Focal Array Demonstrator (AFAD)

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Abstract

Broadband Focal Array Beamformers offer the potential to increase the field of view of reflector antennas. Such systems require a processing bandwidth of order 1 GHz and need to beamform tens of polarized beams from over 100 array elements. A number of such systems have been built but none with the bandwidth and number of elements required by the Square Kilometre Array. In this paper we outline the digital beamformer for the Advanced Focal Array Demonstrator being developed at the National Research Council's Dominion Radio Astrophysical Observatory – a system that meets the bandwidth and beam requirements proposed for the Square Kilometre Array.

1. Introduction

Focal array beamformers are implemented by placing an array of feed elements near the focal plane of a reflector antenna [1]. One of the largest systems developed and the first to demonstrate the polarization performance of a broad band phased array feed was the PHased Array feed Demonstrator (PHAD) developed at the DRAO [2,3]. Its predecessor, the Advanced Focal Array Demonstrator (AFAD), described in a companion paper [4], uses a 2D array of 128 Vivaldi elements, organized as an 8 x 8 array x 2 linear polarizations. Each element contains an L-band LNA and gain stage whose RF output is directly converted by broadband analogue to digital convertor (ADC) which coherently digitizes the RF signal at 2 Gsps. The digital output is filtered into a 500 MHz band and a 1 Gsps stream is transmitted to the beam former via fibre at 10 Gbps. The digital beamformer receives 128, 10 Gbps streams and filters each into 7.5 MHz channels. A channel from each element is then combined as a weighted sum with the same channel on the other elements to form a beam for a specific channel. The operations for forming a beam, B_k, for a channel, j, from antenna elements, i, weighted by beamformer coefficients, W, is given by,

$$B_k(t,j) = \sum_{i=1}^{128} E_i(t,j) \bullet W_{i,j,k} \qquad (1)$$

The following section outlines the AFAD beamformer and describes how these operations are mapped on the hardware.

2. The AFAD FPGA Digital Beamformer

The block diagram of the AFAD is shown in figure 1. The system consists of 8 beamformer cards which filter the data and form 32 polarized beams from 128 Vivaldi elements. The cards are housed in an industry standard ATCA card cage. Each card processes 16 elements and forms 4 polarized beams. Element data are received by a card on the front panel via 16 x 10 Gbps fibre inputs. Beamformer data are output via 10 Gbps fibre at the rear of the chassis via the ATCA Zone 3 connector.

Each beamformer card is based on a Kermode (pronounced Kurr-mo-dee) FPGA processor card being developed by NRC-HIA at the DRAO. The Kermode processor is a general purpose FPGA compute blade that is designed to be used as a beamformer, correlator, and a real-time compute engine for solving inverse matrices used in adaptive optics systems such as the Narrow Field InfraRed Adaptive Optics System (NFIRAOS) [6] for large optical telescopes such as the Thirty Meter Telescope (TMT)[5].

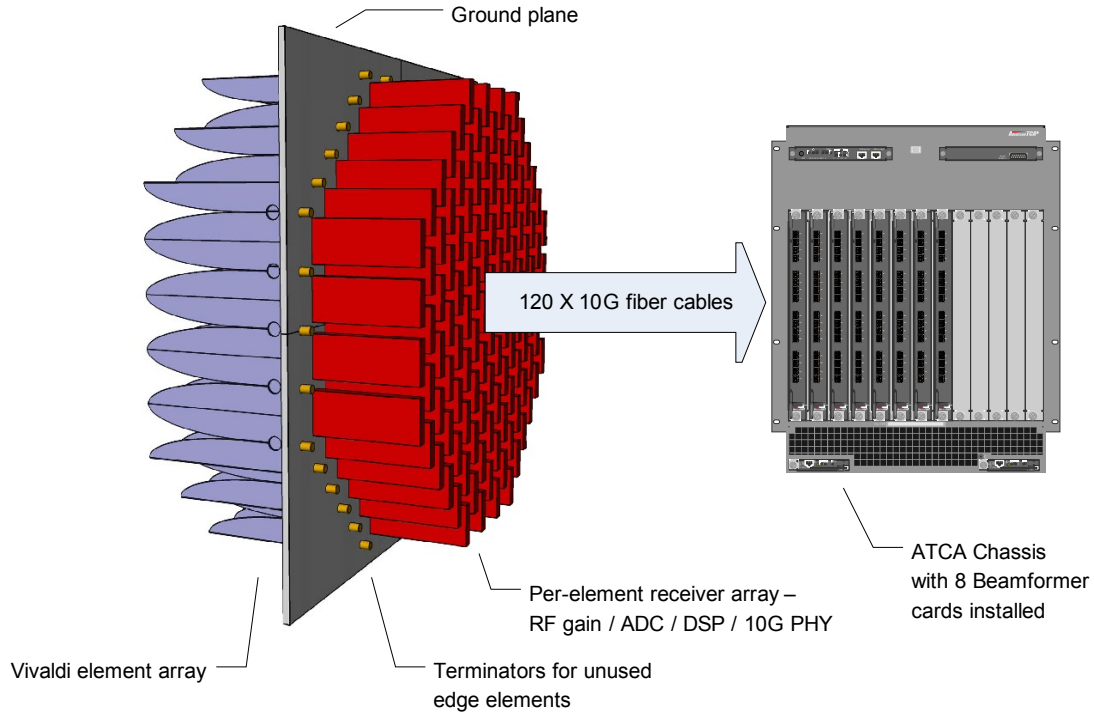

Figure 1 A block diagram of the Advanced Focal Array Demonstrator

The Kermode processor contains 8 high-end Xilinx Virtex-6 FPGAs interconnected in unique but uniform ways. In addition, the array of FPGAs is also connected to its front panel inter-connect, the Zone 3 (ATCA application specific high-speed I/O) connector, and the Zone 2 (ATCA mesh backplane) connector. As shown in figure 2, the FPGAs are arranged in 2 columns. Each left-hand column FPGA (F1 to F4) has full-duplex connectivity to four front panel 10 Gbps links and unidirectional high-speed links to the Zone 2 ATCA mesh, as well as connections to the right-hand column FPGAs. Each right-hand column FPGA (R1-R4) has full-duplex ultra-high speed connectivity to the Zone 3 user I/O connector, which can connect to any user-defined RTM (Rear Transition Module) or user-defined backplane. R1-R4 each has uni-directional 6.5 Gbps links from the Zone 2 ATCA mesh, with matching uni-directional links to the F1-F4 FPGAs.

A low-jitter PLL on the card allows the master clock to be sourced from several sources making it possible for each card to act as or be the facilitator for the master clock source and distribute the clock signal to other cards in the chassis. As well, each card may operate with its own independent clock, suitable for purely packet-based processing with no global coherence requirements.

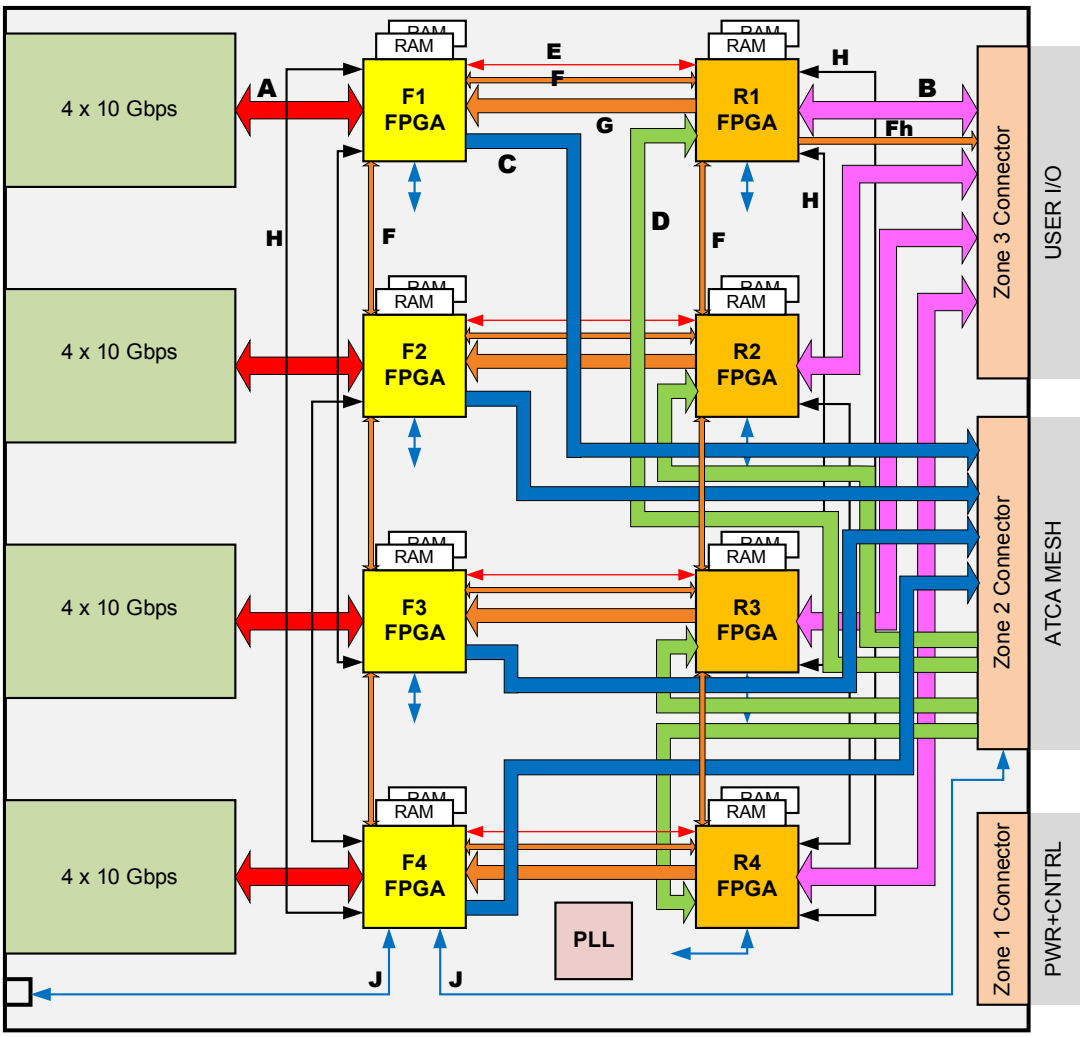

Figure 2 A block diagram of the general purpose Kermode FPGA compute blade.

Figure 3 shows how the AFAD beamformer processing operations are mapped on the Kermode FPGA compute blades. Data from sixteen elements enter a board via the front panel. The F1-F4 FPGAs perform FFTs on the inputs, and distribute the data amongst each other, on average keeping ¼ of their "native" data and shipping off the other ¾ to column companion FPGAs, using intra-column connections. Each F1-F4 FPGA contains a 1/64th sub-set of the frequency channels to be beamformed for all elements that enter the board. This subset of channels, from all elements, is transmitted on the Zone 2 mesh to R1-R4 FPGAs, such that each R1-R4 FPGA receives a 1/64th sub-set of channels from all elements that enter any board in the ATCA chassis. R1-R4 FPGAs beamform the channels, perform any other desired operations, and transmit real-time beam-formed frequency-domain data out to the Zone 3 connector.

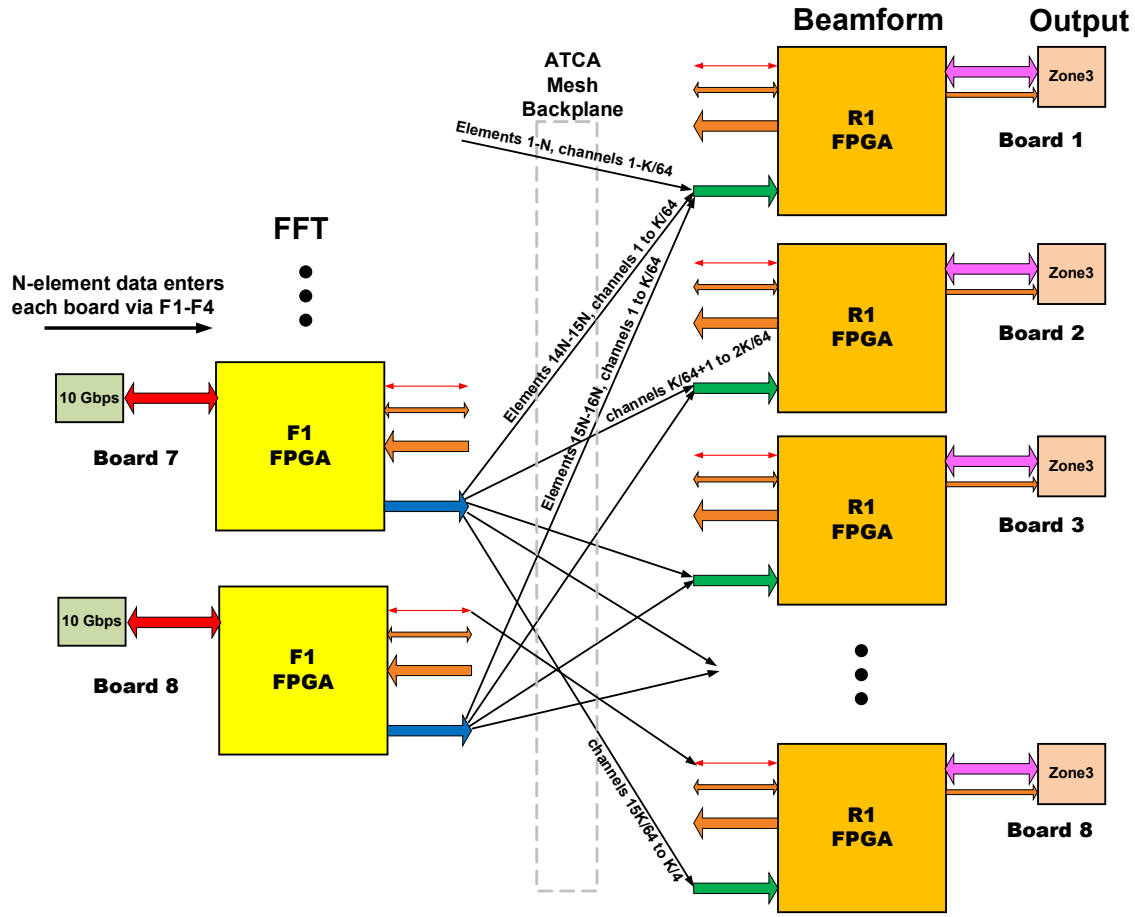

Figure 3 Shows the AFAD beamformer processing operations mapped onto the general purpose Kermode FPGA compute blades. Each R1 FPGA receives a subset (1/64) of frequency channels from all elements entering any board in the chassis. For simplicity, only the F1 FPGA on each card is shown.

3. References

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