On the modeling of complex circuits using behavioral component descriptions embedded into the full-wave TLM method

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Abstract

The simulation of modern microwave circuits is achieved using a variety of tools, chief amongst these are full-wave field solvers and behavioral circuit simulators. While the latter has the advantage of simplicity, field phenomena such as multiple random external noise sources, and complex device coupling are difficult to include. A full-wave model on the other hand incorporates these effects, but is computationally expensive to operate. This paper demonstrates the application of behavioral models embedded into a full-wave field solver, which removes the computational overhead of simulating complex ICs using field solvers, while maintaining the generality and simplicity associated with the behavioral model.

1. Introduction

Behavioral models describe components using only a simple I-V (current-voltage) relationship at each of the input/output ports of the device. Behavioral models are widely used in circuit solvers, due to their simplicity and accuracy, yet their use in full-wave field solvers has received little attention. The simulation of modern ICs using field solvers is becoming increasingly important, due to the ever decreasing size of modern circuits. Unfortunately, the similar reduction in the size of ICs makes their simulation using full-wave solvers computationally expensive due to the level of spatial discretisation required. Techniques to include electrically fine features in full-wave field solvers have been proposed [1], but limited attention has been given to incorporating electrically small features that have complex behavior, such as a full IC. In the work of So and Hoefer [2], a SPICE model was embedded into a full-wave field solver. This has the advantage of being able to use coarse spatial sampling in the field model, while retaining accuracy in the SPICE model, yet is dependent on the SPICE libraries and of limited computational efficiency due to the need to invoke SPICE at each time-step of the field solver.

In this paper we will demonstrate how the IBIS (Input/Output Buffer Information Specification) [3] [4] [5] description of an IC can be included in the Transmission-Line Modeling (TLM) [6] method which is an example of a full-wave field solver. It will be shown how the behavioral IBIS model is used to describe an IC, while the TLM simulation models account for coupling between two microstrip tracks. This approach removes the dependence on the SPICE libraries and is of significant computational advantage, since the need to call SPICE is no longer necessary.

IBIS is a behavioral modeling language widely used by IC manufacturers, most notably Texas Instruments [7].

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The method was pioneered by Intel in the early 1990's, becoming an Electronic Industries Alliance standard in 1995. An IBIS component description contains a collection of lookup tables, with typical, minimum and maximum values for the current, given an operating range of voltages. In Figure 1 the general equivalent circuit of the IBIS lookup tables is shown [8]. The load buffer only has one or both of the clamp tables, while a driver also includes measurements for the pullup and pulldown tables. An IBIS file can be generated from a circuit simulation of the IC, or by experimental measurements. The IBIS files provided by Texas Instruments, which are used in this paper, are measured experimentally. Also included in the model are the package resistance, inductance and capacitance, and the IC die capacitance for each port.

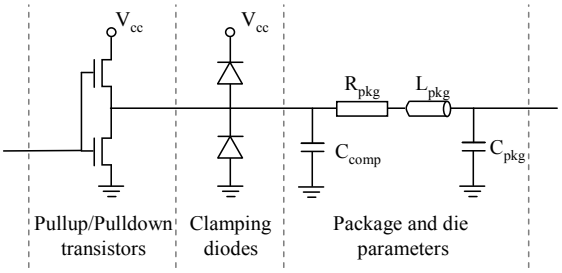


Figure 1 – Generic IBIS Buffer. A complex IC port is represented as pullup/pulldown transistors and clamping diodes with I-V lookup tables for each. Package parasitics and die capacitance are also given.

TLM is a time domain differential modeling method which utilizes the analogy between voltage impulses traveling on discrete sections of transmission-line and fields traveling in space [6]. In 3D TLM, the space is divided into cubes of interconnecting transmission-line sections, of volume Δl^3, where Δl is the spatial discretisation of the model. Simulation proceeds by a scatter-connect type algorithm, where voltage impulses are scattered at each node and connected to their direct neighboring nodes. Repetition of this process propagates a voltage throughout the commensurate mesh of nodes analogous to an EM field in free space. Material properties are included through the use of transmission-line stubs of length $\Delta l/2$, which maintains the time synchronicity of the scatter-connect algorithm [6]. This explanation of TLM is sufficient for the purpose of this paper. Further details can be found in [6] and [9].

2. IBIS-TLM Formulation

The interface between IBIS and TLM is shown in Figure 2a. The short 1D TLM section represents the package parasitics and die capacitance. The 3D TLM is the field TLM that will be used for the primary simulation. The interface between the 1D circuit TLM and the 3D field TLM is linear and can hence be solved using the methods discussed in [6]. This is not discussed here due to space limitations.

The interface between the IBIS and 1D TLM is complicated by the non-linear nature of the IBIS termination. In Figure 2b two Thevenin circuits are shown, which represent the equivalent circuit at the interface for the driver and load IBIS configurations respectively. The current i is determined from the IBIS lookup tables [8], using ${}_kV$, the total voltage at TLM time-step k. ${}_kV^r$ is the TLM scattered voltage incident upon the IBIS boundary at time-step k. To find ${}_kV^i$ (the incident voltage to the TLM node from the IBIS boundary), it is necessary to solve for ${}_kV$. At the driver the conventional Newton-Raphson routine is applied to solve the non-linear loop equation

$$2_k V^r - iZ_{C\_comp} - {}_k V_{src} - {}_k V = 0\,, \tag{1}$$

where the incident voltage is then

$${}_k V^i = {}_k V - {}_k V^r + {}_k V_{src}\,. \tag{2}$$

${}_k V_{src}$ is the source voltage from the IBIS driver. The load termination is solved in the same manner, yet the V_{src} term is no longer present. Successive repetition of Eqns.1-2 for each TLM time-step k solves the non-linear IBIS condition at the boundary. It is a simple matter to interface the IBIS termination to multiple 3D TLM field nodes. The incident voltage for each TLM node is solved for in the same manner as the voltage across a stub added to a shunt TLM node [6], albeit, with the computation at the boundary rather than the node centre.

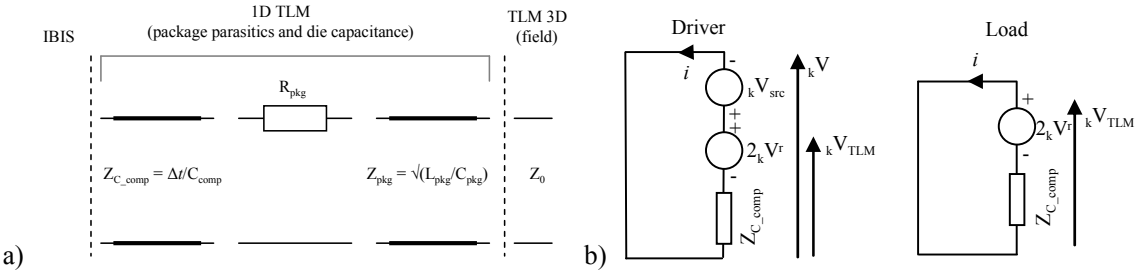


Figure 2 – a) IBIS buffer parasitics modeled using 1D TLM and b) Thevenin equivalent circuit at the non-linear interface between IBIS and the 1D circuit TLM.

3. Results

In this section we use a test structure that will demonstrate an IBIS embedded buffer in TLM. In Figure 3 the structure is shown. Two parallel microstrip tracks of height 0.4mm and width 0.8mm (50Ω) are placed with a separation of 2.8mm, a further two are placed with a separation of 7.2mm. The output (driver) of two 74LVC1G00 NAND gates, and input (load) are connected to the driver and load tracks of each set respectively. The entire PCB model is placed at the bottom of a metal box enclosure of height 29.2mm, length 140mm and width 101.2mm. For the purpose of this simulation the second input of each NAND is assumed to be logic 1. Since the IBIS buffers for each port of the NAND gate are independent, it is only necessary to simulate the two ports in use.

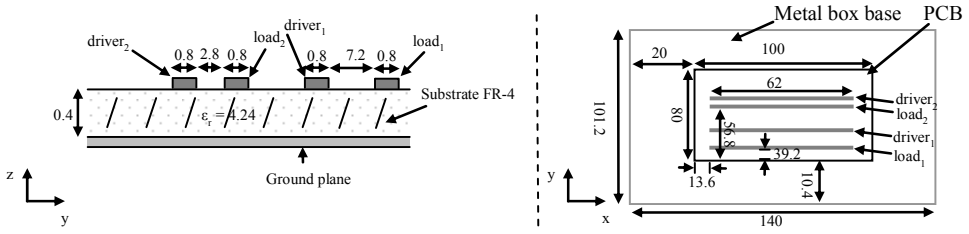
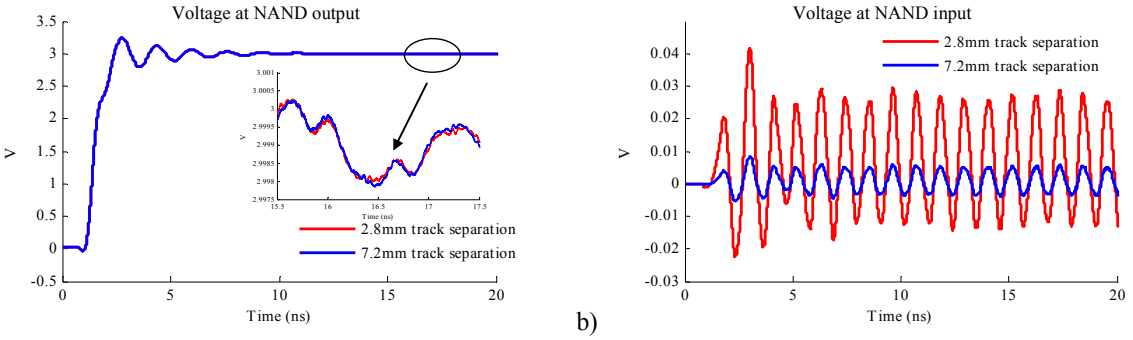


Figure 3 – Test structure. Two parallel microstrip tracks are simulated on FR4 substrate using TLM. The IBIS terminations model the IC buffer behavior at the driver and load. All measurements are in mm.

In Figure 4 the voltage at the output and input of the NAND is shown. In the TLM model the spatial sampling is $\Delta l = 0.4$mm while the temporal $\Delta t = 0.67$ps. $V_{cc} = 3$V. It is seen that the voltage at the output of the NAND gate is coupled to the input via the parallel tracks. The modeled structure allows the simulation of crosstalk between the two sets of tracks (one separated by 2.8mm and the other by 7.2mm) using the 3D TLM, while the IBIS interface simulates the complex NAND buffer behavior.



a) b)

Figure 4 – Voltage at a) output and b) input of NAND gate, simulated using IBIS buffers embedded into the 3D TLM field solver. $\Delta l = 0.4$mm, $\Delta t = 0.67$ps. The crosstalk is clearly visible at the input (load) IBIS buffer.

4. Conclusions

The paper has introduced the IBIS behavioral model and the TLM modeling method. It was shown that IBIS can be used within TLM to model complex device characteristics, while the TLM method can be used to model field interactions. The example of crosstalk between two microstrip tracks was demonstrated using the IBIS-TLM model. Further work will expand on this approach to study coupling situations where there is a risk of changes in logic state due to EMI.

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