Fast and Accurate Design Methodology for Millimeter-Wave Integrated Circuits

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Abstract

In this paper the design of integrated passive and active circuits in silicon by use of rigorous electromagnetic analysis. A broadband directional coupler has been designed with large bandwidth at 110 GHz center frequency and measured from 20 to 140 GHz. The simulation is compared to measurement showing very good agreement. A VCO has been designed at 116 GHz center frequency. The measurement of the center frequency is within 1% of simulation. The design methodology for a 240-GHz power detector also is given showing the design of a L-type matching network.

1 Introduction

The technological advancement of silicon technology, both SiGe HBT or CMOS has powered the increase in operation frequency. Integrated millimeter-wave active and passive circuits as well as fully integrated systems from 30 to 280 GHz have been reported to date [1–6]. All passive devices can be regarded as elements of distributed nature, where wave propagation has to be taken into account. Approaching the top end of the millimeter wave range, every single layout element has to be considered in simulation.

The successful design of integrated circuits is based on two major steps: precise modeling of active circuit elements, e.g. transistors or diodes, and accurate estimation and extraction of passive circuit elements, e.g. inductors or transmission lines. The former has to be provided by the manufacturer by fabricating test circuits and extracting device parameters. The latter has to be performed by the designer including different steps. The response of passive elements has to be extracted by an electromagnetic (EM) analysis, a model has to be created, and a cosimulation with the active circuit models has to be performed.

The EM analysis can be performed by quasi-static field solvers like VeloceRaptor™ or ASITIC, as normally done at RF frequencies up to 30 GHz. The latter software has been successfully used for a 160-GHz design [2]. Full 3D EM solvers can be used for the design like HFSS™ as used for a quadrature receiver in [3]. The simulation cannot be used for full-chip extraction. due to high memory usage. Planar 3D solvers like Agilent Momentum as used in [4] or SONNET® are feasible, with sufficient accuracy and fast optimization cycles. Other design methodologies for narrowband design are based on parameterizable transmission line models without post-layout extraction stage, as shown in [5].

2 Design of a broadside coupled lines directional coupler

A broadside coupled line directional coupler was designed to study the accuracy of the simulation software for a broad bandwidth and vertical coupling between metal structures. A 3D plot of the layout (left) and chipmicrographs (right) of the coupler are shown in Fig. 1. The coupler is a backward coupling structure with quarterwave length at 110 GHz and occupies an area of 95x160 µm^2. The devices has been fabricated in a 250-nm SiGe BiCMOS technology from IHP. A simplified deembedding methodology has been used with only one symmetric THRU deembedding structure [7]. The measurement has been performed by an Agilent 8150XF vector network analyzer from 20 to 110 GHz and from 90 to 140 GHz with a R&S ZVB with external frequency converters. The magnitude of the S-Parameters (left) and the phase difference (right) of the couplers can be found in Fig. 2. A very good agreement between simulation and measurement with only

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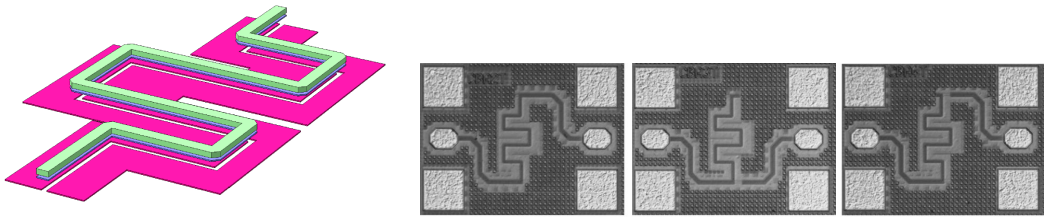

Figure 1: Layer stack (left) and simplified layout (right) of the broadside coupled directional coupler.

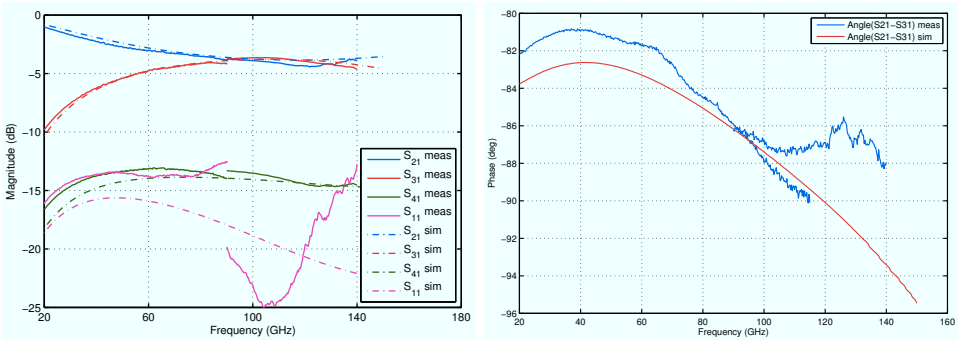

Figure 2: Comparison of S-Parameter measurement and simulation of the directional coupler.

a minor step for the transmission measurements can be found. The measurement of the reflection coefficient however shows a major step and a large difference between the two measurements and between measurement and simulation. This however can be accounted to the calibration of the network analyzer. The first phase measurement from 20 to 110 GHz matches the simulation well with maximum error of 2° and below 0.5° from 80 to 110 GHz. The second measurement shows a different behavior with high noise and spikes and a rather constant phase difference. This emphasizes the error in calibration for the measurement with the frequency extension.

3 Design of a 116-GHz VCO

Another millimeter-wave circuit where high precision in simulation is required is the design of an integrated oscillator. At high frequencies, a push-push oscillator based on the modified Colpitts oscillator, as shown in Fig. 3, is often used [1]. However, a high accuracy in simulation is also necessary for all other types of oscillators. The tank is formed at the base of the transistors by the transmission line L_b, the capacitors C_1, C_2, and the parasitic capacitance C_{BE} of the transistors. The electrical length of the transmission line of the tank has to be carefully designed, as an imprecise model directly results in a change of the oscillation frequency. The oscillator only shows a small tuning range, as no dedicated varactor is available. The design methodology is based on five steps: 1. simulation with simple passive element models, 2. Layout of the circuit, 3. EM analysis and optimization of passive elements, 4. generation of broadband SPICE or S-parameter models, 5. simulation of the circuit with all elements. For the first simulation step simple physical models are used, for example a pi-model for an inductor or a RLGC model for a transmission line. These models do not account for bends, crossings, or vias and are used to estimate overall circuit performance and the values for the passive elements (inductance, length, quality factor, etc.). The VCO has been designed and fabricated in a 130-nm BiCMOS process from IHP. It occupies an area of 800x550 µm^2 and has a current consumption of 25 mA (with an additional 20 mA for a frequency divider) from a 3.3-V power supply. The tuning range and the phase noise of the VCO have been measured at the divider output with a R&S FSUP26 signal source analyzer. The phase noise of the VCO is measured as -86 dBc/Hz at 1 MHz offset. The measurement is within 1 dB of the simulated value. The measured and simulated output frequency (middle) and

output power (right) of the VCO can be found in Fig. 3. The output frequency at a tuning voltage of 0 V is only 1 GHz smaller than simulated. This is a simulation accuracy for the output frequency of less than 1%, which verifies the precision of the active and passive simulation models. The simulated tuning range of the oscillator has not been achieved, as the varactor shows a smaller capacitance variation as expected. The output power is approx. 1 dB larger than expected, which can be attributed to the transistor models.

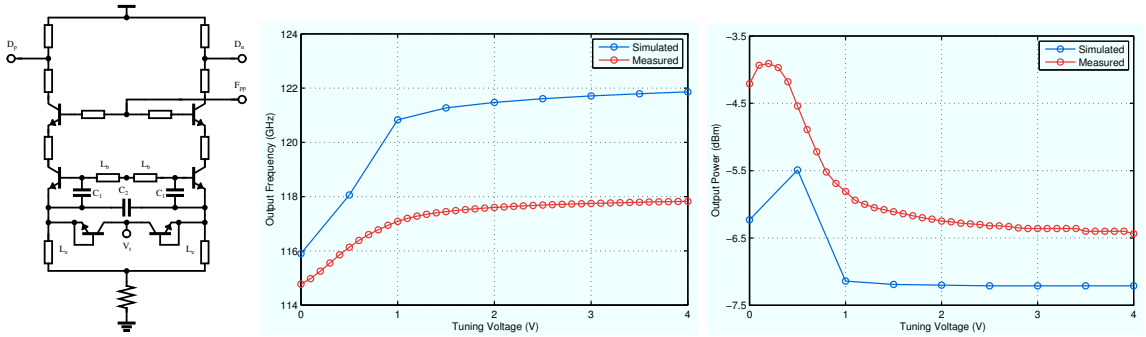

Figure 3: Schematic (left) and comparison of simulation and measurement of output frequency (middle) and output power (right) of the fabricated 116-GHz push-push VCO.

4 Design methodology for a 240-GHz power detector

Increasing the operating frequency of integrated circuits beyond 200 GHz exacerbates the design and simulation. Every simple basic structure has to be taken into account as it operates as a microwave element rather than a simple electrical connection. A 240-GHz Schottky power detector has been designed, but the design principles can be used for any other basic circuit block. The circuit of interest is shown in Fig. 4,

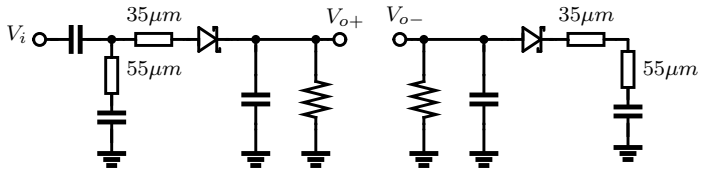

Figure 4: Schematic of the Schottky power detector for 240 GHz operation with simple L-match.

which includes a Schottky diode with transmission line input matching network and a reference path. The diodes are biased at 100 µA by a simple voltage generator. A quarterwave length for a 240-GHz signal in SiO_2 is approximately 156 µm, the transmission lines in the design are 55 µm and 35 µm, respectively. The design methodology for the circuit is based on the principle introduced in the last section. However, at

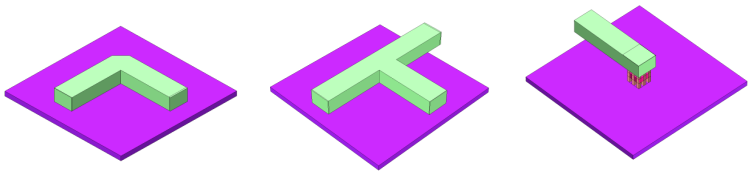

Figure 5: 3D view of modeled passive elements for subdivision of complex structures into basic elements.

these frequencies every discontinuity has to be considered and included in simulation. The effects of different types of discontinuities have been investigated and simulated. Three types of the most important elements

beyond transmission lines are shown in Fig. 5. Another via for connecting transistors to transmission lines is also included in the library. To simplify the design procedure, only a certain via shape is permitted. The discontinuities have been simulated and S-parameter and broadband spice models have been extracted to form library elements. To underline the previous claims, a 90° angle results in a phase error of +1.2° (-2.3 µm) and the shorted via in -3.6° (+6.0 µm). The latter reduces the drawn stub length by nearly 10%. The matching network can now be easily designed on schematic level without the use of time consuming electromagnetic (EM) analysis. The matching network for this circuit has been designed in the proposed way and compared to a full EM analysis. The difference for S21 is only -53 dB magnitude and 0.5°, which states the validity of the approach.

5 Conclusion

We have shown in the preceding sections that with 3D planar electromagnetic simulation software a high degree of accuracy can be achieved for the design of integrated millimeter-wave circuits in silicon technologies. This is exemplified by a broadband directional coupler measured from 20 to 140 GHz and a VCO at 116 GHz, both with good agreement between simulation and measurement. We also showed that the subdivision of passive structures results in a library of basic elements results in high accuracy and further speeds the design cycle.

Acknowledgment

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