Linearity and Efficiency Performance of a Modified Envelope Elimination and Restoration Transmitter Architecture

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Abstract

In this paper, linearity and efficiency degrading mechanisms within envelope elimination and restoration transmitters are explained and demonstrated through simulations. A modified transmitter architecture is proposed to overcome these shortcomings. The proposed and conventional envelope elimination and restoration transmitter performances are compared and it is demonstrated that the proposed architecture provides better linearity and efficiency.

1. Introduction

The envelope elimination and restoration (EER) technique was proposed by L. R. Kahn in 1952 as a method for implementing efficient, high power single-side-band (SSB) transmitters and is also referred to as the Kahn method [1]. The block diagram representation of an EER transmitter is shown in Figure 1. A modulated RF signal is split into its polar components; amplitude (envelope) and phase (constant amplitude but phase modulated) signals, by an envelope detector and a limiter respectively. The limiter output is a constant envelope signal ($\phi(t)$) that can be amplified by a power efficient but very non-linear switching power amplifier (PA), ideally, without adding significant amplitude (AM/AM) and phase (AM/PM) distortion. The envelope information ($E(t)$) is restored at the output by modulating the supply voltage (V_{dd}) of the amplifier, where the modulating signal is derived from the envelope detector. In theory, a well-saturated amplifier can be approximated as an RF voltage generator whose amplitude is proportional to the dc-supply voltage, i.e. $V_{out} \alpha V_{dd}^2$.

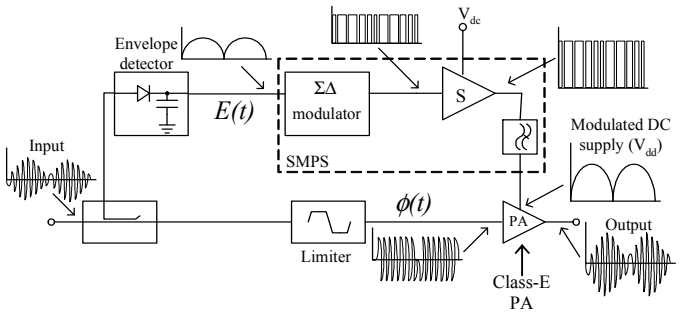

Figure 1: A conventional envelope elimination and restoration transmitter.

By using a double envelope-feedback loop with EER, up to 56% transmitter efficiency has been achieved [1]. A monolithic CMOS implementation of the technique has been presented [2] that improved the overall efficiency of the transmitter from 36% to 49%. It has been shown in [3] that phase feedback EER architecture may achieve average power added efficiency (PAE) up to 70%, while satisfying the spectral mask of IEEE 802.11n WLAN system with only a small degradation in link level performance.

In this paper, the performance limiting factors of EER are explained and a novel transmitter architecture is proposed that may facilitate to achieve higher linearity and efficiency than those of the conventional EER architecture.

2. Over-sampling, Envelope Bandwidth and Delay Matching Requirements

The power added efficiency (PAE) of an EER transmitter depends on the efficiency of the PA, envelope signal path and losses through the other components (coupler, detectors, delay lines, etc.) in the system. The square-wave signals drive the switching type amplifiers in a more efficient mode of operation compared to sine-wave type input

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signals. For the switched mode power supply (SMPS) process to be highly efficient, 1-bit sigma-delta modulators (ΣΔ) are used to digitize the envelope. In ΣΔ-modulation the pulse density linearly varies with samples of the input signal, and the pulse duration is synchronized with the sampling frequency and kept fixed.

Usually for satisfactory linearity, a sampling rate at 10 times the RF bandwidth (B_{RF}) is chosen. High over-sampling rates represent the envelope with good accuracy and thus provide lower intermodulation distortion (IMD) from the EER transmitter. ΣΔ modulation generates strong IMD, thus a low-pass filter (LPF) is required at the output of the class-S modulator to suppress the out-of-band IMD products and the quantization noise generated by the ΣΔ modulator. The envelope filter bandwidth (B_E) should be at least twice the RF signal bandwidth ($B_E > 2B_{RF}$). The selection of this filter is a compromise between passing the infinite bandwidth envelope signal and rejecting the spurious components that are inherent in the ΣΔ modulation process. Another important factor degrading the linearity performance is the delay matching between the modulating supply voltage and constant envelope signal. The misalignment must not exceed one tenth of the inverse of the RF bandwidth ($\Delta t < 0.1/B_{RF}$) for 30dBc IM3 level [4]. The delay matching requirement is related to the bandwidth of the signal, i.e. wideband signals require more accurate delay match. According to Raab, the IMD introduced by the delay mismatch can be approximated by (1), which explains this relationship.

$$IMD \approx 2\pi\, B_{RF}^2 \Delta t^2 \tag{1}$$

3. Class-E Amplifier Behaviour

In switching amplifiers (class-E/F), the transistor operates as an on/off switch and the output load network shapes the output waveforms to prevent simultaneous high voltage and high current, which minimises the power dissipation in the transistor. A Class-E amplifier as shown in Figure 2 has been designed in EESof ADS by using a GaAs FET (MWT-773HP, MicroWave Technologies).

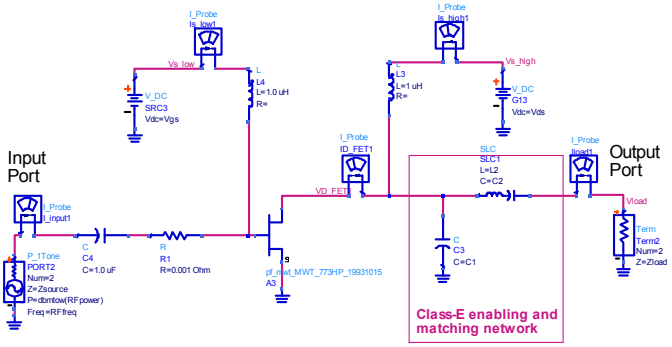

Figure 2: A class-E amplifier.

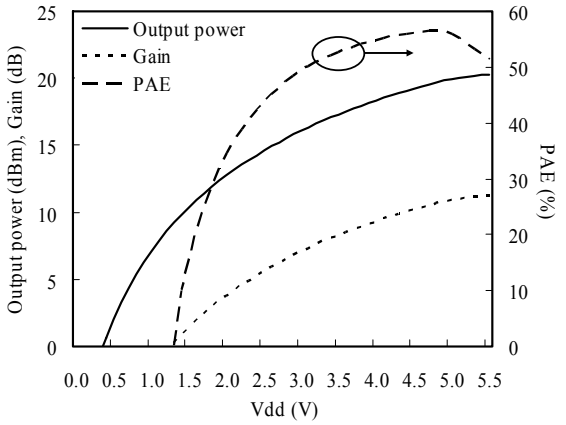

Figure 3: Output power, PAE and gain as a function of V_{dd}.

In order to investigate the effects of modulating the supply voltage of the amplifier, the drain supply voltage (V_{dd}) is swept from 0 to 5.5V. The output power, gain and PAE of the amplifier as a function of supply voltage is obtained, results are shown in Figure 3. The gain of the amplifier and thus the output signal power is changing

according to the supply voltage level. Indeed the envelope information can be restored by using this feature. PAE degradation is not large up to 2.5V, but degrades very quickly for the values below 2.5V, dropping to only 12% at 1.5V. This plot shows that, in terms of PAE, changing the supply voltage of a switching amplifier within a limited dynamic range, i.e. in our case from around 2.5 to 4.5 V is acceptable, but other V_{dd} values should be avoided. Setting a lower or a higher limit for maintaining the PAE at a reasonable level contradicts with the idea behind the EER technique since it will result in partial reconstruction of the envelope information, which means higher IMD levels.

4. Proposed Linear Transmitter Architecture

In this paper, it is proposed to digitize the envelope information and then use this pulse-train to convert the constant envelope RF signal to binary by using the switching PA as the modulating device as shown in Figure 4 [5]. This is equivalent to ΣΔ-modulating the RF output of the PA, but without needing extremely high sampling rate analog to digital converters (ADC). In other words, the class-E amplifier is driven with a constant envelope RF input signal and its output is a ΣΔ modulated signal at RF. A band-pass filter (BPF) at the output of the class-E amplifier is then used to constrain the current flow to the desired frequency which reconstructs the envelope at the transmitter output. Therefore, the supply voltage of the class-E amplifier is binary (either optimum V_{dd} or 0 V) and thus all the intermediate values of supply voltage between the optimum V_{dd} and 0 V are eliminated. This means alleviation of AM/AM and AM/PM introduced during envelope reconstruction.

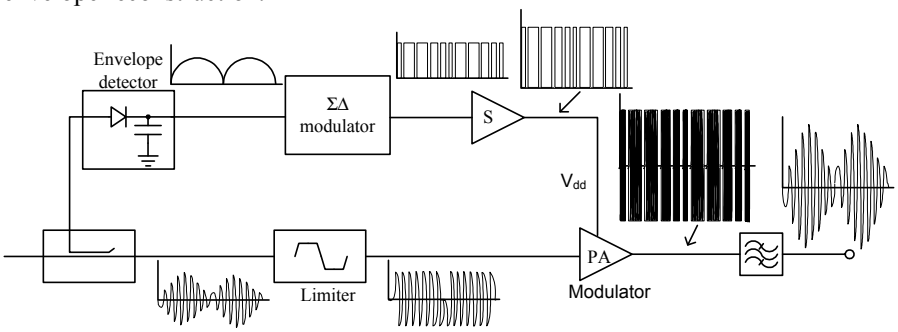

Figure 4: ΣΔ modulated supply voltage driven PA.

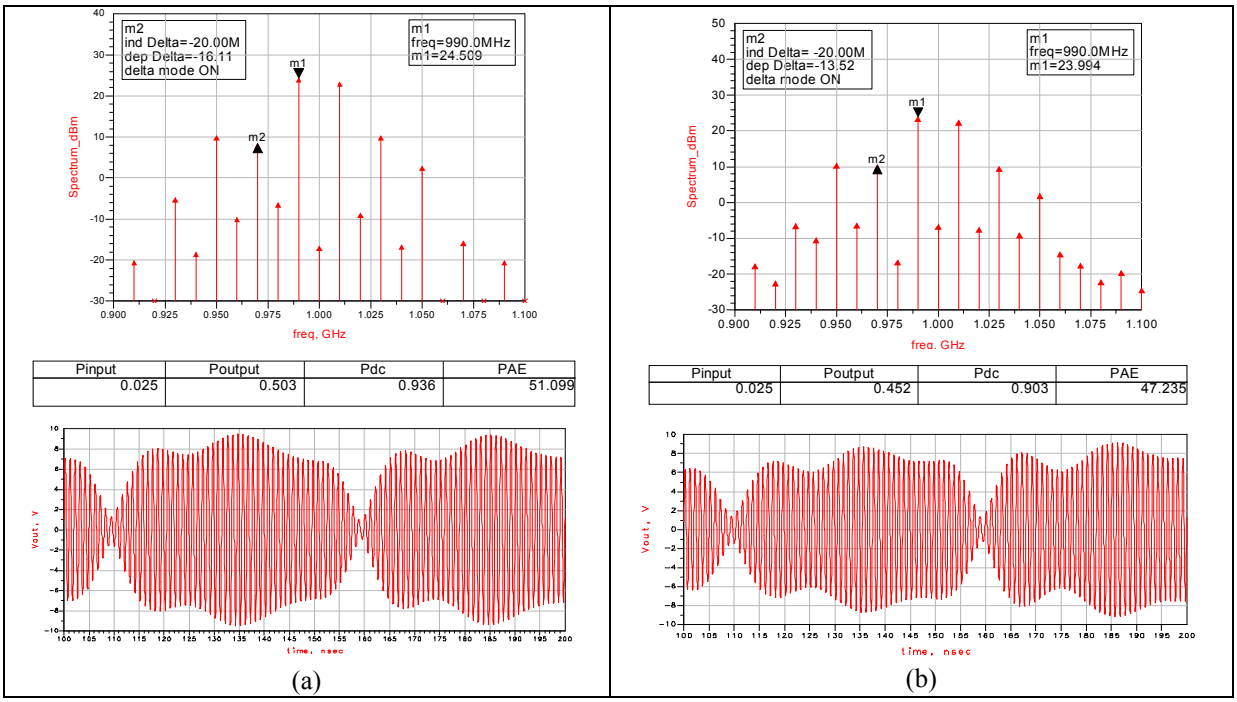

Figure 5: (a) ΣΔ modulated supply voltage driven EER architecture, (b) Conventional EER.

4.1 ΣΔ Modulated Supply Voltage Driven and Conventional EER Performances Compared

A first order ΣΔ-modulator with 1-bit ADC was constructed. The input of the modulator is the signal envelope and the output is the amplified ΣΔ-modulated signal which is used to modulate the supply voltage of the PA. The output of the ΣΔ-modulator is amplified so that the maximum peak is at 5 V where the class-E amplifier delivers maximum PAE. The sampling rate used in the ΣΔ Modulator is 10 times the RF bandwidth. The novel architecture shown in Figure 4 and the conventional EER shown in Figure 1 are simulated with a 20MHz wide two-tone signal. The output spectrums, delivered PAE, output power and DC power consumption of both transmitters are shown in Figure 5. The novel architecture provides about 3 dB lower IM3 and 4% higher PAE than the conventional EER architecture.

5. Conclusion

The EER transmitter architecture has been investigated and the factors limiting its performance have been explained. Simulations have demonstrated the effects of changing the supply voltage of a class-E amplifier for the purpose of reconstructing the envelope. It has been shown that envelope reconstruction process reduces the average PAE and it introduces non-linearity to the EER transmitter. A novel EER architecture has been proposed where supply voltage is ΣΔ-modulated. It is shown by ADS simulations that that the novel architecture provides better PAE and linearity than conventional EER.

6. References

1. L. R. Kahn, Single-sideband transmission by envelope elimination and restoration, *In Proceedings of the IRE*, July 1952, Volume: 40, Pages: 803-806.

2. F. H. Raab, E. B. Sigmon, G. R. Myers and M. R. Jackson, L-band transmitter using Kahn EER technique, *IEEE Transactions on Microwave Theory and Techniques*, Dec 1998, Volume 46, no: 12 pt 2, Pages: 2220-2225.

3. D. Su and W. McFarland, IC for linearizing RF power amplifiers using envelope elimination and restoration, *In HP Laboratories Technical Report*, no: HPL-98-186, November 1998, Pages: 1-13.

4. T. Nesimoglu, S.C.J. Parker, K.A. Morris, J.P. Mcgeehan, The performance and efficiency of envelope elimination and restoration transmitters for future multiple-input multiple-output wireless local area networks, *IET Communications*, Volume 2, Issue 3, March 2008, Pages:473 – 483.

5. F. H. Raab, Intermodulation distortion in Kahn-technique transmitters, *IEEE Transactions on Microwave Theory and Techniques*, Vol: 44, no: 12, part 1, pp: 2273-2278, December 1996.

6. T. Nesimoglu and K. A. Morris, Signal processor for use with a power amplifier in a wireless circuit, *World Intellectual Property Organisation (WIPO) patent publication*, WO2007064007, A1 - 2007-06-07.