A MICROSTRIP AMPLIFIER DESIGN SUBJECT TO THE TRANSISTOR PERFORMANCE LIMITATIONS

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Abstract

This paper presents synthesis of the microstrip matching circuits to be used at the input and/or output ports of the low-noise transistor. In this synthesis, input matching circuit matches the given generator impedance to the optimum noise impedance of the transistor while the output matching circuit matches the receiver impedance to the load impedance of the transistor which provides the available maximum gain within the maximum potential bandwidth at the expense of the minimum mismatching at the input port. A worked example is given all the details.

1. Synthesis using the Performance Limitations of the transistor

In this work, microstrip matching circuits for the input and output ports of a low-noise microwave transistor are synthesized subject to the potential performance of the transistor. Since the amplifier is utilized for the first stage, the noise figure acts the dominant role at the noise of the whole system, however at the same time maximum transducer gain must be obtained within an available maximum operation bandwidth at the expense of a reasonable mismatching at the input port. For this purpose, the minimum noise figure at each operation frequency is taken as a target in the synthesis process, thus transistor must be driven by the optimum noise impedance Zs_{opt} at each operation frequency. The remaining problem is to determine load impedance Z_L to meet gain and bandwidth requirements. In [1], the proper load termination variation $Z_L(\omega)$ is worked out for the available maximum gain within the available widest bandwidth at the expense of reasonable mismatching at the input port. Thus, the source $Z_S(\omega)$ and load $Z_L(\omega)$ variations are obtained for the available minimum noise, maximum gain within the potential widest bandwidth at the expense of the potential smallest input mismatching.

2. Utilization of the Microstrip Lines as the Matching Element

In this work, microstrip lines are used as the distributed element in the matching circuits. Thus, the characteristic impedance Z_c (W,T,ε_r,H) and effective dielectric coefficient ε_{eff} (W,T,ε_r,H) functions for the quasi-static case are directly used in the whole synthesis process which are;

$$Z_c = \frac{\sqrt{\varepsilon_{eff}}\sqrt{\mu_0\varepsilon_0}}{C} = \sqrt{\frac{\mu_0\varepsilon_0}{\varepsilon_{eff}}}\frac{1}{C_a} \tag{2.1}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+\frac{12H}{W}\right)^{-\frac{1}{2}} + F(\varepsilon_r,H) - 0.217(\varepsilon_r-1)\frac{T}{\sqrt{WH}} \tag{2.2}$$

$$Ca = \frac{2\pi\varepsilon_0}{ln\left(\frac{8H}{W}+\frac{W}{4H}\right)} \qquad ,W/H \le 1 \tag{2.3}$$

$$Ca = \varepsilon_0\left[\frac{W}{H} + 1.393 + 0.667ln\left(\frac{W}{H}+1.444\right)\right] \qquad ,W/H > 1 \tag{2.4}$$

3. Matching Circuit Synthesis for the Input and Output Ports of the Transistor

Since the microstrip lines are assumed as the lossless and reciprocal lines, the only cause for the loss of the two-port matching circuits are due to the mismatching at the input or output port, which are the same. Thus the maximum power delivery conditions, in the other words, the unit gain conditions are sufficient to be satisfied to meet for the matching requirement. For this purpose, the unit gain is targetted as an objective at each operation frequency, thus the error function to be minimized can be expressed for the matching circuits as follows:

$$\epsilon = \sum_{i=1}^{n}[(1-G_T(\omega_i))^2] \tag{3.1}$$

Where n is the number of the sampling frequency. In the gain $G_T(\omega_i)$, i = 1, …. n evaluation, the matching two-port is terminated by the conjugate of the required source impedance $Zs_{opt}(\omega_i)$, i=1,….n, for the input port, while it is driven by the conjugate of the required load impedance $Z_L(\omega_i)$, i=1,….n for the output port. Besides, the $G_T(\omega_i)$ function is

expressed in terms of the Z_c and ε_{eff} given by the equations in (2.1-2.4) and in the optimization process, the substrate is chosen with its known parameters ε_r, H in the practice and the error function given in (2) is minimized with respect to the W and ℓ with a certain conductor thickness T. Π- T-, and L- types of circuits are synthesized as the matching networks for both the input and output ports and the T- types circuits are resulted with the most optimum results which are given here. The genetic algorithm is used as the optimization algorithm.

4. Worked Examples

In the worked examples, NE3511S02 is chosen as high technology low- noise transistor in the front-end amplifier synthesis and its minimum noise figure variation with respect to the frequency at the bias condition V_{DS}=2V, I_{DS}= 5mA is given in the Fig.1. Furthermore, the available maximum gain variations are given taking the mismatching at the input port as the parameter in the Fig.1 where the reasonable value for the input mismatching is chosen as ρ=0.3 since it provides the widest bandwidth. Besides, the obtained source $Zs_{opt}(\omega)$ and load $Z_L(\omega)$ termination variations are depicted in the Fig. 3. The gain, noise and input mismatching performances resulted from the synthesis process are taken place in Figs. 4,5,6 where at the same time, targeted performances and simulated performances obtained with synthesized parameters W, ℓ using an electrical circuit and full –wave electromagnetic simulators are also given. The W and ℓ values of the low-noise amplifier are shown in the Table I. The targeted and the synthesized source and load variation are depicted on the Smith chart in Fig.7.

5. Conclusion

In this work, a low-noise broad –band amplifier synthesis is carried out. First of all, it is a simple synthesis based on our previous works [1] and [2]. Here we used the microstrip lines on basic L- type of the configuration and applied its equations directly to the optimization process. The synthesis process can be considered as successful since it is verified by both the electrical circuit and full-wave electromagnetic simulators.

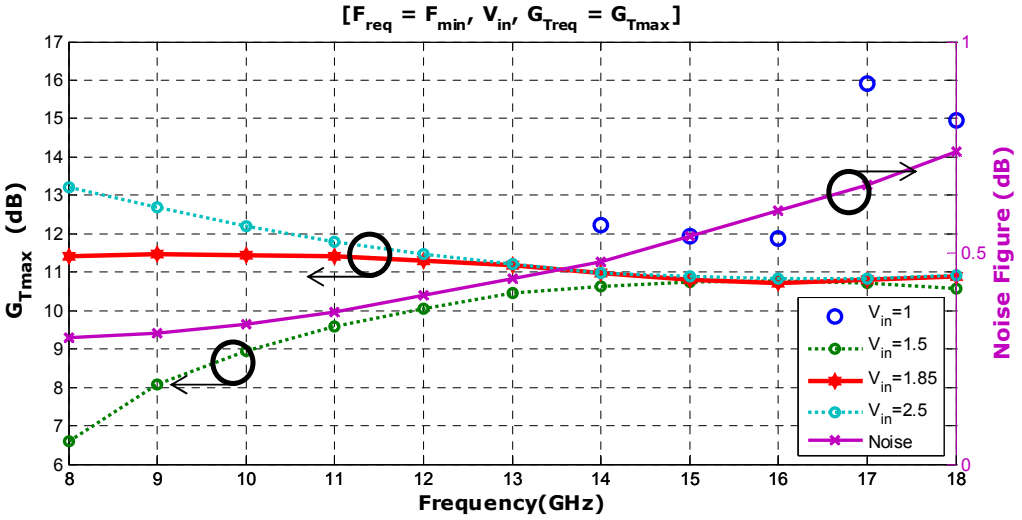

Fig.1 Minimum Noise Profile and the Maximum Gain Characteristics Constrained by the Minimum Noise and Input VSWR for NE3511S02 at V_{DS}=2V, I_{DS}=5mA.

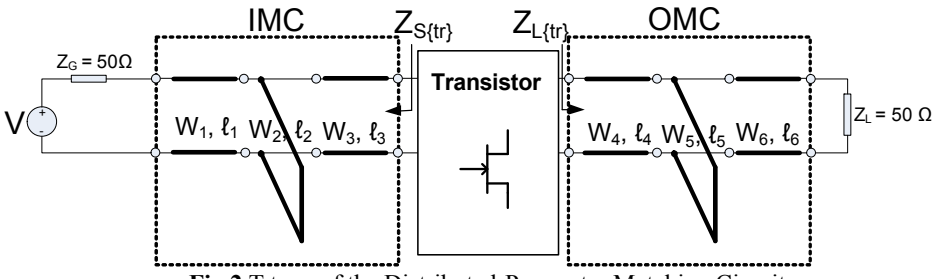

Fig.2 T type of the Distributed-Parameter Matching Circuit

TABLE – I Solution Space for the (T - T) IMC & OMC Elements

$W_1(mm)$	$W_2(mm)$	$W_3(mm)$	$W_4(mm)$	$W_5(mm)$	$W_6(mm)$	$\ell_1(mm)$	$\ell_2(mm)$	$\ell_3(mm)$	$\ell_4(mm)$	$\ell_5(mm)$	$\ell_6(mm)$
1.15	2.36	4.99	1.65	0.78	1.72	4.23	2.98	0.51	0.55	2.57	1.03

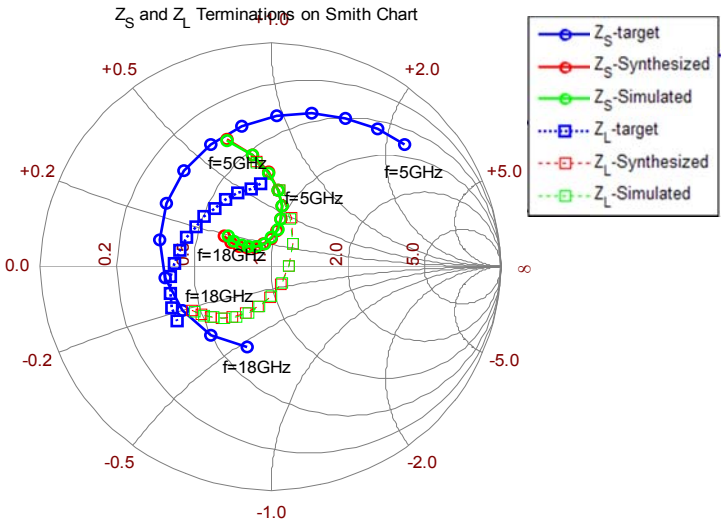

Fig.3 Source and Load Terminations of the constrained maximum gain by $\{F_{min}(f), V_{ireq} = 1.85\}$

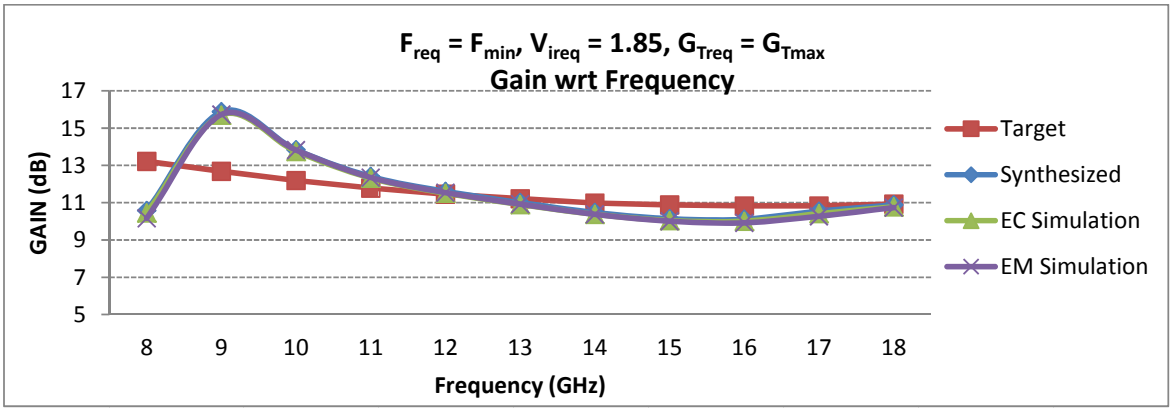

Fig.4 G_T (dB) variations with respect to the frequency for the Microwave Amplifier.

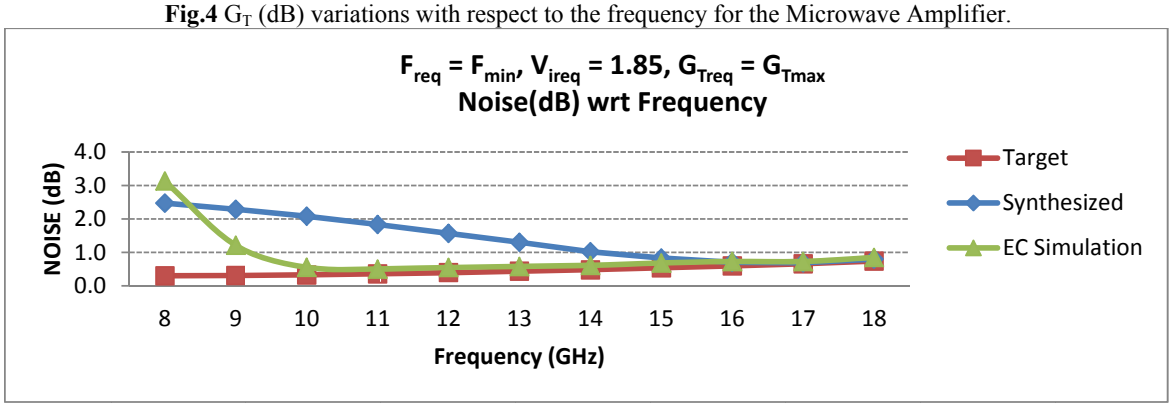

Fig.5 Noise (dB) variations with respect to the frequency for the Microwave Amplifier.

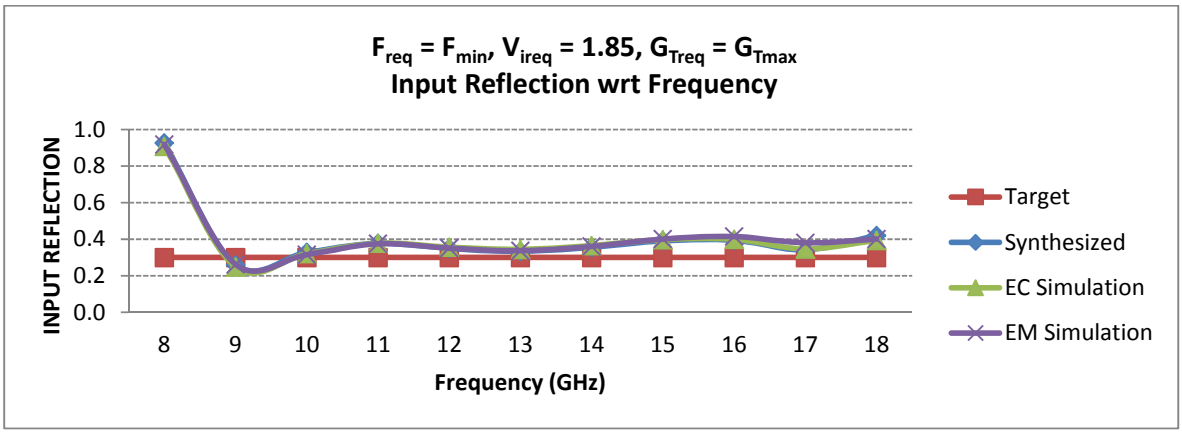

Fig.6 Input Reflection Coefficient variations with respect to the frequency for the Microwave Amplifier.

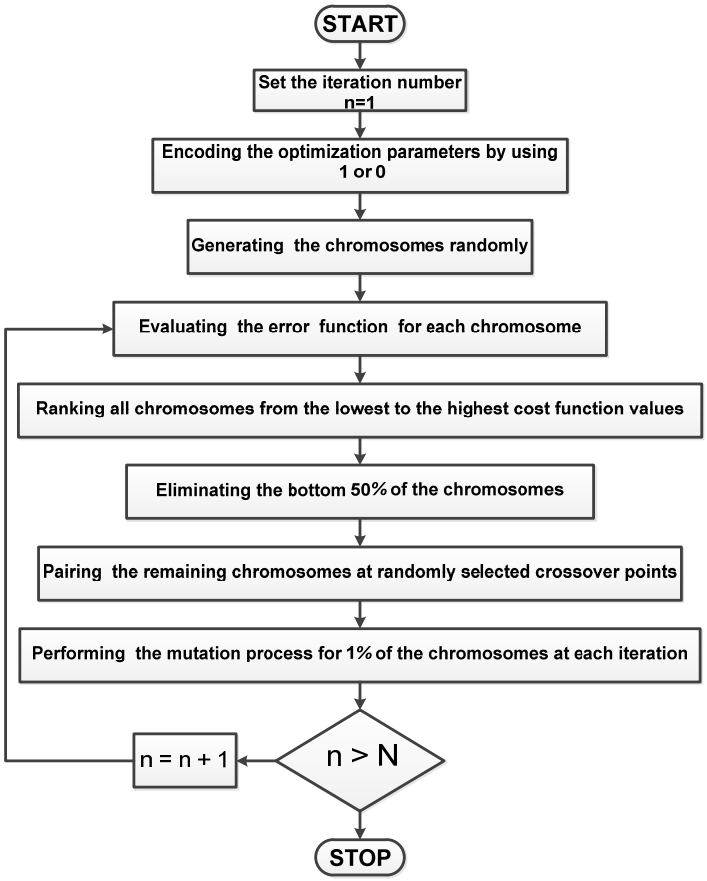

Fig. 7 The flow diagram of the genetic algorithm

6. References

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2. Gunes F., DemirelS., Ozkaya U., "A low-noise amplifier design using the performance limitations of a microwave transistor for the ultra-wideband applications", *International Journal of RF and Microwave Computer-Aided Engineering*. Volume: 20 Issue: 5 Pages: 535-545 Published: September 2010.