A Graphical Approach for the Optimization of SDR Channelizers

***Sufi Tabassum GUL*[1], *R. Mahesh*[2], *Christophe Moy*[1], *A. P. Vinod*[2], *Jacques Palicot*[1]**

[1] SUPELEC/IETR, Rennes Campus, CS47601 F-35576 Cesson-Sévigné, France
Email:<sufi.gul, christophe.moy, jacques.palicot >@supelec.fr

[2] School of Computer Engineering, Nanyang Technological University, Singapore
Email: <mahe0001, asvinod>@ntu.edu.sg

Abstract

The design of future multi-standard systems is very challenging. Flexible architectures exploiting processing commonalities of the different set of standards cohabiting in the device offer promising solutions. This paper presents a graphical approach for the optimization of multi-standard Software Defined Radio (SDR) systems. The potential of our approach for optimizing multi-standard SDR systems is highlighted by considering a realistic example of channelizers for SDR systems. In this paper we compare several channelization techniques. Computational complexity for multi-standards, multi-channels channelizers is presented that is to be included for the optimization procedure of flexible systems. Results show that Frequency Response Masking (FRM) technique is most suitable as compared to others.

1. Introduction

Software defined radio (SDR) is one of the most important topics of research, and indeed development, in the area of mobile and personal communications. SDR is viewed as an enabler of global roaming and as a unique platform for the rapid introduction of new services into existing live networks. It therefore promises mobile communication networks a major increase in flexibility and capability [1]. SDR is defined as a radio in which the receive digitization is performed at some stage downstream from the antenna, typically after wideband filtering, low noise amplification, and down conversion to a lower frequency in subsequent stages- with a reverse process occurring for the transmit digitization. Digital signal processing in flexible and reconfigurable functional blocks defines the characteristics of the radio [2].

Design of SDR systems is very challenging because it is very difficult to design a system that preserves most of the properties of the ideal software radio while being realizable with current-day technology. The possibilities to design software radio architectures range from "Velcro" approach to a "Very Fine Grain" approach [3]. The "Velcro" approach aims to support several communication standards through a few self-contained complex communication components; each exclusively dedicated to a given standard. On the contrary, "Very Fine Grain" approach is based on manipulating small size operators/components to support different standards.

The parameterization approach [4], in particular, aims at designing multi-standards systems made of entities (typically functions) whose operations can be modified by a simple parameter adjustment. This approach can be extended to lower level entities called common operators. Reference [5] proposes a procedure for optimal determination of common operators for multi-standards SDR. This is a very promising approach consisting of designing radio systems entities in a way that permits to take advantage of the programmable or at least reconfigurable capabilities of the underlying hardware of SDR systems. This approach is based on selecting the primitive operators (adders, multipliers, logic gates etc) and invoking these operators repeatedly to perform the various communication tasks as necessitated by the standards.

We consider an analytical approach for multi-standards SDR systems design based on a chosen graphical formalism, being developed in our laboratory. The exploration and selection of operators is based on a formal approach as the problem is given in an analytical form. This formalism is not detailed here but details can be found in [3]. An optimization process is then used to solve the formulated problem.

This study's main purposes are to present a mathematical model for the design of multi-standard SDR and to solve the optimization problem associated with it. In this paper we concentrate only on the channelizers which are

used in the SDR receivers for extracting individual channels from the digitized wideband input signal. To support multi-standards, the channelizer in an SDR should be able to reconfigure its hardware for the new mode of operation. The optimization procedure itself is not in the scope of this paper. In fact we address in this paper, the cost computations of filter banks (FBs) which are to be used in the optimization process.

The rest of this paper is organized as follows. First we present a review of channelization techniques. In the next section we describe our proposed methodology for designing flexible multi-standards systems. This step includes the drawing of a graph that represents design alternatives, the considerations of possible performance metrics, and the specification of appropriate cost parameters/constraints. Subsequently in order to apply it to the multi-standard channelizers, complexity costs of several alternatives of FBs are computed. Finally, we conclude our discussion addressing further interpretation of our results as well as limitations and future directions.

2. Review of Channelization Techniques

The most computationally intensive part of an SDR receiver is the channelizer since it operates at the highest sampling rate [1]. It extracts multiple narrowband channels from a wideband signal. Low complexity, high-speed and reconfigurable channelizers are required in the SDR receivers. The flexibility of an SDR depends on its capability to operate in multi-standard wireless communication environments. Thus the channelizer in an SDR should be able to reconfigure its hardware for the new mode of operation, while maintaining low power consumption and high speed. The channel per channel (CperC) approach is an efficient approach, if the number of channels to be received is less [6].

Efficient implementations of a channelizer using Discrete Fourier Transform filter banks (DFTFBs) are available in literature [6, 7]. The limitation of the DFTFB is that the channel filters have fixed equal bandwidths corresponding to the specification of a given standard. The limitations of DFTFBs for SDR receiver applications are as follows [6]:

1. DFTFBs cannot extract channels with different bandwidths. This is because DFTFBs are modulated filter banks with equal bandwidth of all band-pass filters. Therefore, for multi-mode receivers, distinct DFTFBs are required for each standard. Hence the complexity of a DFTFB channelizer increases linearly with the number of received standards.
2. Due to fixed channel stacking, the channels must be properly located for selecting them with the DFTFB. The channel stacking of a particular standard depends on the sample rate and the DFT size. To use the same DFTFB for another standard, the sample rate at the input of the DFTFB must be adapted accordingly. This requires additional sample rate converters (SRCs), which would increase the complexity and cost of DFTFBs.
3. If the channel bandwidth is very small compared to wideband input signal (extremely narrowband channels), the prototype filter must be highly selective resulting in very high-order filter. As the order of the filter increases, the complexity increases linearly. Also the DFT size needs to be increased.

An FB channelizer based on modified Goertzel algorithm was proposed in [6] as a solution of second and third problems of the DFTFB. But since the Goertzel FB (GFB) is also a type of modulated filter bank, the first problem remains unsolved. In [8], we have proposed the possibility of a reconfigurable filter based on the frequency response masking (FRM) technique [9]. In [10] a new reconfigurable filter bank based on the FRM approach is proposed. We have modified the original FRM approach to achieve following advantages: (1) incorporate reconfigurability at the filter level and architectural level, (2) improve the speed of filtering operation and (3) reduce the complexity.

3. Design of Multi-standard Flexible Systems

3.1. Common Operators Approach

Common operators (COs) approach involves the identification of an optimal level of granularity for operations (simpler than a self-contained module implementing a major communication task but more complex than gate level primitive operators such as AND, OR, etc.), in order to support several communication standards with a single architecture [3, 5]. For instance, [11] shows that many tasks of communications receiver can be implemented using the Fast Fourier Transform (FFT) especially for Orthogonal Frequency Division Multiplexing (OFDM) based

systems. In turn, the FFT can be implemented with butterflies. Thus, the butterfly can serve as a common operator for several FFT implementations of different orders.

3.2. Graph Model for SDR Systems

A multi-standard reconfigurable system can be represented in a graph with several layers. These layers depend upon the granularity level of considered processing elements (PEs). Our approach aims at providing the options to the designer, to select the most appropriate level of granularity as dictated by his needs. A great advantage is that at certain levels of granularity, the operators can be re-used several times, inside and between different standards and the result will be an improved design of SDR system. Each node of the graph represents an elementary functional PE. Each of these PEs can either be directly implemented in the system, or can represent a functionality obtained by invoking lower-level PEs. It is necessary to use a hypergraph instead of a simple graph in order to introduce two different types of dependencies between the nodes, as shown in Figure 1. Nodes dependencies occur between nodes of different levels. A node of a higher level, called a *parent node*, may have dependencies with nodes of underlying levels, called *descendant nodes*. An OR arc (direct arrow) means that only one of the descendant nodes is necessary to implement the parent node. An AND hyperarc ("inverted Y" connection) means that all descendant nodes are needed to implement the parent node. The roots of this graph, at the top level, represent the standards to be supported by the radio as shown in Figure 1.

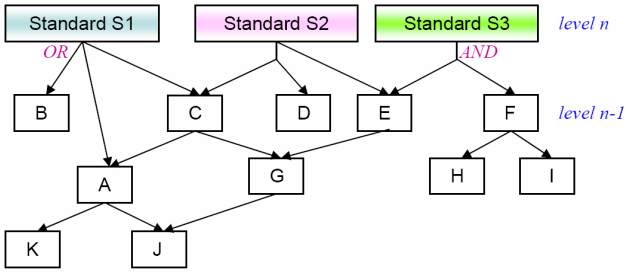

Figure 1: Global structure of graph for tri-standard SDR

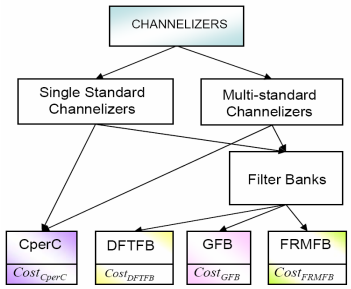

Figure 2: Channelizers for single/multi-standard SDR

The graph is originally planned to support the complete design of a multi-standard SDR system including all the signal processing elements it contains as in [12]. This graph can be translated into an optimization problem [3, 5]. Here we concentrate only on channelizers' branch. To implement channelizers for a single/multi-standard system we have different alternatives available as shown in Figure 2. In order to implement the optimization procedure of [5], we need to have the costs for each box of Figure 2. These costs can be e.g., installation cost, execution cost, area, number of gates etc. In our scenario we consider that the cost is proportional to the number of multiplication required per second. Costs, which are associated with each of the available alternatives as shown in the bottom level blocks of Figure 2, are computed in next section.

4. Cost Computation for Optimization of Channelizers

In this section, we present a quantitative comparison of different filter banks. Multiplication rate of a channelizer is defined as the total number of multiplications per sampling period for extracting N_I number of channels simultaneously. The multiplications in a channelizer involved with channel filtering are mainly considered. We can find multiplication rates of CperC approach, DFTFB, Goertzel FB and FRM in [6, 10]. Using these multiplication rates a comparison of different channelizers for multiple channels extraction with a fixed down-sampling rate in terms of sampling frequency f_s can be found in [10]. A comparison of multiplication complexity of multi-channel channelizers using sampling frequencies of various communication standards in terms of million of multiplications per second (MOMs) is given in Table 1. The results show that for single channel channelizer the CperC approach is the best e.g. for single channel IEEE 802.11b-DSS CperC costs 594 which is less as compared to costs of DFTFB (1100), GFB (1100) and FRM (638) respectively, as mentioned in Table 1. However, with the increase in number of channels, the less complex solution (in terms of MOMs) starts converging towards the FRMFB e.g., for 10 channels of WCDMA-FDD/TDD, FRMFB costs 2105 which is 8 times less than DFTFB/GFB and 40 times less than CperC approach. FRMFB is definitely advantageous for higher number of channels and this advantage can be seen even if we increase the number of channels from one to two as verified by the figures given in Table 1. This reinforces the interest for FRM technique for SDR. We can foresee from these computations that

FRMFB will be chosen by the optimization process for a multi-standard, multi-channel channelizer, but the price to pay for the lower arithmetic complexity in this approach is an overall longer delay.

Table 1: Costs of the channelizers in terms of million of multiplications per second (MOMs)

Standard	No. of Channels	Chip Rate	Sampling Frequency	$Cost_{CperC}$	$Cost_{DFTB}$	$Cost_{GFB}$	$Cost_{FRM\ FB}$
TD-SCDMA	1	1.28 Mcps	5.12 MHz	139	256	256	149
WCDMA-FDD/TDD	1	3.84 Mcps	15.36 MHz	415	768	768	446
IEEE 802.11b-DSS	1	11 Mcps	22 MHz	594	1100	1100	638
TD-SCDMA	2	1.28 Mcps	5.12 MHz	1009	994	999	415
WCDMA-FDD/TDD	2	3.84 Mcps	15.36 MHz	3026	2980	2996	1245
IEEE 802.11b-DSS	2	11 Mcps	22 MHz	4334	4268	4290	1782
TD-SCDMA	10	1.28 Mcps	5.12 MHz	27418	5469	5520	702
WCDMA-FDD/TDD	10	3.84 Mcps	15.36 MHz	82253	16405	16559	2105
IEEE 802.11b-DSS	10	11 Mcps	22 MHz	117810	23496	23716	3014

5. Conclusions and Future Directions

We have presented a channelizer approach and procedure that can aid a designer of a multi-standard SDR system to find an optimal architecture that balances cost and performance while observing pertinent multiplication rate constraints. The approach is illustrated through a particular example of multi-channel channelizer but one can find the generalized [12]. In addition, Binary Subexpression Elimination (BSE) [10] can be combined with FRM to further reduce the complexity. BSE can also act as common operator. In future we plan to integrate the channelizer branch in complete communication chain of multi-standard systems.

6. References

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