ESD coupling to interconnects

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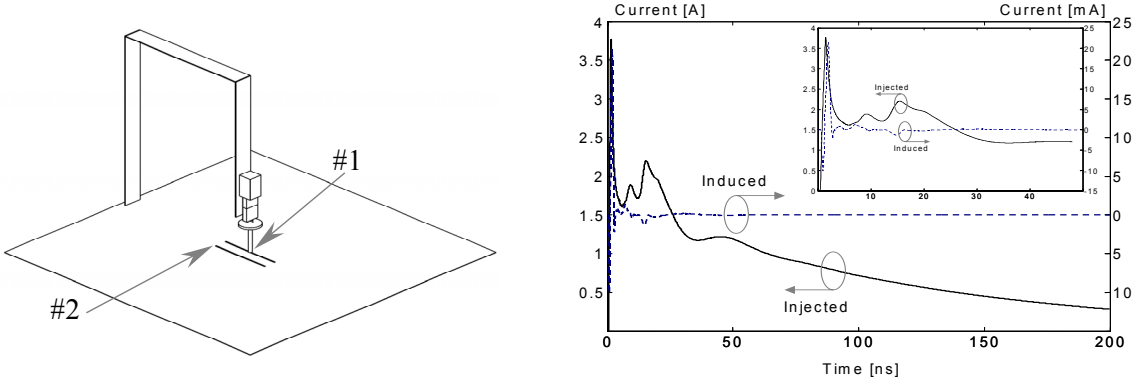
Currents and voltages injected and induced on high speed high populated printed circuit boards (PCBs) due to an electrostatic discharge (ESD) may produce damages and failures on fast logic devices. Thus, ESD generators are widely used for testing the robustness of electronic equipments which must comply with immunity standards [1-2]. In order to ensure a reproducibility of test results, the contact discharge mode is usually preferred to the air discharge one, since the influence of the arc on the discharge current is avoided. Anyway, a correct study of the susceptibility of a system claims an accurate simulation of the generator and the ground strap whose current distribution must be predicted to reproduce the fields which couple with the victim. The numerical simulation of ESD generators represents a tricky issue on which much work has been published [1-5]. Recently it has been suggested [4] a simplified model which allows to simulate the main features of an ESD generator with reasonable accuracy and computational effort, avoiding the necessity of a fully detailed model which makes use of time dependent materials [1]. Although some details are not correctly modelled, e.g. the electrostatic field due to the charging of the generator and the highest frequency content of the fields due to the pulse forming structure which is not included in the model, the magnetic radiated field is simulated with good accuracy as well as the time trend of the electric field, which only differs by an offset constant value [4].

In this paper it is conducted a study on the induced effects which the ESD event may produce on printed circuit boards. The simplified model proposed in [4,5] is used to simulate the discharges on classical microstripline configurations. A new simplified equivalent lumped circuits of the ESD generator is proposed [5]. As a preliminary study, the geometry depicted in Fig.1a has been simulated: the ESD generator discharges in the middle point of a microstripline (W = 140 mils, L = 20 cm) placed on a FR-4 substrate (ε_r = 3.38, h = 60 mils) at a distance of 4 cm from another equal microstripline. All the ends of the lines are matched on 50 Ω loads. The discharge current injected at port #1 and the induced current flowing at port #2 are reported in Fig. 1b, normalized to the discharge voltage of 1 kV. It is possible to note that the injected current is the classical current defined by a 1 ns rise time and 3,75 A/kV peak value for the contact discharge mode specified in IEC 61000-4-2. Moreover the induced current is in the order of several mA which can exceed the failure levels of several sensitive equipments.



(a) (b)

Figure 1 – (a) Prospective view of the ESD generator and PCB; (b) injected and induced currents respectively in port #1 and port #2.

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