High input impedance Front-End Circuit

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We present a front-end circuit for a sensor with a high input impedance. The voltage gain of this circuit is not critical (GV = 10 is sufficient), but other parameters like the input impedance, the input capacitance, the bandwidth and the power consumption are imperatives.
The necessary principal characteristics are reported below:

. high input impedance (higher than 30 M @ 1KHz)
· a low input capacitance (< 1.5 pF)
· low power consumption (about 30 mW)
· a bandwidth higher than 50 MHz
· an input noise lower than 30 nV/sqrt(Hz)@1MHz
· 2V of output dynamics
· the characteristics must be stable between +100 and -100°C
· the final circuit will have to be rad-hard (this will be carried out in the final version of the circuit)

Several tests for the design were tested (in particular a version containing transistors MOS) and finally the selected architecture is a bipolar structure for which the characteristics, after foundry, are very close to the desired values. The first stage comprises a whole of four sub-stages with high input impedance. Each sub-stage has also a high output impedance which is gradually decreased until being able to drive a gain stage which constitutes the second stage of the circuit. The last stage is an output stage which allows an adaptation of impedance on 600 Ω. The most delicate part of this circuit is the first stage. It is not indeed common to have a bipolar structure with so high input impedance. With the MOS structures, which we tested, it was not possible to obtain a low input capacitance, associated with a large bandwidth and low power consumption and low input noise. The first realization, intended to test the characteristics of the circuit, was carried out on silicon with a technology of 0.8 µm. The final structure will use the same architecture, but with a substrate allowing a rad-hard behaviour.