SiGe CMOS DIFFERENTIAL LOW NOISE AMPLIFIER 100MHz - 300MHz

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I. INTRODUCTION

In the next year, several projects of large radiotelescopes will be developed. These include LOFAR (LOw Frequency ARray), SKA (Square Kilometer Array) and FASR (Frequency Agile Solar Radiotelescope). LOFAR and SKA will be made up of thousands of antennae and consequently of thousands of front-end receivers. Each front-end is constituted of a LNA (Low Noise Amplifier), a filter, a mixer, …

In this perspective, we study a differential Low Noise Amplifier (LNA) realized in a CMOS 0.35µm technology from AustriaMicroSystems (AMS). A Silicon technology is chosen because of integration, manufacturing and cost advantages.

A bibliographical study has shown that the LNA's Noise Figure objectives, for instance in communication applications, are often of a few dB. However, radioastronomical received signals are very faint. So the required LNA must have a Noise Figure as low as possible (<1dB) and a 50 O input and output matching across the frequency band.

This paper will, first of all, describe a single-ended topology, based on a technique called "Thermal Noise Cancelling" [1], which allows to obtain simultaneously a low Noise Figure and a good matching. Then, in a second part, simulated and measured results of a differential circuit will be presented.

II. SINGLE-ENDED TOPOLOGY USING THE "THERMAL NOISE CANCELLING" TECHNIQUE

II. 1 Principle of the Technique

To apply this technique, a first stage with a transistor and a feedback resistor is used. The transistor in saturation is modelled as a voltage-controlled current source with transconductance gm. This source generates noise voltages with equal sign and signal voltages with opposite sign due to the feedback, at the input and output of the transistor. The technique consists in inserting a second stage, composed of two transistors in a push-pull configuration. The first one is connected at the input of the first stage and the second one at the output. This second stage performs summation of the two signals. Therefore, the noise voltages are cancelled and the signal voltages are constructively added. Fig.1a) represents the principle of this technique and Fig.1b) the final topology.

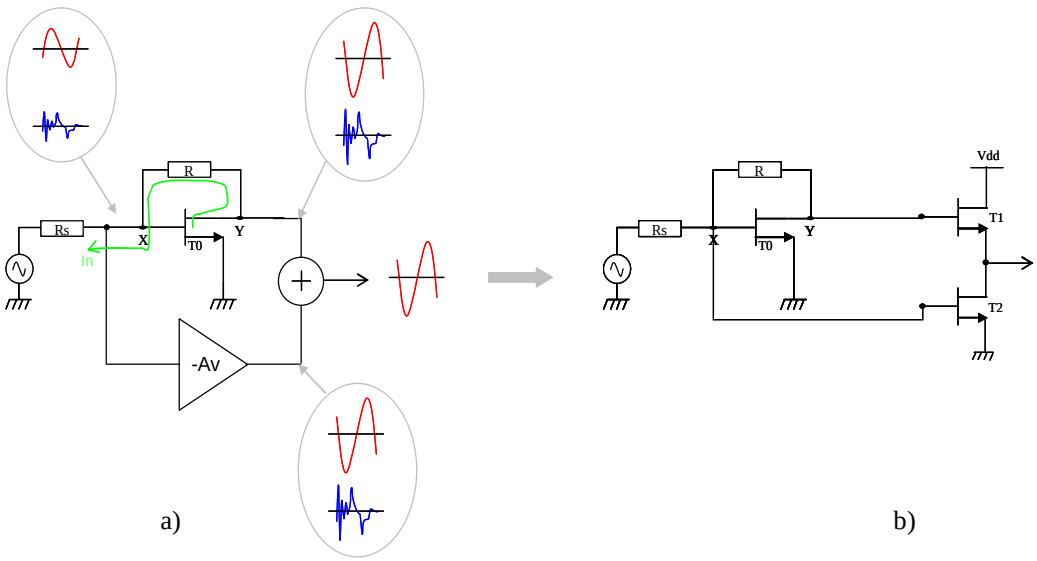

Fig. 1: Principle of the "Thermal Noise Cancelling" Technique

II. 2 Single-Ended Topology

We first study the single-ended topology presented in Fig.1a). Considering the equivalent low frequency small signals model of a transistor (voltage-controlled current source), we can calculate the value of the transconductance gm to have the desired adaptations. We then show that:

$$Zin=1/gm_0 \text{ and } Zout=1/gm_1$$

where Zin and Zout are the input and output impedances and gm_i is the transconductance of the transistor number i. We can obtain an input and output adaptation and a noise reduction if:

$$gm_0=1/Rs,\ gm_1=1/R0 \text{ and } gm_2=(1+\frac{R}{Rs})/R_0$$

where Rs is the source impedance at input port and R0 the charge impedance at output port.
The transmission coefficient S21 is equal to:

$$S_{21}=-\frac{R}{\sqrt{R_0.Rs}}$$

Ideally, T0 and T1 provide respectively the input and output adaptation, and T2 with R set the gain. The relationship between gm2 and R allows reducing the noise due to the drain current of T0. Simulations confirm this analysis, despite the fact that the effects of each parameters are not completely independent.

As the Noise Figure of a transistor decreases when its size increases, the first transistor T0 must be quite big in order to obtain a low Noise Figure. One of the parameters which limits the size of T0 is the power consumption. We choose a first stage current not in excess of 25 mA. So T0 is realized with 5 paralleled NMOS with 40 gates each. With a consumption of about 23 mA, this transistor achieves NF=0.7dB and S21=21dB. Then, we set the value of the resistor R. NF changes in opposite direction with respect to R. So, we choose a value of R=1.6kO, which is not too big and which does not add much noise. After that, we size T2, providing a slight NF decrease and helping to obtain input matching. As the size of T2 increases, the NF improves but the input becomes mismatched. To have simultaneously a quite small NF and a matched input, a trade-off is to use 3 paralleled transistors with 40 gates each. Finally, we size T1 (1 transistor with 12 gates) in order to reach a good output matching without degrading the other performances.

With ideal polarisation (0.8V on the gate of T0 and T2, 3V on the drain of T0 and T1), we obtain the results shown in Fig. 2.

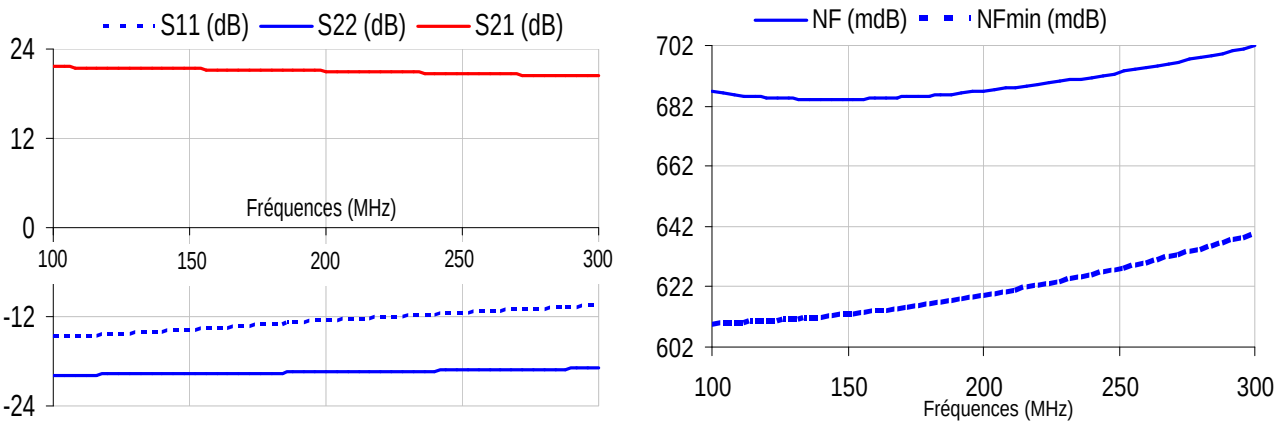

Fig. 2: [S] parameters and Noise Figure of the single-ended LNA

A NF lower than 1dB and good input and output matching are reached. Moreover the gain is about 21 dB and its in-band variation is less than 2 dB. The input 1dB compression point -14.7 dBm and the power consumption is 105mW, which is quite high. The circuit is stable in the operating frequency band, but not unconditionally stable, which can be a problem.

III. DIFFERENTIAL LNA

III. 1 Schematic and Layout

The circuit described in the preceding section is then transformed to be differential. Active loads with PMOS transistors are used for bias. These active loads are of great importance. Firstly, they have an effect on the input matching, leading to cascade 3 PMOS transistors in order to obtain the desired input impedance. As a consequence, T0 drain voltage is no more 3.3V, but 1.55V. Secondly, all the bias must be linked together. The Monte-Carlo simulations show that keeping the bias independent will dramatically increase the risk that the circuit does not achieve the desired performances. Linking the bias together allows to equalize voltages in the 2 differential branches, giving low sensitivity to process variations, confirmed by Monte-Carlo analysis. A current source is then added, limiting the power consumption to 24 mA for the entire circuit and providing a non zero impedance path to ground, needed to ensure that the circuit is fully differential. Finally, all the transistors have to be resized to allow for the lower current.

Due to the low frequency band, no coupling capacitors are integrated in the circuit. The schematic without the bias and the layout of this circuit are presented in Fig. 3.

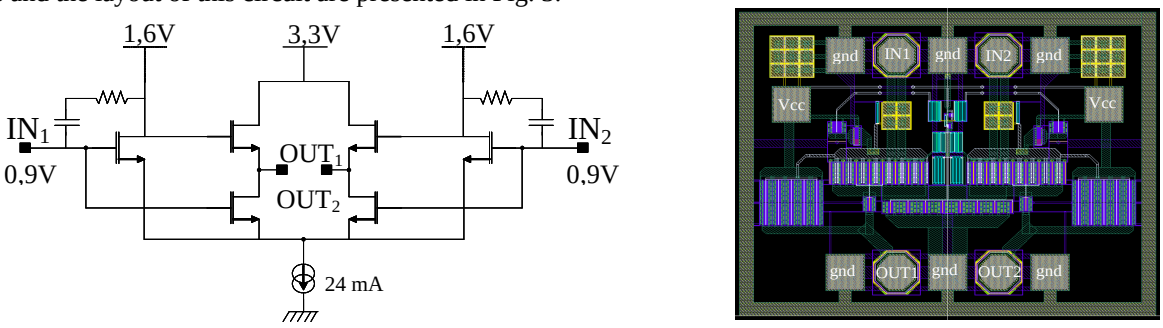

Fig. 3: Simplified differential LNA schematic and his layout (1mm²)

III.2 Simulated Results

Two schematics are used for the simulations. In the first one, baluns are added at the input and output ports. This configuration allows to simulate the Noise Figure. The other one is a 4-port network, so that the mixed-mode [S] parameters can be calculated.

Mixed-mode [S] parameters are a set of 16 parameters, used to describe a differential network. The first two sets describe differential to differential mode (Sdd11, Sdd12, Sdd21, Sdd22) and common to common mode (Scc11, Scc12, Scc21, Scc22). The two other sets describe conversion mode, that is to say, differential to common mode (Scd11, Scd12, Scd21, Scd22) and common to differential mode (Sdc11, Sdc12, Sdc21, Sdc22). Each parameter is expressed in function of the 2-port [S] parameters. An ideal differential circuit has neither conversion mode, nor common mode. We define the quality of a differential circuit by a quantity called CMRR (Common Mode Rejection Ratio), which is defined as follow:

$$CMRR = Sdd21 - Scc21$$

where Sdd21 and Scc21 are expressed in dB. Fig. 4 shows the simulation results of the differential LNA.

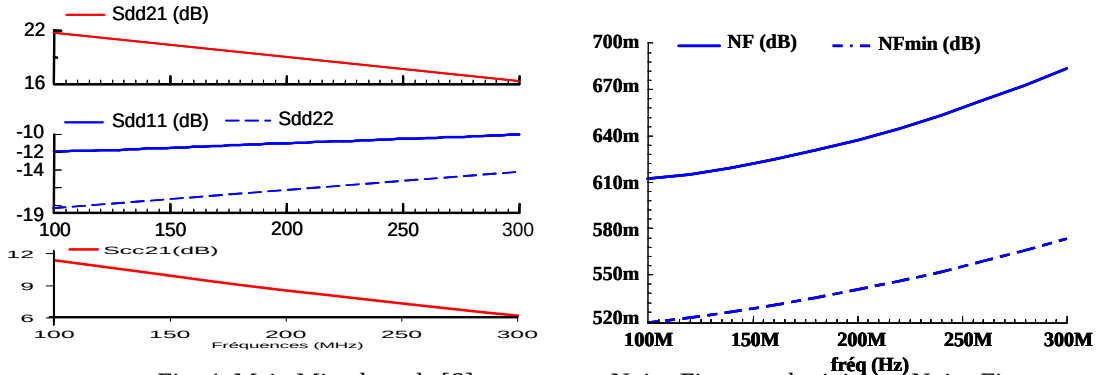

Fig. 4: Main Mixed-mode [S] parameters, Noise Figure and minimum Noise Figure

We can note that NF, input and output matching are close to the ones obtained for the single-ended topology, but the gain has a large variation in the operating band. This variation becomes larger, when the size of T0 is increased to optimize the NF. The circuit is unconditionally stable and its power consumption is about 80 mW (20 mW less than the single-ended topology). The CMRR is about 10 dB, which is quite a good value. As the second stage consumption is very small, that is necessary to reach the output matching, the circuit has not a good linearity (input 1dB compression point of -20dB).

III. 3 Measured Results

Measurements are performed in collaboration between AMARC (Axe de Micro-électronique Appliquée en Région Centre) and IRCOM (Institut de Recherches en Communications Optiques et Microondes - Limoges University). The on-chip measurements have been performed with a Differential Vectorial Network Analyser. As we have no available baluns, Noise Figure has not been measured yet. Fig. 5 shows the main measured mixed-mode [S] parameters.

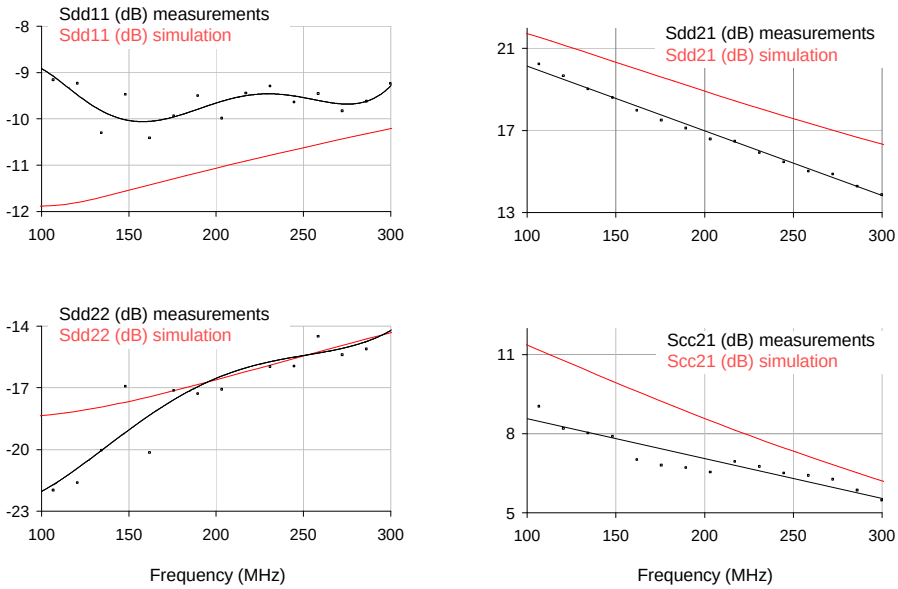

Fig. 5: Main measured mixed-mode [S] parameters

We can observe a quite good agreement between the simulated and measured results. We have verified that there is not conversion mode (Sdcii and Scdii around -30dB). The measured CMRR is around 10 dB (same value than in simulation).

IV. CONCLUSION

We have realized a SiGe CMOS differential LNA in the frequency band 100 MHz – 300 MHz with the 0.35µm technology of AustriaMicroSystems. Measurements have shown a good agreement with simulations. However two main points remain to improve: the gain variation in the band and the linearity.

The prospect is now to adapt this topology in a wider frequency band (350MHz – 2GHz), which corresponds to the lower frequency part of the SKA radiotelescope working band.

[1] Federico Bruccoleri, Eric A. M. Klumperink, Member, IEEE, and Bram Nauta, Senior Member, IEEE, “Wide Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Cancelling”, *IEEE Journal of Solid-State Circuits*, Vol. 39, NO. 2, February 2004.