SiGe Bipolar Transistor Low Noise Amplifier 150MHz – 2GHz

S. Bosse[1], S. Barth[1], N. Dubouloz[1], B. Jarry[2], B. Barelaud[2], L.Billonnet[2]
[1]Station de Radioastronomie de Nançay USR C.N.R.S B704, 18330 Nançay
[2]IRCOM UMR C.N.R.S 6615, Université de Limoges, 87060 Limoges
[1]stephane.bosse@obs-nancay.fr, severin.barth@obs-nancay.fr, nicolas.dubouloz@obs-nancay.fr
[2]jarry@ircom.unilim.fr, barelaud@unilim.fr, gary@ircom.unilim.fr

I. Introduction

The importance of microelectronics in radioastronomy projects will increase in the next decade, particularly in the scope of the SKA (Square Kilometer Array), with its very large number of channels. Radio frequency (RF) Silicon Circuits manufactured using BiCMOS technologies exhibit better performances in term of mass production and low cost, as compared to their GaAs counterparts, especially since the emergence of SiGe for bipolar transistors [1]. So, Silicon technologies have to be considered seriously for emerging applications such as the SKA.

In this paper, design aspects of a wideband low noise amplifier are discussed for frequencies between 0.15 GHz and 2 GHz, using a SiGe 0.35 µm BiCMOS commercially available process from AMS (AustriaMicroSystems).

The work described hereafter has been made in collaboration between Nancay Radioastronomy Observatory and IRCOM (Institut de Recherche en Communications Optiques et Microondes, Limoges), with additional funding from the Center Region of France.

II. Bipolar transistor noise performance and input impedance matching

The transistor with the lowest noise figure available in this technology is used in a common-emitter configuration. Ideal bias is used (V_{be} = 0.8 V, V_{ce} = 1.2V). The source R_s and load R_L are equal to 50 Ω. Simultaneous 50 ohms input and output impedance matching together with as low a noise figure as possible are desired, without using a feedback resistor [2].

II.1. Bipolar transistor noise performance

We choose a small emitter length (4 µm). The simulated minimum noise figure (NF_{min}) is 0.57 dB at 0.15 GHz and below 0.71 dB from 0.15 to 2 GHz, while the simulated noise figure (NF) is about 6.2 dB on this frequency band.

We show that the optimal noise impedance (Z_{min}) to present at the input of n two port networks connected in parallel, is equal to the optimal noise impedance to present at the input of this single network divided by n (Fig. 1). Moreover, the minimum noise figure of n two port networks in parallel is equal to the minimum noise figure of this network (Fig. 1).

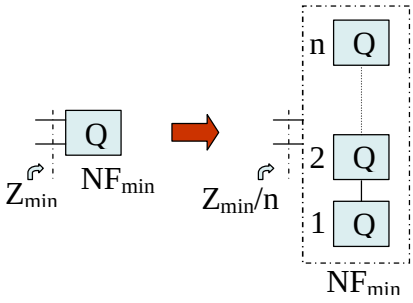

Fig. 1: NF_{min} of n two port networks connected in parallel

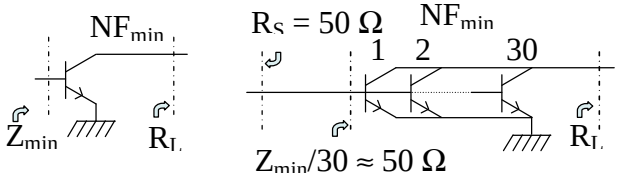

Fig. 2: Thirty NPN132h5 bipolar transistors connected in parallel

We choose thirty NPN bipolar transistors with a small emitter length (4 µm), connected in parallel in a common emitter configuration to obtain the optimal noise impedance around 50 Ω (Fig. 2). Then, NF is 0.68 dB at 0.15 GHz and below 0.86 dB from 0.15 to 2 GHz. These values are very close to the transistor minimum noise figure.

II.2. Bipolar transistor input and output impedance matching

Then, the real part of input impedance $\Re(Z_e)$ varies from 65 Ω to 7.5 Ω. This large variation is a problem to match the input impedance to 50 ohms. The imaginary part $\Im(Z_e)$ varies also strongly from -205 Ω to -17 Ω. We show that high load impedance improves the input impedance Z_e of these thirty bipolar transistors connected in parallel, in order to maintain a good matching (Fig. 3).

The imaginary part $\Im(Z_e)$ is nearly cancelled on this frequency band [0.15 – 2 GHz], and the real part variation of input impedance $\Delta\Re(Z_e)$ decreases clearly according to the frequency. The output of the thirty bipolar transistors is then cascaded with a low value capacitor C_1, realizing the needed high impedance without increasing the noise figure. Finally, a second stage must be added to match the output impedance to 50 ohms (Fig. 4).

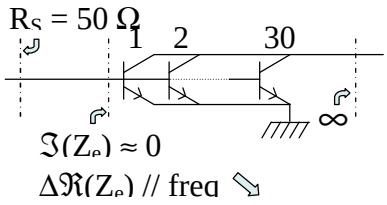

Fig. 3: 30 NPNh5 loaded by open circuit

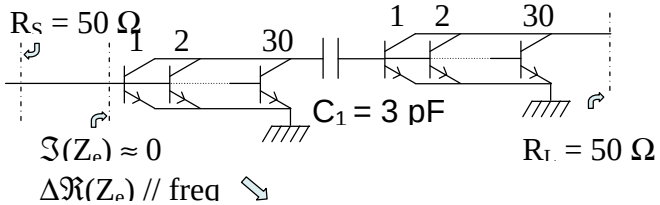

Fig. 4: Addition of C_1 capacity and of a second stage

$\Re(Z_e)$ is always low at 2 GHz, and its variation according to the frequency depends on C_1. It is shown that an inductor L_1 between emitter and ground can be used to improve input impedance [3] on a broad frequency band, still retaining a low noise figure. In spite of low frequencies between 0.15 GHz and 2 GHz and thanks to the large area of the 30 transistors in parallel, low value emitter degeneration inductor below 1nH can be used. Then, C1 and L_1 are a set of values that we have optimized for good matching. In the same way, an inductor L_2 between emitter of the second stage and ground improves the output impedance matching. L_1 and L_2 are realized with short microstrip lines.

In addition, in order to maintain a good matching in the lower part of the band, input and output coupling capacitors (C_L) must be of high value. For example, 20 pF capacitive value corresponds to -53 Ω at 0.15 GHz, what is too high. So, with the BiCMOS process used, a high capacitor value creates a high parasitic capacitor C_p with the substrate, significantly decreasing circuit performance. To evaluate this effect, two common emitter circuits have been manufactured, one including input and output coupling capacitors, and the other one with these capacitors removed.

Active loads with PMOS transistors are used to bias the transistors (Fig. 5). The topology obtained is presented in Fig. 6.

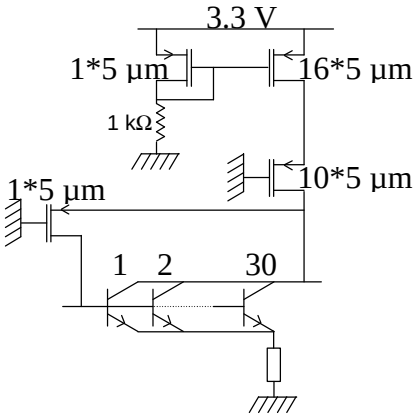

Fig. 5: Active load circuit

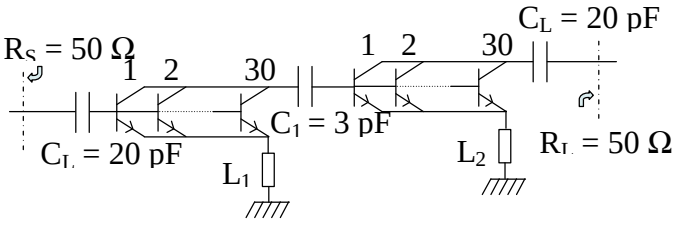

Fig. 6: Circuit topology

III. LAYOUT, SIMULATED AND MEASURED CIRCUITS.

Two layout are manufactured, one (circuit 1) without input and output coupling 20 pF capacitors (Fig. 7), and the other one (circuit 2) with these capacitors included (Fig. 8).

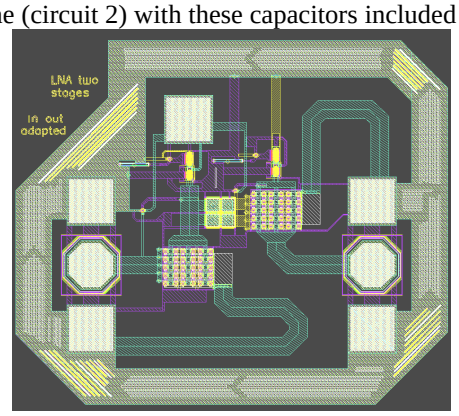

Fig. 7: Layout of circuit 1

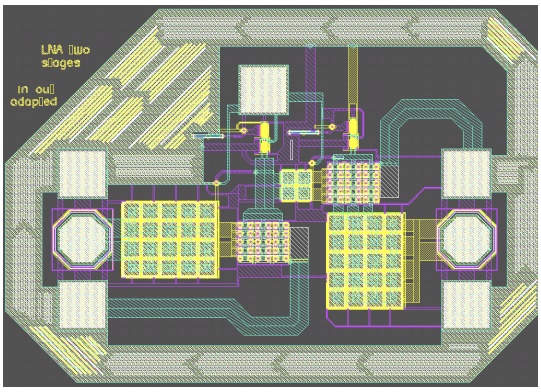

Fig. 8: Layout of circuit 2

III.1. Simulated circuits with Cadence 4.4.6

Simulated scattering parameters and noise figure (NF and NF_{min}) with and without C_L are respectively presented in Fig. 9 and Fig. 10.

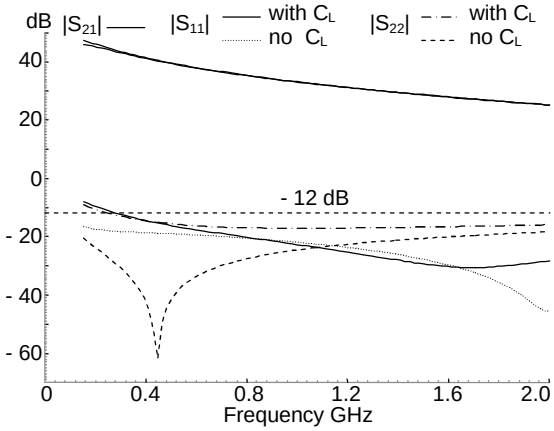

Fig. 9: [S] parameters with and without C_L

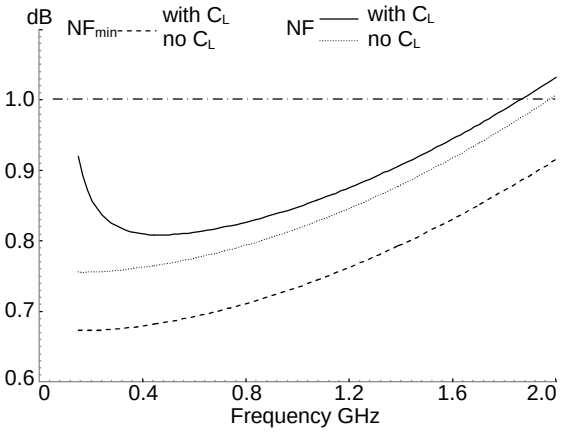

Fig. 10: Noise figure with and without C_L

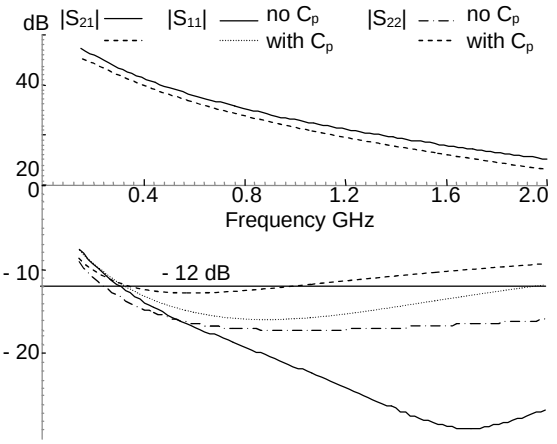

Fig. 11: [S] parameters with C_L, with and without C_p

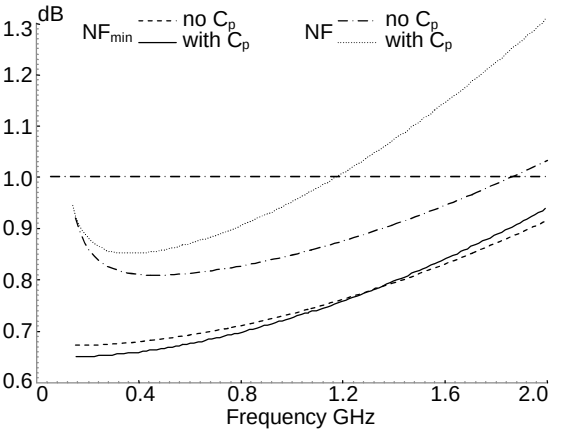

Fig. 12: Noise figure with C_L, with and without C_p

Circuit 2 exhibits a good impedance matching (Fig. 9) from 350 MHz to 2 GHz. Impedance matching of circuit 1 is even better.

The gain peaks at 47 dB at 0.15 GHz and decreases to 25 dB at 2 GHz. No attempt has been made to flatten the gain (inductor connected to ground for example). The simulated noise figure (Fig. 10) is below 1 dB on this frequency band, with circuit 1 being better than circuit 2 below 0.4 GHz as expected.

Circuits 1 and 2 are unconditionally stable. The output 1dB compression point P_{-1dB} is about – 3 dBm. This value is low because no element has been considered to increase P_{-1dB}. In particular, the second stage is identical to the first one and used only for output matching. Die's dimensions for circuit 2 are 1*0.7 mm^2 and the power consumption is 45 mW.

Simulated scattering parameters and noise figures (NF and NF_{min}) of circuit with C_L are respectively presented on Fig. 11 and Fig. 12. When taking into account the parasitic capacitors C_p of about 0.6 pF with the substrate, created by the coupling capacitors, input and output impedance matching for circuit 2 deteriorates slightly ($|S_{11}|$ < -12 dB and $|S_{22}|$ < -9 dB on this frequency band). The gain $|S_{21}|$ decreases by 1.5 dB. The simulated noise figure increases to 1.3 dB at 2 GHz

III.2. Measured circuits

The measured scattering parameters and noise figure (NF) are presented on Fig. 13 and Fig. 14.

Noise figure is classically measured with a diode which noise is defined with a 0.2 dB uncertainty. NF is corrected for measurement losses. The measured and simulated power consumptions are identical (45 mW).

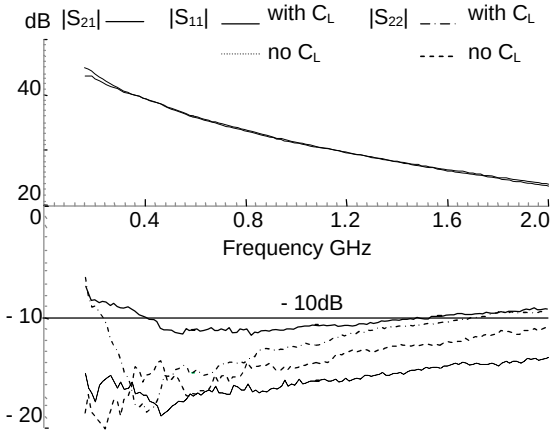

Fig. 13: Measured [S] parameters

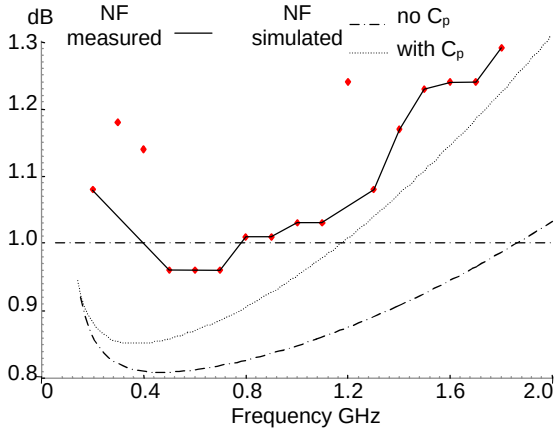

Fig. 14: Simulated and measured noise figure NF

We obtain a good agreement between simulated and measured scattering parameters. Circuit 1 achieves a better impedance matching ($|S_{11}|$ and $|S_{22}|$ < -12 dB) than circuit 2 ($|S_{11}|$ and $|S_{22}|$ < -9 dB). We obtain a good agreement between simulated and measured noise figure. The simulated (with C_p) and measured noise figure are respectively 1.22 dB and 1.29 dB at 1.8 GHz. The minimum measured noise figure is 0.95 dB at 0.5 GHz.

IV. CONCLUSIONS AND PROSPECTS

We have successfully designed and manufactured a low noise wide band amplifier. This paper shows that we can match input and output impedance to 50 Ω and obtain a low noise figure on a relatively large frequency band [0.15 – 2 GHz], with a SiGe 0.35 µm BiCMOS commercially available process from AMS, without using a feedback resistor. A good agreement is reached between simulations and measurements. The measured noise figure is 0.95 dB at 0.5 GHz and 1.29 dB at 1.8 GHz.

Future improvements include flattening the gain and increasing output 1dB compression point, using a passive circuit and improved active loads for example.

[1] D. Harame et al., *«The emerging role of SiGe BiCMOS technology in wired and wireless communications »*, 4th IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 2002

[2] Beom Kyu and Kwyro Lee, *«A Comparative Study on the Various Monolithic Low Noise Amplifier Circuit Topologies for RF and Microwaves Applications. », IEEE Journal Of Solid State Circuits,Vol.31, No. 8, August 1996*

[3] S.P. Voinigescu et al., *«A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design », IEEE Journal Of Solid State Circuits,Vol.321, No. 9, August 1997*