A high-resolution FPGA-based frequency counter for metrology applications with automatic Nyquist zone detection

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Frequency counters are generally used to determine the frequency of a periodic electronic signal. Simply counting the number of zero crossings of the signal within a certain period of time by far does not provide the resolution that is typically required in frequency metrology. Thus, sophisticated interpolation methods were developed to increase the resolution [1]. These measurements can be carried out directly on analog signals. However, it is more advantageous to digitize the signal and carry out the analysis in the digital domain. In this case, efficient filtering and interpolation algorithms can be implemented to obtain correct frequency information even from noisy signals.

When analyzing digital signals, it must always be considered that the signal can be distorted by aliasing through the AD conversion if its frequency exceeds the Nyquist frequency. We have developed a novel method with which we can determine unambiguously the frequency of undersampled signals beyond the Nyquist frequency. In this method, the ADC sampling frequency is changed dynamically, and the resulting frequency shift is measured. The Nyquist zone is automatically determined from the ratio of these two frequency shifts. Additionally, choosing a suitable sampling frequency circumvents frequency gaps near integer multiples of the Nyquist frequency.

We use the Red Pitaya STEMLab platform 125-14 [4] which can be found in many applications in the field of time and frequency metrology. For this platform, the properties of the AD converters are well characterized [5]. For automatic Nyquist detection, the Red Pitaya hardware was modified so that the sample clock of the ADC is created in the FPGA by a PLL from an external 100 MHz reference. With this technique, the measuring range of the counter could be extended to up to 500 MHz. Two different methods to extract the frequency information have been implemented.

The first method employs an all-digital-phase-locked-loop (ADPLL) [6-7], comparing the phases of the input signal and the output of a direct digital synthesizer (DDS) and feeding back the phase-difference to the DDS frequency tuning word via a loop filter. As the DDS phase in the locked state follows the phase of the input signal, the DDS tuning word represents the frequency of the input signal within the PLL tracking bandwidth. With this approach, the bandwidth can be adjusted to efficiently remove unwanted noise. However, there is a risk that the phase of the measurement signal will be lost (cycle-slip) due to rapid changes or amplitude collapses. Although this error can be detected under most relevant conditions, the absolute phase information cannot be restored.

The second method to determine the frequency and phase is based on the accumulated unwrapped phase between the digital signal and a fixed-frequency digital oscillator (NCO). A Hilbert transform of the input signal is implemented to obtain the full phase information.

Both methods were implemented in a way that multiple signal components can be distinguished in the digital signal. This is, for example, useful in frequency comb applications. By using configurable bandpass filters in the FPGA, it is possible to separate these (aliased) frequency components into several data streams and analyze them separately using the aforementioned methods. The implemented filters require a frequency spacing of ≥ 3 MHz between the components to be analyzed.

We will describe the implementation of this method in detail and present and compare the corresponding measurements.

References

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