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TALON Asynchronous – SKA Mid.CBF Timing and Synchronization without Central Timing Reference

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The TALON Asynchronous design is an approach to the Square Kilometer Array (SKA) Mid Frequency Correlator/Beamformer (Mid.CBF) signal processing chain that supports the application of timestamps, delay tracking and other models without requiring that Mid.CBF is synchronized with the Central Timing Reference (CTR). There are two key advantages of implementing Mid.CBF in such a manner. First, the cost and complexity of Mid.CBF can be reduced by removing the internal timecode distribution system and reducing bulk memory requirements. Second, Mid.CBF can be deployed in locations that do not have access to the CTR locked timing signals, such as the System Integration and Test Facility (ITF) or Science Processing Center (SPC), both of which will be located in Cape Town. This talk begins with a short description of the Mid.CBF design presented at the Critical Design Review (CDR) which required clock and 1PPS timing signals locked to the CTR and then provides a detailed description of how it will be implemented without these timing signals. The implementation presented is based on the COTS PCIe FPGA cards planned for using in Mid.CBF. Mid.CBF receives all required timing information from metadata in the digitized data streams and synchronization is performed without any system wide clock / 1PPS distribution system. Each Field Programmable Gate Array (FPGA) device is clocked using a local crystal oscillator with the logic running at a clock rate faster than required to keep up with input data. Processing rate is throttled to match input data rates, which are synchronized to the CTR across the SKA_Mid array via the distributed reference clocks that drive the analog to digital converters in the digitizers at each dish. The underlying signal processing performed does not change from the Mid.CBF CDR design; changes are isolated to data management and "when" particular signal processing steps occur.

Identified advantages / key factors of this approach for Mid.CBF include:

1. Flexibility in selecting the location of Mid.CBF without adding a GPS based frequency reference/1PPS or an additional system to recover CTR locked timing signals from DSH data.
2. Elimination of CTR locked clock / 1PPS interfaces.
3. Elimination of timecode distribution hardware, firmware and software. This reduces production hardware costs, design effort and system complexity. It also increases the portability to Commercial off the Shelf (COTS) hardware.
4. Reduction in bulk memory usage.
5. Elimination of the discontinuities in the data stream generated by periodic bulk delay changes.
6. Support for On-the-Fly Mapping mode in the standard imaging correlator FPGA design.

The TALON Asynchronous design underwent review by a panel of correlator experts in March 2021, received positive feedback and has since been adopted via an approved SKA Engineering Change Proposal (ECP) to move Mid.CBF from the Karoo Array Processor Building Central Processing Facility Central Processing Facility (KAPB-CPF) at the SKA_Mid site to the SPC in Cape Town. Functional simulation of the key FPGA firmware functions was performed leading up to the external review and more recently, the TALON Asynchronous design has been implemented in the TALON Demonstration Correlator (TDC) FPGA firmware for SKA Array Assembly 0.5 and Array Assembly 1.