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Tailoring Wireless Intra-Chip Communication Links Using a Programmable Metasurface

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In multi-core chipsets, intra-chip communication is a crucial part of the parallel computing process as it allows to exchange information between cores. These communication links are conventionally realized using wired interconnections. Such interconnections need to be kept short to avoid excessive link delays, power consumption, and other damaging factors. Therefore, as the number of cores increases, the number of link traversals needed to reach the destination with wired interconnects grows drastically, motivating the search for complementary alternative interconnect technologies. An enticing candidate are wireless links between different cores based on millimeter waves. In this framework, each core is equipped with a small antenna for transmitting and receiving signals. The chipset package surrounding the multi-core chip acts like a metallic enclosure that prevents interference between the on-chip wireless communication and the outside world.

Wireless intra-chip links, however, face their own set of challenges. The metallic enclosure (the chip package) of a multi-core chip acts like an electrically large cavity. If this cavity is lossy due to thick silicon layers (silicon layers are an inevitable part of a multi-core chipset), the signal is significantly attenuated before arriving at the receiver. If the silicon layer is kept thin, the propagation losses are mitigated. However, this gives rise to a multipath environment and the channel impulse response becomes long due to reverberation inside the metallic enclosure. Since the transceiver modules used for intra-chip communication links must be kept simple, they rely on simple modulation techniques and struggle to handle the low signal to noise ratio of the former case or the multipath effect in the latter case.

In this presentation, we overcome the above challenges by introducing a programmable metasurface into the multi-core chip packaging. The underlying idea is that the programmable metasurfaces endows the on-chip propagation environment with programmability [1, 2]. It offers degrees of freedom that allow us to navigate the trade-off described above, similar to the idea of using programmable metasurfaces as reconfigurable intelligent surfaces on the indoor scale. We start by designing programmable meta-atoms that can be deployed in an on-chip environment. Each designed meta-atom is equipped with a varactor. Its reflected phase can change by around 180° as the DC voltage addressing its varactors is changed. Once the element design is complete, we examine a cavity similar to the one encountered in multi-core communication in full-wave simulations. We simulate this environment when one of its walls is covered by an array of the designed programmable meta-atoms. Using this simulation setup, we show that by changing the reflection phase of the meta-atoms, we can shape the channel impulse response to take a pulse-like shape despite strong multipath effects, thereby effectively mitigating the impact of multipath and associated inter-symbol interference. We conclude this presentation by outlining future directions of programmable metasurfaces for intra-chip communication links and other similar environments.

References

[1] M. Imani, S. Abadal, P. Del Hougne, "Smart On-Chip Electromagnetic Environment," *arXiv:2109.03284*, 2021.

[2] M. Imani, S. Abadal, P. Del Hougne, "On-Demand SIMO Channel Impulse Response Shaping in Smart On-Chip Electromagnetic Environments," in *Proceedings of the ACM NanoCoCoA '21*, Coimbra, Portugal, November 2021.