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Packaging of a Beamforming IC by Laser Enhanced Direct Print Additive Manufacturing (LE-DPAM)

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Abstract

This paper presents the first demonstration of a 24.25-27.5 GHz 4-channel differential beamforming integrated circuit (BFIC) (AWMF-0135) packaged using a laser-enhanced direct print additive manufacturing (LE-DPAM) technique. LE-DPAM allows for the direct integration of the beamforming IC package, radio frequency (RF) signal, and digital control lines over a multi-layer electronic assembly structure. By taking advantage of the automated LE-DPAM platform capabilities (fused deposition modeling (FDM), microdispending, milling, and laser micromachining), we complete the entire packaging process without removing the BFIC from the printing bed.

1. Introduction

Engineers have employed additive manufacturing (AM) to build multi-layer structural electronics, while combining microdispensing, FDM, laser machining, milling, pick-and-place, and other techniques within a single automated platform. Compared to conventional fabrication methods, these AM processes facilitate innovative structures in 3D printed electronics exhibiting superior performance via their uniqueness, degrees of freedom in construction, and multi-function integration [1]. AM also allows design flexibilities in material selections. Filament based FDM printing typically uses Acrylonitrile butadiene styrene (ABS); however, ULTEM Polyetherimide, Polycarbonate (PC), and Cyclo-Olefin-Polymer (COP) are three other substrate materials [2] that may benefit designs in terms of different dielectric constants, lower losses and/or operation under higher temperatures. Combination of these materials or their density variations in a single print can allow for controlling dielectric constant and achieving better thermal management. Conductive traces can be realized with different silver inks and pastes with typical trade-offs being in conductivity and printing resolution.

Many 5G wireless communication systems designers use BFICs for implementing phased array antennas. Increased path loss at millimeter wave (mmW) frequencies necessitates the design of smaller and more compact designs. The integration of phased antenna arrays with multiple BFICs operating at mmW bands via traditional manufacturing is challenging [3]. Therefore, AM holds promise to alleviate challenges and increase the level of integration. Recently, we have employed LE-DPAM to implement mmW phased antenna array elements integrated with different IC components such as discrete switches and phase shifters [4, 5]. This paper presents the progress in utilizing LE-DPAM for realization of mmW phased antenna arrays operating in the 24.25~27.5 GHz band while embedding 4-channel BFICs. The packaging format of BFICs, the inclusion of amplifiers, and the inclusion of the digital control electronics all present unprecedented challenges for LE-DPAM based packaging of mmW phased antenna arrays. This paper describes the successful design and integration of such a BFIC utilizing LE-DPAM methods.

2. Package Design and Integration

In LE-DPAM, we can conveniently introduce new material and conductive layers to increase the level of integration. In references [4] and [5], we placed thicker substrate layers with vertical transitions to realize the antenna elements directly over the thinner substrate layers that are used to host the IC packages. Since BFICs are more challenging to integrate due to their significantly larger package format (as opposed to discrete phase shifters or switches of prior work), we chose to start by demonstrating a successful BFIC integration using LE-DPAM by prototyping a compact test board.

Fig. 1 shows the design of the test board that consists of two dielectric substrates and two conductive layers. The base dielectric substrate layer acts as a rigid support for the other layers to include the integration of antenna elements in future designs. Both the RF and direct current (DC) control signals utilize the common ground layer. The thickness of the 0.2 mm thick top dielectric substrate layer is based on 50 Ω microstrip lines placed on the top. ABS is used for base and top substrate layers with a relative permittivity of ε_r=2.51 and a loss tangent of 0.0043. We characterized these dielectric properties using a thin sheet cavity resonator before carrying out the layout design. We use DuPont CB028 silver conductive paste for the conductive traces. DuPont CB028 exhibits an effective RF conductivity of 5×10^6 S/m at 30 GHz [6]. The BFIC comes with a quad flat no-leads (QFN) 48 lead 6×6×0.8 mm^3 package. The QFN package is embedded upside-

down into the structure and its height penetrates through the top dielectric, ground, and base layers. This exposes the QFN package pads on the top during packaging and allows interconnects to form with other traces during microdispensing of the conductive RF and DC control traces. There are five microstrip to grounded co-planar waveguide (GCPW) transitions designed and formed by micro-dispending RF traces to interface with the BFIC RF pins. These transitions are designed through ANSYS HFSS 3D EM simulations, and the performance is experimentally validated with LE-DPAM prints of the transitions. We present the measured loss per unit length from the 15 mm long lines in Table 1. Transmission line loss over the microwave printed circuit board (PCB) laminates at 20 GHz is ~0.03dB/mm. The printed samples exhibit a loss of ~0.05dB/mm at 20 GHz that is almost on par to the PCB laminate counterparts. Moreover, the loss remains below 0.2 dB/mm up to 27 GHz (Table 1), which makes LE-DPAM and material choices suitable for mmW phased antenna array packaging.

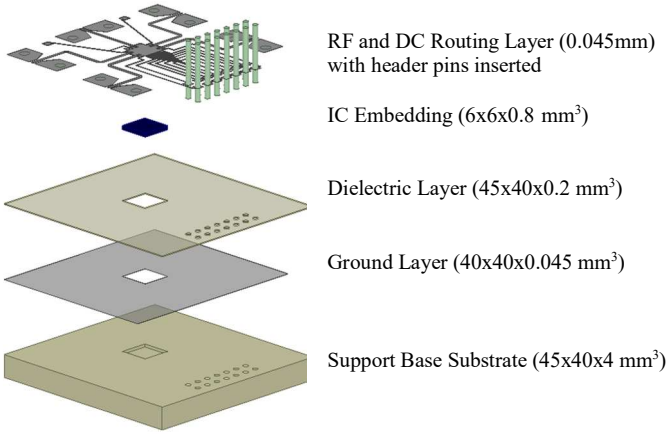

Figure 1. Test board layers for structural integration and experimental verification of a mmW BFIC by LE-DPAM.

Table 1. Measured loss per unit length versus frequency.

Frequency (GHz)	14	15	19	20	26.5	27.5
Loss per unit length (dB/mm)	0.036	0.041	0.049	0.055	0.166	0.206

We used header pins to interface DC bias and digital control/data communication signals with an external microprocessor board. The base substrate has a cutout (milled at the end of the process) under the BFIC package to embed an aluminum heatsink. We based the size of the heat sink according to thermal simulations performed in ANSYS ICEPAK with the associated thermal properties for ABS and CB028 silver conductive paste shown in Table 2. The heat sink size is 12×12×3 mm^3 and is expected to maintain the BFIC below 75℃ under any operation mode with a peak power of 0.83 Watts.

We printed the test board from bottom to top with the base dielectric substrate layer printed first. An nScrypt 3Dn-450 platform is used for the LE-DPAM. The ABS filament used has a glass transition temperature of 90℃. Therefore, we cured the conductive paste by maintaining the printer bed at 80℃ for at least two hours. We used the micromilling capability of the LE-DPAM platform to form the cavity needed for embedding the BFIC. We also used micromilling to drill the via and mounting holes for header pins with diameters of 0.5 mm and 0.8mm respectively. Since a cylindrical drill bit cannot generate 90° corners, we create ears at the four corners of the cavity that allows for easy BFIC insertion.

Table 2. Properties used for ANSYS ICEPAK simulation.

Materials	Thermal Conductivity (W/m·℃)	Mass Density (kg/m^3)	Specific Heat (J/kg·℃)	Thermal Expansion Coefficient (1/℃)
ABS	0.172	1080	1990	8.1e-5
CB028	0.7	1000	1200	0

Fig. 2 shows the fabricated test board and images during several stages of fabrication. The front and back sides of the package are shown in Fig. 2(a) and (b). All RF ports are connectorized with 2.92 mm connectors and DC header pins are accessed with jumper wires. Fig. 2(c) shows the BFIC cavity. There is a potential risk for the conductive paste to escape into the gap between the QFN package and dielectric substrate layers. Therefore, we use FDM at an elevated temperature to print a thin barrier on the perimeter of the QFN IC package to serve as a trench refill. The elevated temperature helps to increase the sticking of ABS to the exposed trench surfaces surrounding the IC. We employed laser micromachining after drying/curing the ink to improve the RF conductivity, especially for GCPW and transmission lines. The reader can find experiment results showing the improvements with laser micromachining on

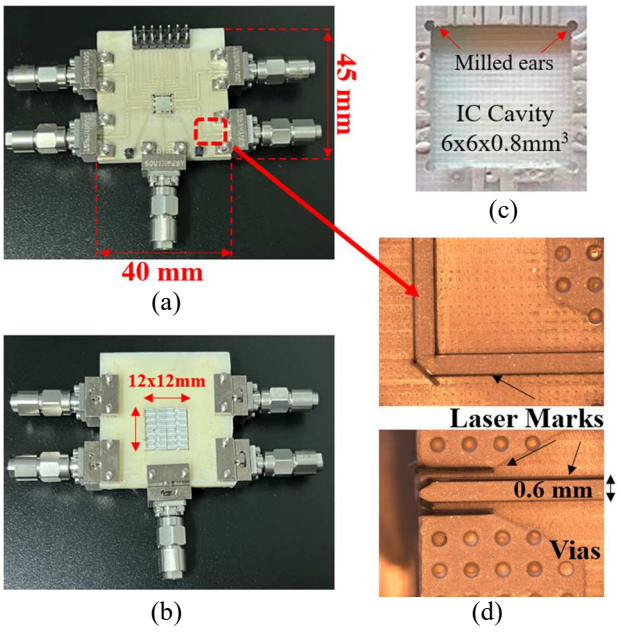

Figure 2. (a) Front side and (b) back side of the BFIC integration package; (c) milled BFIC cavity with round ears at four corners and (d) laser micromachining to trim the RF lines edges to enhance RF conductivity.

the effective conductivity in reference [6]. Fig. 2(d) shows the precision in manufacturing of the conductive traces. The test board is currently under test and we will present the measurements at the time of the conference. Future work will also include phased array results upon final integration of antenna elements over the test board through the addition of more dielectric substrate and conductive layers via LE-DPAM processes.

3. Concluding Remarks

We have integrated a mmW BFIC package within a test board structure by using LE-DPAM as a first step towards realization of full-scale 3D integrated high performance active mmW phased antenna array. Future work includes modification of the existing design by inclusion of additional dielectric and conductive layers to host antenna elements over the structurally integrated BFIC. We will discuss additional design details and experimental results at the time of the conference.

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