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Channel Characterization and Engineering for Wireless Chip-Scale Communications

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Multicore processors, used virtually in every computing domain from embedded systems to large supercomputers, nowadays rely on an integrated packet-switched network for cores to exchange and share data. The performance of these intra-chip and inter-chip networks, commonly referred to Network-on-Chip (NoC) and Network-in-Package (NiP), respectively, is a key determinant of the processor speed. When the number of cores per chip and the number of chips increases, the NoC/NiP become an important bottleneck due to scalability issues related to transporting packets across an increasingly dense network. To address this, several works propose the use of millimeter-wave/terahertz wireless interconnects for chip-scale communication and demonstrate that, thanks to their low-latency broadcast and system-level flexibility, this new paradigm could break the scalability barriers of current processor architectures [1].

The main caveat of a large fraction of the wireless chip-scale communications research is that it lays on incorrect channel models. Many works either neglect the influence of the chip package, which is a great contributor of losses and dispersion, or directly neglect dispersion [2]. While this does not invalidate the potential of this wireless paradigm, it leads to erroneous assumptions on the achievable speed and power. For instance, many works assume bandwidths amply exceeding 10 GHz, which may not be achievable due to reverberations within the package [1, 2]. Other works obtain power consumption estimates by assuming a path loss of a few tens of dB.

In this presentation, we first dispel such assumptions by presenting a wireless channel characterization work in the frequency and time domains for in-package links at millimeter-wave frequencies, showing that commercial packages cannot support the path loss and bandwidth assumed in the literature. Then, we present a co-design methodology that allows to reduce the path loss and delay spread through channel engineering, this is, by optimizing the dimensions of the silicon substrate and the heat spreader present in most commercial chip packages [3]. Through this method, we obtain a reduction of the path loss of several tens of dB and a severalfold improvement of the worst-case delay spread. Finally, we describe how communication engineers can exploit the static nature of the wireless in-package channel to combat dispersion in unique ways. Thanks to such a cross-layer optimization technique, we reach beyond the conventional coherence bandwidth limit and achieve dispersion-free operation without incurring into prohibitive complexity or power requirements [3].

References

[1] D. Matolak, S. Kaya, and A. Kodi, "Channel modeling for wireless networks-on-chips," *IEEE Communications Magazine*, 2013.

[2] S. Abadal, C. Han, and J. M. Jornet, "Wave Propagation and Channel Modeling in Chip-Scale Wireless Communications: A Survey from Millimeter-Wave to Terahertz and Optics," IEEE Access, vol. 8, pp. 278-293, December 2019.

[3] X. Timoneda, S. Abadal, A. Franques, D. Manessis, J. Zhou, J. Torrellas, E. Alarcón, and A. Cabellos-Aparicio, "Engineer the Channel and Adapt to it: Enabling Wireless Intra-Chip Communication," *IEEE Transactions on Communications*, 2020.