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# Wide Band RF ADC Conversion Artefacts and their Impact on Radio Astronomy

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## Abstract

Current trends in state-of-the-art RF Analogue to Digital Converters (ADCs) indicate that their performance is approaching theoretical bounds imposed by the jitter noise of the supplied/distributed sample clock [1, 2]. In the first part of this paper, we show that ADC jitter noise, in the presence of strong, band-limited input signals, impacts the noise-floor performance of high-resolution ADCs which has a particularly harmful effect on pulsar radio astronomy. Furthermore, many of the current wide bandwidth RF ADCs typically rely on precise time-interleaving of several lower-rate ADCs to achieve high output resolution at the full Nyquist rate (see e.g. [3, 4]). In the second part of this paper, we present a new adaptive technique to mitigate the residual effects of time-interleaving artefacts from high-performance ADCs caused when strong, band-limited RFI is present at the converter input.

## 1. Introduction

At least 9 surveys of the evolution of ADC technology and performance have been reported in the literature [2]. The earliest of these, [1] presented converter performance trends and compared these to various theoretical limits, including sample clock jitter which is the focus of the first part of this paper. The most recent and comprehensive survey [2] covering the evolution of ADC development and performance over almost four decades to 2012, suggests that some performance characteristics of State-of-the-Art (SoA) devices are approaching hard theoretical limits of the underlying (mainstream) device technology and architectures. In [2] Johnson shows that one of the primary converter parameters of sample time jitter has already reached a state of "saturation" imposed by limits on the capacity to generate low-jitter sample clocks.

As SoA wide-band RF ADCs move above the 5GS/s sample rate range with 12 to 14 bits of resolution [3-5], the effects of very low-level artefacts such as sample clock jitter, which were previously masked by the higher converter noise floor, are now becoming noticeable. In some applications, these effects are critically impacting the overall system performance in which the ADCs are used. In Section 2 of this paper, we show that strong, band-limited RF Interference (RFI) which is ubiquitous at all but the most remote radio observatories, couples with the sample clock jitter of the RF ADC, impacting the noise floor performance of the converter. In conditions where the RFI power is also time-varying, common for mobile telephony base stations, the impact on radio astronomy, particularly Pulsar astronomy, can be severe.

A group of effects that are closely related to the sample clock jitter in SoA ADCs are conversion artefacts caused by small errors in time-interleaving of multiple sub-converters. Time-interleaving arrays of lower-rate ADCs (usually on the same device die) is an architecture that can deliver higher overall converter resolution (number of output bits) while still meeting the requirements of very high RF sample rates and the practical constraints of die size and power consumption [6]. Precise time-interleaving of 4 or 8 sub-converters is widely used in many of the current wide bandwidth RF ADCs to achieve high output resolution at the full Nyquist rate (see e.g. [3-5]). Time-interleaved ADCs generally have sophisticated start-up and even real-time/adaptive calibration processes to keep the sub-converters equalized for any offset or gain mismatches or errors in phase alignment. However, as with the clock jitter effects mentioned earlier, strong, band-limited RFI couples with any residual interleaving errors resulting in spectral artefacts, termed "interleaving spurs", that can appear in-band and at a sufficiently high level to impair sensitive radio astronomy measurements, in particular spectral line observing.

In [7] it was shown that the interleaving spurs for the Xilinx RFSoC ADCs [4] were below the noise floor once the device calibration algorithm was enabled. However, in Section 3 of this paper we show the impact of interleaving artefacts in data taken from the Parkes radio observatory's Ultra-Wideband Low (UWL) receiver [8] are noticeable in the integrated power spectrum after long integration times and in the presence of very strong band-limited RFI from a local communications tower. These spectrum artefacts occur in a critical region for red-shifted Hydrogen line observing. In Section 3 we present a new adaptive algorithm for real-time mitigation of interleaving spurs and show that the spectrum artefacts are undetectable in the resulting integrated power spectrum after compensation.

In the final section of this paper, we draw conclusions from the work in each of the main two sections and present areas of further work.

## 2. Sample Clock Jitter

Sample clock jitter, or uncertainty in the sample instant from one sample to the next, will always be present to some

degree in an ADC output and is the result of several contributing sources of timing jitter; including jitter in the reference clock source itself; degradation from the clock distribution network, and active devices along it such as fan-out buffers; as well as within the ADC device due to the process technology and internal architecture.
For radio astronomy instrumentation, it is typical to distribute a very high quality "station reference" clock signal that might be obtained from a Hydrogen maser or a GPS-disciplined Rubidium reference oscillator, followed by local clock synthesizers consisting of tightly locked "clean-up" loops to deliver the final sample clock to the ADC device clock pins [8]. However, even with these considerable and expensive measures, the performance limit on SoA low-jitter ADC clock synthesis sits at around 90fs and from the survey in [2], the limit appears to have reached "saturation" of around 100fs since 2005.

The process of output noise generation caused by sample time jitter with an input sinusoid to the ADC is shown in Figure 1.

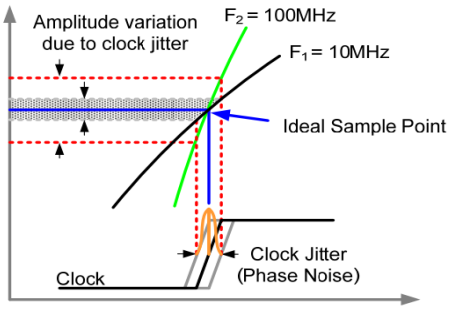



**Figure 1.** Converter amplitude noise induced by sample clock jitter for two different sinusoidal inputs showing the dependence on both input amplitude and frequency.

From the minimal case of pure sinusoidal input signals shown in Figure 1, the induced jitter noise, $\Delta V$ , is proportional to both input amplitude and frequency, i.e.,

$$\Delta V \propto 2\pi A f_{in} \Delta_t \qquad (1)$$

where the input sinusoid amplitude and frequency are given by $A$ and $f_{in}$ , and the sampling jitter is represented by $\Delta_t$ . For sinusoidal inputs the worst-case amplitude jitter will occur at the zero crossings and, since $\Delta_t$ is randomly distributed, the sampling jitter has the effect of spreading the power in the input tone across the whole converter output spectrum thus increasing the converter noise floor. This can also be expressed as the sample jitter contribution to the converter Signal-to-Noise Ratio (SNR) [2] as

$$SNR_J = -20\log_{10}\left(2\pi f_{in}\Delta_t\right) \qquad (2)$$

In (2) the sample jitter induced SNR is explicitly denoted $SNR_J$ to highlight the fact that it is independent of other converter noise contributions and will be present in the ADC output even for perfect (infinite) converter resolution. This effect is demonstrated in isolation through computer simulation, the results shown in Figure 2, where a fixed band-limited noise is present at the ADC input plus a second band-limited noise whose power is stepped for two separate simulation runs. The sample clock jitter is fixed for both runs at a representative value of 100fs.

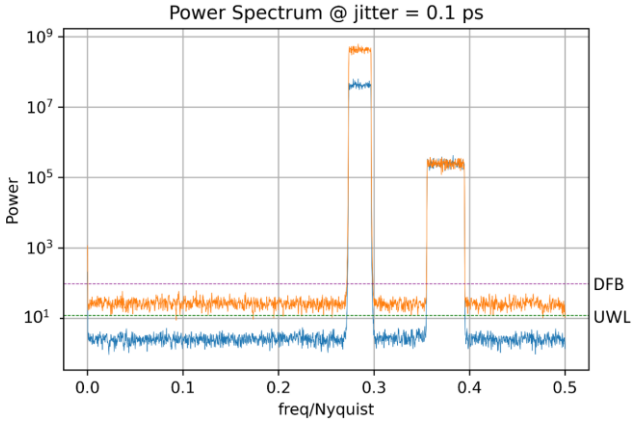



**Figure 2.** Simulated noise floor fluctuations from an artificially introduced strong bandlimited source coupling with the ADC sample clock jitter.

Note that the ADC noise floor changes in proportion to coupling of the stepped-power band-limited noise. For reference the noise floor of a previous generation instrument "DFB" (Digital Filter Bank) using 8-bit 512MS/s ADCs at the Parkes observatory is shown along with the noise floor of the current generation UWL [8] based on 12-bit 4GS/s ADCs; highlighting that jitter noise has recently become a significant impediment on high-dynamic-range SoA ADC applications such as pulsar radio astronomy.
These simulation results are supported by recent measurements in the laboratory on a new prototype wideband receiver based on the Xilinx RFSoC 12-bit, 4GS/s devices [4], Figure 3.

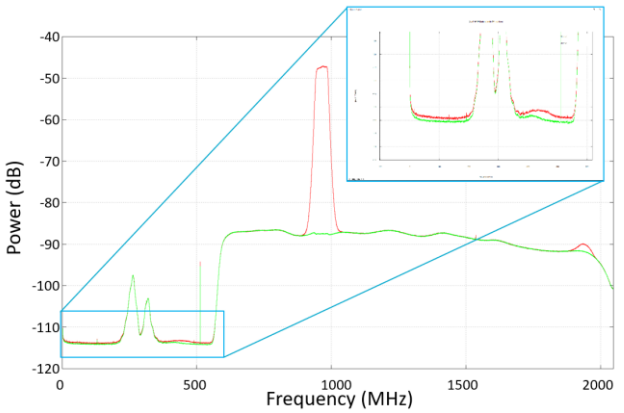



**Figure 3.** Measured noise floor fluctuations from an artificially introduced strong bandlimited source coupling with the ADC sample clock jitter. The device is a Xilinx RFSoC 12-bit, 4GS/s RF-ADC.

Figure 3 shows a digital receiver bandpass from approximately 600MHz to 1800MHz (green) and then with a strong band-limited noise centered at 950MHz added (red). The zoomed insert panel from DC to 500MHz clearly

shows that the added broadband noise has also raised the ADC noise floor for this measurement.

The impact of ADC jitter noise on radio astronomy measurements has been observed recently in pulsar observations which rely heavily on a fixed instrument noise floor for the duration of the observation. With new wideband receiver systems, such as the Parkes UWL, and emerging receivers based around the Xilinx RFSoC, the RFI environment can be up to 30-40dB in power-spectral density above the astronomy signal at the ADC input and the ADC input power is therefore dominated by strong RFI. As we have already seen in this section, the jitter noise floor is set by strong band-limited RFI entering the converter input and therefore, fluctuations in the RFI power will result in fluctuations in the measurement noise floor of a similar magnitude to the astronomy signal variations we are trying to detect.
The effect is highlighted in Figure 4 where the raw receiver data has been "folded" for a nominal pulsar pulse-period of 1 second. The upper part of the figure gives the spectrogram showing vertical bands across the entire 1GHz bandwidth that are directly correlated with strong RFI from a communications tower operating from 1815MHz to 1825MHz and fluctuating in transmitted power on the timescale of the order of a second.

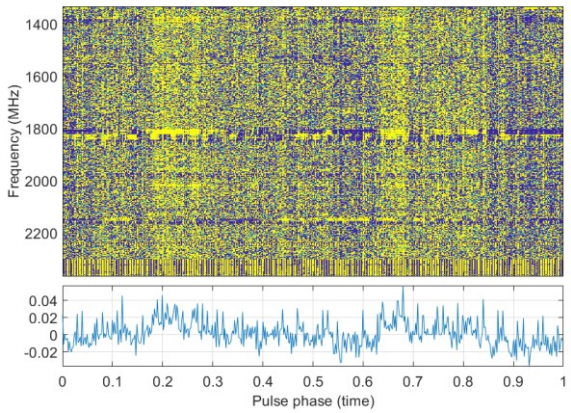


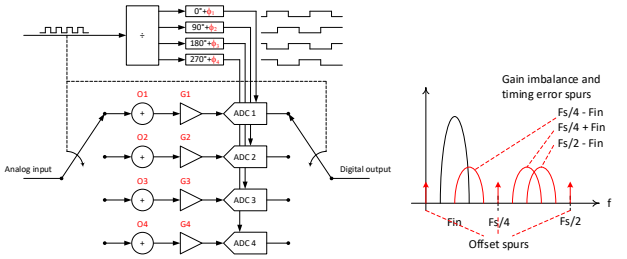

**Figure 4.** Uneven noise floor after pulsar folding due to self-generated broadband interference from broadband spreading from sample clock jitter of a strong and time-varying bandlimited interferer centered at 1820MHz.

The lower plot in Figure 4 is the median-filtered total power in each phase (time) bin across the 1GHz bandwidth. In this measurement, which does not contain any known pulsar, the lower plot should be approximately flat across all phase bins and the pulse profile of a pulsar if it were present could be approximately of the order of the fluctuations seen here.

## 3. Time-Interleaving ADCs

### 3.1 Interleaving Effects

The basic architecture of a 4-way time-interleaved ADC is shown in Figure 5 (a), with the three primary causes of interleaving spurs highlighted in red.




(a) (b)

**Figure 5.** (a) A 4-way time-interleaved ADC architecture with the primary interleaving error contributors shown in red; (b) interleaving spurs in the device output spectrum for a 4-way interleaved ADC caused by offset and gain mismatch and timing skew errors.

In [6] it is shown that offset mismatch, denoted *O1-O4*, appears as narrow spurs in the spectrum at integer multiples of a quarter of the high-rate sample frequency, *Fs*. The interleaving spurs caused by gain imbalances between the sub-converters, *G1-G4*, and by phase errors in the four separate sample clocks, $\phi_1 - \phi_4$, however depend on both *Fs* and the ADC input signal frequency, *Fin*. These ADC output spectrum effects are summarized in Figure 5 (b)

There is a substantial body of work in the open literature covering fixed and adaptive compensation schemes for ADC interleaving artefacts (see e.g. [9, 10]) that make use of calibration signals or operate "blind" using the incoming ADC data. Proprietary algorithms in commercial ADCs are usually closely guarded IP and are typically not disclosed.

Nevertheless, when strong band-limited RFI is present in the ADC input, as we have seen in the previous section, residual errors in the interleaving can still pose significant problems where extremely sensitive measurements are called for. One example is in spectral line observing where perhaps several hours of spectrum data is averaged down to detect minute molecular or atomic absorption or emission lines. An example of ADC interleaving artefacts impacting an observation is shown in Figure 6.

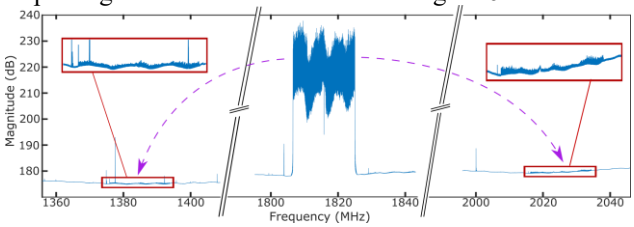



**Figure 6.** ADC interleaving artefacts resulting from strong, bandlimited RFI from 1815MHz to 1825MHz.

Here, the band of frequencies around 1380MHz is an important astronomical band for red-shifted Hydrogen line observing and, in this case, has been significantly degraded by the presence interleaving artefacts shown in detail in the inset plots.

### 3.2 Real-Time Adaptive Compensation

In this section we present an algorithm based on the Least-Mean Squares (LMS) iterative update [11] that can be run on-line with the astronomical data and adapts in real-time

to the time-varying characteristics of the ADC interleaving artefacts as the strong RFI itself changes. The implementation of the adaptive filter, arranged as an "interference canceller" [11], in a typical radio astronomy digital receiver signal chain is shown in Figure 7. Here, we make use of a polyphase filterbank channelizer but this could equivalently be done using two separate bandpass filters to provide the "signal+noise" and the "noise only" adaptive filter inputs.

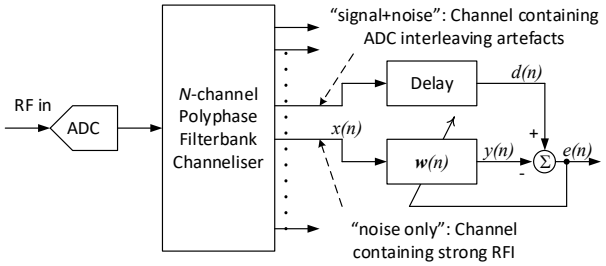



**Figure 7.** Digital receiver architecture incorporating LMS adaptive compensation for ADC interleaving artefacts.

The LMS algorithm iteration update is summarized as follows:

Initialize:

$$\mathbf{w}(0)=\mathbf{1}+\mathbf{1}j;\mathbf{x}(0)=\mathbf{0}$$

For each new sample $x(n)$ update:

$$\mathbf{x}(n)=\left[x(n);\mathbf{x}(n-1)_{K-1}\right]$$

$$y(n)=\mathbf{w}(n)^{H}\,\mathbf{x}(n)$$

$$e(n)=d(n)-y(n)$$

$$\mathbf{w}(n+1)=\mathbf{w}(n)+2\mu e(n)\cdot\mathbf{x}(n)$$

where $\mathbf{w}(n)\in\mathbb{C}^{K\times 1}$ is a complex-valued $K\times 1$ weight vector for filter order $K$, $\mathbf{x}(n)\in\mathbb{C}^{K\times 1}$ is the input signal vector, augmented with the latest input sample, $e(n)\in\mathbb{C}$ is the output error signal and $\mu$ is the LMS algorithm step size.

The effectiveness of the LMS interference canceller in mitigating the interleaving artefact at around 1380MHz highlighted in Figure 6 is shown in Figure 8. The filter order in this example was $K=2$, and the interleaving artefacts have been effectively removed from the integrated power spectrum (inset).

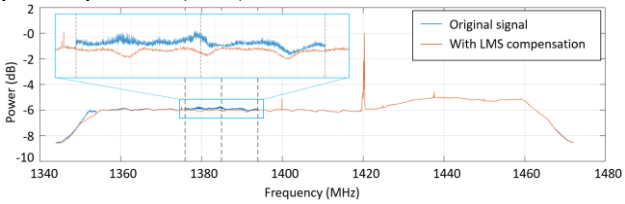



**Figure 8.** Integrated power spectrum before compensation (blue) and after compensation (red). Any residual effects of the ADC interleaving are undetectable in this data.

## 4. Conclusions

Of the two ADC conversion artefacts dealt with in this paper, the sample clock jitter impact on the noise floor is the more serious problem for future radio astronomy instrumentation since, apart from using RF filters to notch out strong RFI, there are no other obvious approaches to mitigation for current mainstream ADC technology. More exotic techniques, such as photonic sampling [12], may provide a way forward but examples of these are still rare or confined to the laboratory.

Real-time adaptive compensation of time-interleaving errors (particularly gain mismatch and timing skew errors) has been shown to be very effective in eliminating, or at least significantly reducing these effects for wide-band radio astronomy applications and the typical instrument architectures employed. Ongoing work in this area is now focusing on fast implementation of the LMS adaptive filter within the Field Programmable Gate Array (FPGA) processing hardware that is widely used in the digital receiver stages of radio telescope systems.

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