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Generating a Realtime Time Scale with the Time Processor

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The traditional design of a time scale is based on a master clock, typically a hydrogen maser, and a set of auxiliary clocks. All the clocks are compared to the master that generates the time scale output, being steered to the average of the auxiliary clocks. The main problems of this solution are reliability, performance, complexity and low flexibility. The first limitation is the failure of the master clock. This problem can be mitigated by an automatic system that switches to a backup master clock, but at the cost of an increased complexity. Traditional designs have the short-term frequency stability of the master clock that is worse than the average of the clocks. In addition, they are composed of many complex instruments with very specific tasks whose integration is often problematic and, in many cases, degrades the short-term stability. Adding new functionalities to the system requires additional hardware. Moreover, the use of new typologies of signals like the ones coming from optical clocks is, in general, cumbersome, because the latter involves odd frequencies.

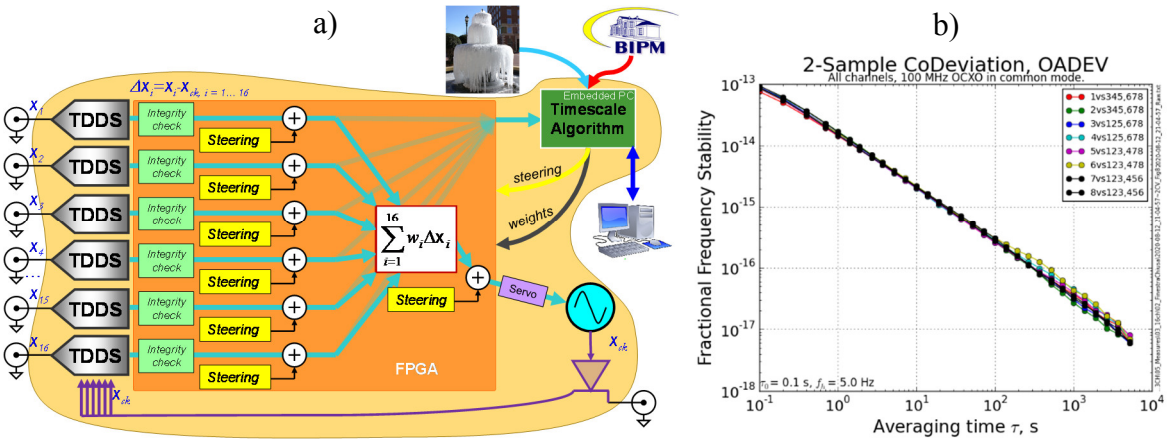

Figure 1. Block diagram of the Time Processor (a). A single board integrates 16 Tracking Direct Digital Synthesizers (TDDSs) used as phasemeters, a Field Programmable Gate Array (FPGA), an embedded processor and a local oscillator. The residual noise of single TDDS, single channel (b).

The Time Processor solves all these problems by processing the phase information contained into the sinusoids at the input instead of the sinusoids themselves. This is a key point. As shown in Figure 1.a, it is based on a bank of 16 low-noise digital phasemeters called Tracking DDS. They provide data to an FPGA that implements integrity check, steering and weighted average, according to the parameters set by an embedded computer. The latter implements the algorithm and interfaces the Time Processor with the external world for retrieving additional information and for monitoring and storing the internal signals. The phasemeters compare the phase time of the inputs with the one of the local oscillator, which is in common mode. At the end of the processing chain, i.e. at the input of the servo, there is the phase time difference between the local oscillator and the weighted average of the steered inputs. When the loop is closed, the servo forces the local oscillator to follow the weighted average of the inputs, and this leads to the physical representation of the clock ensemble.
The noise of the TDDS, reported in Figure 1.b, sets the ultimate performance of the Time Processor, because the processing is done numerically in a noiseless environment. It is well below commercial microsteppers, fully adequate to support active hydrogen masers and not so far from cryogenic oscillators.
Part of this work has been already been published to the 30th Annual Workshop on Synchronization and Timing Systems (WSTS) [1].

1. C. E. Calosso, “The Time Processor: A New Platform for Next Generation Timescales”, Workshop on Synchronization and Timing Systems, WSTS 2021, March 30, 31 & April 1