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Development of General-purpose Digital Backend for Single-dish Centimetre and Millimetre-wave Telescopes

Chao Liu*(1), Michael E. Jones(1), and Angela C. Taylor(1)
(1) Department of Physics, University of Oxford, Oxford, OX1 3RH, United Kingdom

Abstract

Backend systems for radio telescopes have tended to be designed specifically for the particular RF and IF frequencies and digitization bandwidth of the particular project. As analogue-to-digital conversion technology advances, it is becoming feasible and cost effective to develop receivers using wideband digitization with a common architecture. This project lead by the Oxford Experimental Radio Cosmology Group aims to design and develop a common receiver – down-conversion and digital backend – for a number of different telescopes. A down-conversion architecture using a single heterodyne step with IQ mixers and a baseband IF presents a common IF signal to the digitiser from a variety of RF signal sources. The Xilinx RF System-on-Chip device (RFSoC), which has RF ADCs integrated with and FPGA and processors, was selected as the platform for the backend. In this paper, the system architecture of the RFSoC-based digital backend, including the down-conversion circuit interfacing the existing electronics and RFSoC ADCs, will be described. We have performed a comprehensive performance characterization of the RFSoC ADCs, and the test results address concerns about the interleaved spurs, dynamic range, intermodulation distortion and long-term stability. We have successfully developed a real-sampling PFB-based spectrometer on the RFSoC platform and we are currently working on the IQ sampling PFB-based spectrometer. The latest test results for the IQ sampling spectrometer and the future development plan will be discussed in this paper. Applications of the common receiver system will include the CBASS-South telescope, the Goonhilly-3 29-m telescope, the Tulancingo 32-m telescope, and the Redshift Receiver on the Large Millimetre Telescope where the existing IF signal band is comparable to the RF band on the other systems.

1 Introduction

The design and implementation process of digital backend systems for centimetre and millimetre-wave wide-band radio astronomy telescopes can be costly and time consuming. The hardware and software of backend system telescopes are often developed based on the requirements per telescope. This project aims to develop a common architecture for the backend systems, which can be used in all the telescope system under develop in Oxford Experimental Radio Cosmology Group. The system architecture of the backend will be described in this paper.

As analogue-to-digital (ADC) and system-on-chip (SoC) technologies advance, some of the semiconductor vendors, such as Xilinx and Intel, started integrating RF ADCs with FPGA and processors, which include most of the essential components for a backend system. The RFSoC device family from Xilinx has been selected as the base platform for implementing backend systems. There are a number of commercial boards with RFSoC devices available off-the-shelf. We use the Xilinx ZCU111 RFSoC evaluation board for initial system prototyping and Knowledge Resources KRM-4ZU27DR board with the carrier they developed for final system development. The Xilinx ZCU111 evaluation board has more reference designs, which makes it a better platform to develop test prototypes. And the Knowledge Resources KRM-4ZU27DR board has all the input and output ports we need for radio telescope backend. We have performed a comprehensive characterization of the data converters integrated in RFSoC specifically for the critical parameters for radio astronomy with ZCU111 evaluation board. All the results are summaries in [1] and the performance of the data converters is sufficient for radio astronomy applications. In this paper, test results for data converters with KRM-4ZU27DR board will be summarised. In [1], the test results for a real sampling spectrometer has been presented and we have been developing an IQ sampling spectrometer. In this paper, we will present the details of the IQ sampling spectrometer firmware and software design and discuss the latest test results.

2 System Architecture of Digital Backend

The general-purpose digital backend system we designed has a modular structure. Figure 1 shows the backend system designed for the Redshift Receiver of Large Millimetre Telescope (LMT) as an example to demonstrate the structure of the common backend system design. The backend system mainly includes a down-conversion module and a digital module.

The down-conversion module converts the RF signals from the existing electronics to IF and from single RF signal to in-phase and quadrature components. The applications of the backend system have different operating fre-

quency bands. For each of the applications, only the down-conversion module needs to be slightly altered. In most of the of cases, the change required can be as simple as re-programming the frequency synthesizers, which generate the local oscillators (LO) frequencies.

The digital module is implemented with RFSoC based commercial boards and custom designed anti-aliasing low-pass filter. The integrated ADCs in RFSoC are configured to sample at 4.096 GHz. The digitized signals are processed in real-time by using the FPGA fabric within RFSoC chip. More details of the signal processing will be discussed in the following section. For each of the application, no changes is required for the digital module. Based on the bandwidth of the application, the number of the digital modules required can be determined. For example, the Tulancigo telescope only needs one digital module to cover the whole bandwidth for both polarizations, while the Redshift Receiver of LMT needs 12. In general, the common backend structure will make the components for all the applications shareable, which can significantly simplify the development processes across projects.

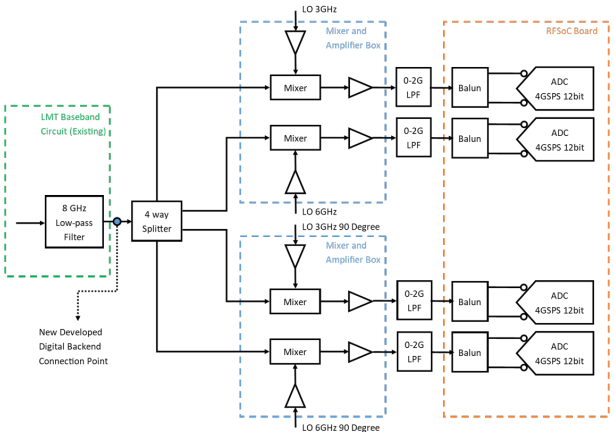

Figure 1. Digital backend system level layout

3 The KRM-4ZU27DR Board Data Converter Performance Evaluation

In [1], the performance of ADCs integrated in RFSoC have been characterized by using Xilinx ZCU111 evaluation board. The interleaved spurs, dynamic range, intermodulation distortion and other parameters calculated by ADCs on ZCU111 evaluation board are close the device specification of RFSoC and meet the requirements for radio astronomy application. The KRM-4ZU27DR board selected has complete different circuit design with ZCU111 board, which can make a significant difference in the performance. The spurious free dynamic range (SFDR) of an ADC can indicate it overall performance. The SFDR plots at frequencies across the Nyquist frequency of one of the ADCs on KRM-4ZU27DR board with and without take 2nd and 3rd harmonics into account are shown Figure 2. The RF test signals are generated by an Anritsu MG3692B signal generator. An anti-aliasing low-pass-filter (LPF) with 1.6 GHz cut-off frequency design in house is connected in series before the test tone is injected to the RF input port of the board. The ADC samples at 4.096 GHz and 16384 ADC samples are captured each time. Then sample captured are interpreted by using Fast-Fourier-Transform (FFT) and other data processing routines in MATLAB to calculate the SFDR values at each frequencies.

As Figure 2 shows, the SFDR is around 72 dB and 2 or 3 dB better without the 2nd and 3rd harmonics at some of the frequency. As the level of harmonics can highly depend on the signal generator used to generate the test tones, the SFDR exclude the harmonics is commonly used to specify the performance ADCs.The other ADCs have very similar SFDR values, so only one set of the test results is summarised in this case. Comparing with the measurement results in [1] and the specifications in the data sheet of RFSoC [2], the SFDR of the ADCs on KRM-4ZU27DR board is reasonably close. Therefore, the performance of ADCs and RF interface circuits on KRM-4ZU27DR board is sufficient for radio astronomy application.

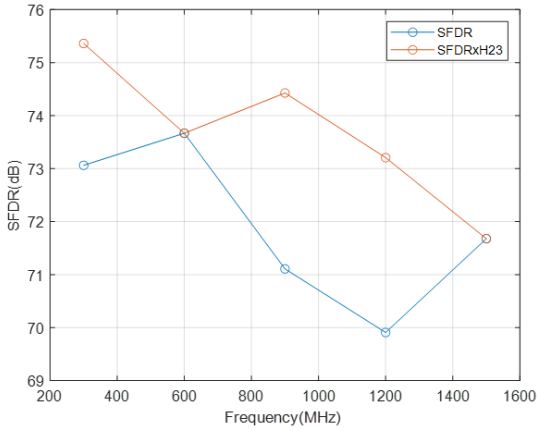

Figure 2. SFDR of ADCs on KRM-4ZU27DR Board

4 IQ Sampling Spectrometer Development

The IQ sampling spectrometer is the core component of the backend system. In this section, the firmware and software architecture of the spectrometer will be described and the test results of the implemented design will be discussed. We have observed issues with the DSP part of design and the issues will also be analyzed in this section. The IQ sampling spectrometer was prototyped with the Xilinx ZCU111 evaluation board.

4.1 Firmware and Software Design Architecture

Figure 3 shows the system diagram of the IQ sampling spectrometer. The IQ sampling spectrometer we implemented in this case is single-channel. The spectrometer takes the in-phase (I) and quadrature (Q) components of the down-converted RF signal digitized by a pair of the ADCs

integrated in RFSoC and calculates the spectra in real-time. The ADCs used for each pair of I and Q components are from the same ADC tile in RFSoC. In the spectrometer design, the ADCs are sampling at full speed, 4.096 GHz. In Xilinx Vivado design environment, the ADCs are represented as an IP, named RFdc. The digital samples are in the format of AXI4-streaming buses. The ADCs have the resolution of 12 bits, but padded to 16 bits for convenience of the data bus system. The AXI4-streaming buses carry the samples from the in-phase and quadrature components have a 128-bit wide data bus and clocked at 512 MHz. Those two buses for I and Q are combined to a single bus before further processing. At a clock frequency of 512 MHz, the timing requirements of the design is challenging to be met. Therefore, a FIFO is used to reduce the clock frequency to 256 MHz. The poly-phase filter bank (PFB) consist of poly-phase filter and FFT is designed and implemented by using the DSP blockset from CASPER toolflow in System Generator. The HDL netlist of the design in Simulink has been generated and then synthesized in Vivado. The synthesized netlist is exported and integrated with the FIFO, scaling and integration VHDL code in IP integrator. The entire spectrometer DSP is packaged as a single IP to be integrated with rest of block design.

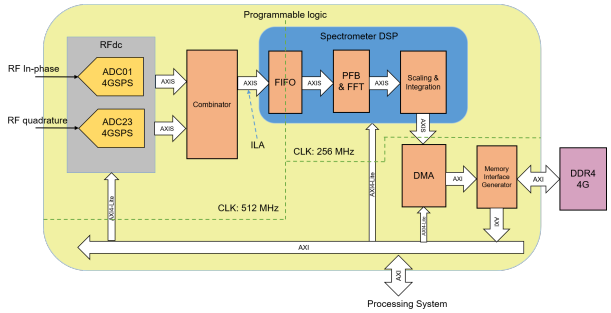

Figure 3. System Diagram of Firmware and Software Design for the IQ Sampling Spectrometer

The PFB block has 3 tabs and 12 stages. The length of FFT is 4096, so the frequency resolution of the spectrometer design is 1 MHz. The shift scheme of the FFT and the integration length and scaling factor of scaling and integration IP are all configurable via AXI4-Lite buses in software applications running in the Processing System(PS) of the integrated processor in RFSoC. The spectra data is generally integrated for milliseconds, so the bandwidth of Giga-bit Ethernet (GbE) is enough to transfer the data to the host. The integrated spectra data was converted from AXI4-Streaming protocol to memory mapped AXI protocol by using the Direct Memory Access (DMA) IP. The data is stored in an off-chip DDR4 memory to be accessed by the process applications. The Triple-Speed Gigabit Ethernet of I/O peripheral on PS side is used to transmit the data to the host. All the software applications are running on the Arm Cortex-A53 based Application Processing Unit (APU) on PS side. The applications support the operation of many parts of the system, such as off-chip clock device programming, RFSoC data converter status check, DMA data conversion, DDR4 data movement, UDP Ethernet data transmit and configuration of control registers.

4.2 Test Results and Discussions

One of the tests we have performed with the IQ sampling spectrometer implemented was to terminated both of the ADCs for I and Q. The test setup is shown in Figure 4 and the test aims to evaluate background noise level of the spectrometer. The integration time of the spectrometer has been configured to 10.24ms and the power spectra captured is shown in Figure 5. As Figure 5 shows, there are significant noise spikes starting from 128 MHz and in 256 MHz steps over the entire spectra. The noise spikes result in about 20 dB loss in dynamic range, which is not acceptable for our applications.

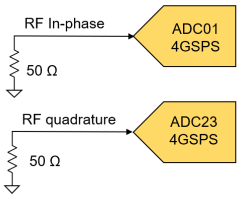

Figure 4. IQ sampling spectrometer test setup with I and Q terminated

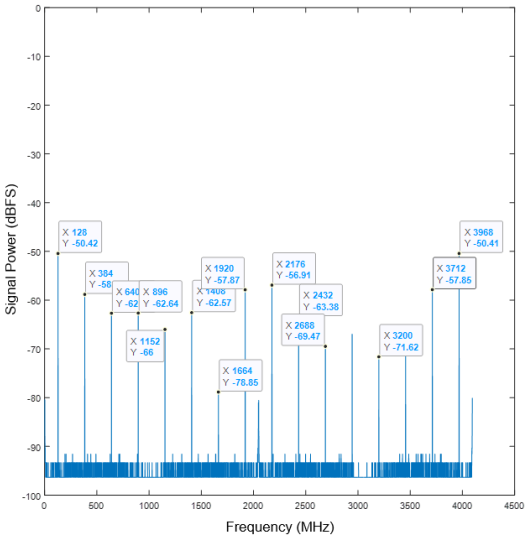

Figure 5. The background noise spectra captured by the IQ sampling spectrometer

To determine the possible causes for the noise spikes shown in Figure 5, the Integrated Logic Analyzer (ILA) was inserted as shown in Figure 3 to capture raw samples for the ADCs of I and Q components. The samples of the ADCs were captured with the test set up in Figure 4. Due to the length limit of the ILA, 131072 samples have been captured

per ADC. Then the samples are off-line processed in MATLAB with the float-point complex FFT. There are 32 consecutive FFT windows with length of 4096 and the power spectra calculated for all the windows is integrated. Then the integrated spectra is normalized spectra and shown in Figure 6. The spikes in this case are significantly lower than the spikes in Figure 5. The frequency of the spikes in Figure 6 are started at 512 MHz and in 512 MHz steps. Those spikes are mainly caused by the interleaved spurs of the ADC itself, which was observed in [1] as well. Therefore, the high background noise spikes observe in Figure 5 can be mainly attributed to the DSP part of the IQ sampling spectrometer rather than the performance of ADCs.

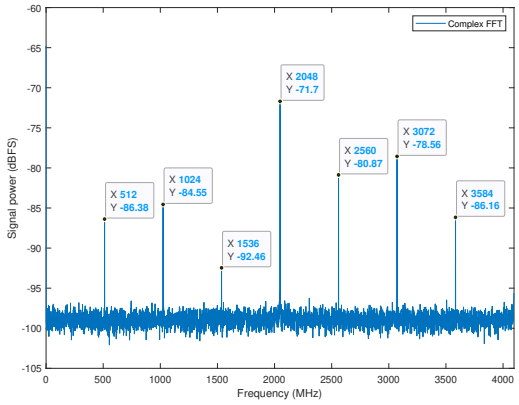

Figure 6. The background noise spectra calculated with raw ADC samples

The sample mis-alignment between the ADCs of I and Q components introduce by either the sampling process and the handling of the data buses can contribute to the noise performance of the IQ sampling spectrometer. The effect of mis-alignment between ADCs maybe not noticeable with the background noise test setup in Figure 5. To determine the alignment level between the ADCs, the test circuit in Figure 7 has been used. A test tone at 128 MHz is generated by the Anritsu MG3692B signal generator and divided by a 2-way power divider. The divided signals are injected to the ADCs for I and Q components. In Figure 8, 64 samples from each of the ADCs are plot on top of each other. As Figure 8 shows, there is only an extremely marginal lag between the samples from the ADCs. The lag might be mainly caused by the mis-match between the cable lengths or PCB track lengths for RF signals. Therefore, the background noise spikes can be isolated to the DSP part of the the IQ sampling spectrometer.

The PFB block is the most complicated DSP part of the spectrometer. There was timing issues at the beginning of the design process and the timing issues were resolved by adapting the figuration for PFB block, adjusting the interface VHDL code and updating the version of place and routing tool from Xilinx. Non of those really resolved the high background noise level. It might the case that the bug was introduced at place and routing stage, which is extremely to be localized and fixed. Therefore, FFT block will be replace by the FFT in super sample rate (SSR) block set in System Generator. The blocks in SSR block set can process multiple sample per clock cycle and that makes the implementation of high throughput data process much simpler.

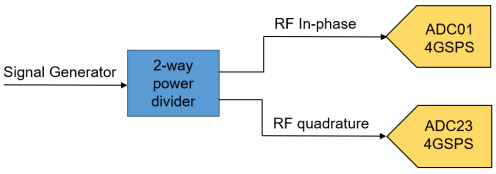

Figure 7. ADC alignment test setup

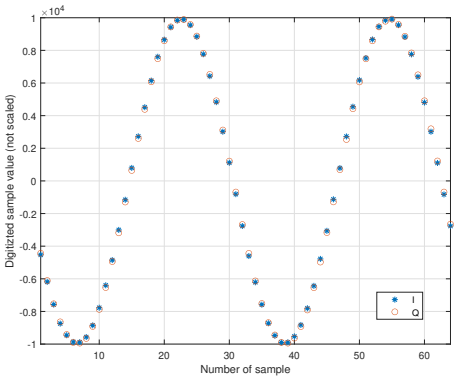

Figure 8. Raw samples from I and Q ADCs

5 Conclusions

We have designed a general-purpose backend based on the Xilinx RFSoC device. The modular system architecture makes it simple to implement backend system for centimetre and millimetre-wave telescopes with different bandwidth. The firmware and software designed for RFSoC can be reused across different applications and that can significantly shorten the design cycle of backend systems. There are issues we experienced with implementing the IQ sampling spectrometer and mainly down to the DPS design. There are various options we have in implementing the DSP part. Once we got a well-performed design, it will be quite swift to scale it up to backend systems of telescopes.

References

[1] Chao Liu, Michael E Jones, Angela C Taylor, "Characterizing the performance of high-speed data converters for RFSoC-based radio astronomy receivers," *Monthly Notices of the Royal Astronomical Society*, **Volume 501**, Issue 4, March 2021, pp. 5096–5104, https://doi.org/10.1093/mnras/staa3895.

[2] Xilinx,"DS926: Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics," *Zynq UltraScale+ RFSoC Data Sheet*, January 2021.