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Time-continuous Delta-Sigma-Modulator with switchable resistors in 65 nm CMOS Technology

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Abstract

A time-continuous, 3rd-order Delta-Sigma-Modulator (DSM) with switchable resistors for applications in adaptive ADCs is presented. The DSM consists of three differential Amplifiers, one Comparator, a clock-delay-unit, a DAC-unit and several switchable resistor-arrays representing the coefficients of the DSM. Based on an external control signal, the resistors can be set to the desired value for a given clock frequency. The presented DSM is designed to operate at clock frequencies of 64, 32, 16 and 8 MHz with a supply voltage of 1.2 V. The DSM occupies an area of 576x619 µm^2 on a test chip using 65 nm CMOS TSMC technology.

1. Introduction

Power consumption of ADC is a significant topic and there are several ways for approaching it. Some of the most common solutions are scaling the power supply, currents, dimensions and clock frequency. Compromises need to be made in order to ensure sufficient performance of the ADC. Another approach is to use adaptive ADCs, which are capable of controlling their own clock frequency. Adaptive Nyquist-rate ADCs were presented in [1] and [2] capable of controlling their clock frequency or their DAC-step-size correspondingly.

To overcome some of the limitations of adaptive nyquist-rate ADCs, ΔΣ-ADCs were taken into consideration. The inherited high clock frequency (due to oversampling in ΔΣ-ADCs) mitigates the reduced accuracy of the converter during fast transients when the clock changes. Figure 1 illustrates this issue.

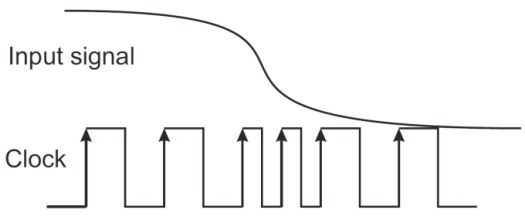

Figure 1. Change in the the clock frequency (bottom) according to the transient change of the input signal (top).

Several methods for realizing ΔΣ-ADCs with adjustable or scalable parameters ([3], [4] or [5]) were presented, though none of them were built as an adaptive ADC. In order to use an adaptive ΔΣ-ADC, a DSM is necessary, which can adjust its parameters during the AD-conversion, so that the coefficients remain same for each possible clock frequency. Time-continuous DSMs offer feasible realization opportunities by switching the resistor values in the RC-integrators. Furthermore, they allow more relaxed specification for amplifiers as well as better gain-bandwidth (GWB), allowing higher signal frequencies [6]. Therefore a time-continuous DSM with switchable resistors was selected for this work.

The paper is organized as follows: Section 2 discusses the principle of the time-continuous DSM. Section 3 focuses on the design of the building blocks of the DSM. Section 4 shows the layout of the proposed DSM as well as simulation results.

2. Model of the DSM

The time-continuous DSM was modeled using MATLAB Simulink. A 3rd-order Modulator was chosen, to have lower excessive loop delay in the modulator, while providing sufficient noise-transfer-function (NFT). The Simulink model of the proposed DSM can be seen in Figure 2.

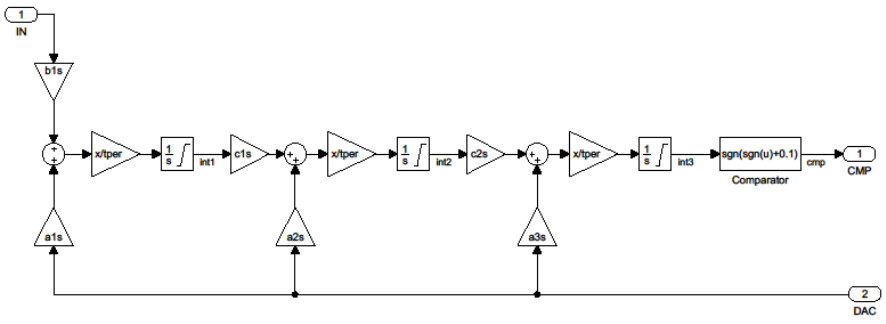

Figure 2. MATLAB Simulink model of the proposed time-continuous, 3rd-order DSM.

The integrators in MATLAB Simulink can be adjusted using a parameter. The coefficients can therefore remain constant for all possible frequencies. Only the integration gain of the amplifiers will be adjusted according to the clock frequency. The coefficients were calculated using the Delta-Sigma-Toolbox within MATLAB.

3. Design of the DSM in 65 nm technology

The 3rd-order DSM was designed in Cadence Virtuoso using the 65 nm technology from TSMC (tsmc65). The supply voltage for the circuit was set to 1.2 V . The DSM consists of three differential amplifiers, a clock-delay-unit, a DAC-unit, a comparator and 12 resistor-arrays (representing the coefficients).

The core of the DSM is built by the three differential amplifiers. Each of them builds together with two capacitances and two resistor-arrays a single RC-integrator. The amplifiers use common two-stage differential architecture with an additional common-mode control section. The goal of this additional section is to ensure that the common-mode voltage on the output of the amplifier can be adjusted and controlled using an external common-mode voltage source. The exact voltage range is temperature and corner dependent, but can be approximated to 0.4V-1.0V. Figure 3 shows the schematic of the designed amplifier and figure 4 shows a simulation result depicting the output-common-mode voltage in relation to the input-common-mode voltage.

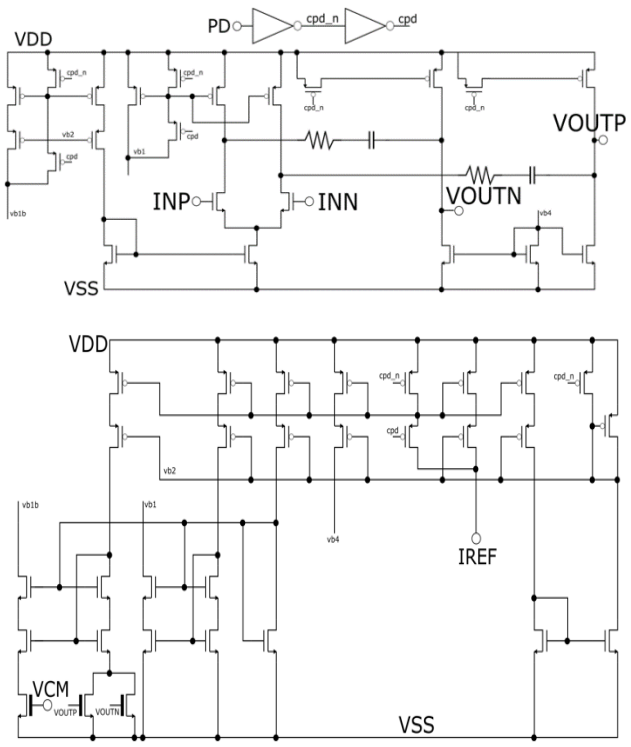

Figure 3. Schematic of the designed two-stage differential amplifier (top half) with common-mode control (bottom half).

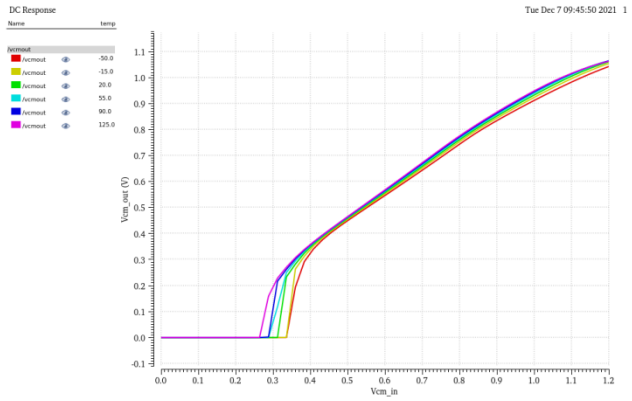

Figure 4. Simulation of the output common-mode voltage of the amplifier in relation to the input common-mode voltage. The temperature range is from -50°C to 125°C.

The three amplifiers use the same architecture, the main difference is the biasing current used (The transistor dimensions were adjusted as necessary to meet the required performance under the specific bias current).

The resistor-arrays used to set the DSM coefficients, are realized using parallel unit-resistors, CMOS-switches and inverters (to generate the complementary switching signals). Figure 5 depicts the schematic of one such resistor-array.

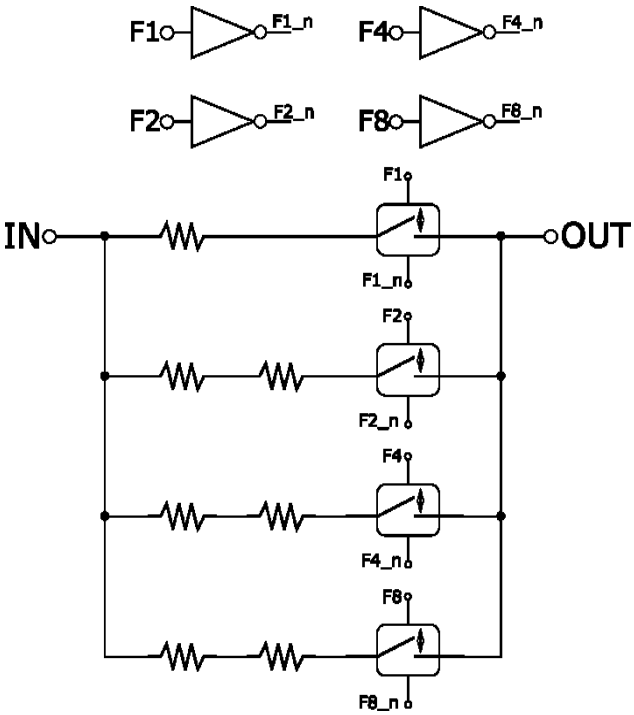

Figure 5. Schematic of one resistor-array.

Similar structure is used for all resistor arrays, only the number of unit-resistors is different to represent each of the necessary coefficients. Programmable resistors were considered, as presented in [7]. Due to the total number of the coefficients for four different clock frequencies a simple structure, as presented, was chosen.

Equation (1) was used to determine the theoretical value for the resistor for a given coefficient (Coeff), integration capacitance (Cint) and integration period (T).

$$R = \frac{Vin * T}{Coeff * Cint} \quad (1).$$

The theoretical values were then used as a starting point to determine the real values using simulation. A voltage step of 1V (Vin) was given as input and the output voltage was observed after one integration period. At that point the output voltage should be equal to the coefficient value. Figure 6 shows the schematic used for this simulation. It consists of a single differential amplifier, two integration capacitances and two resistor-arrays. Together they represent a single coefficient of the DSM.

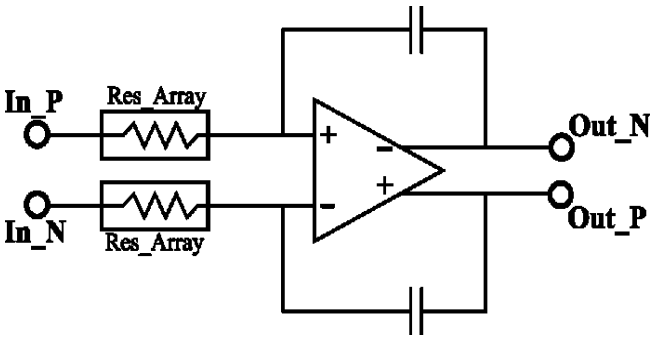

Figure 6. Schematic representing a single coefficient of the DSM.

The simulated resistor values were then further adjusted based on a fitting unit-resistance for optimal layout matching. Table 1 summarizes all resistor values for different frequencies and coefficients.

Table 1. Summary of resistor values for different coefficients and frequencies.

Coeff	64 MHz	32 MHz	16 MHz	8 MHz
0,176	16 kΩ	35,6 kΩ	75,3 kΩ	155 kΩ
0,264	10,4 kΩ	23,4 kΩ	49,8 kΩ	102,5 kΩ
0,3	23 kΩ	51 kΩ	108,2 kΩ	224 kΩ
0,439	15,5 kΩ	34,4 kΩ	73,5 kΩ	152,7 kΩ
0,6	17,2 kΩ	44,7 kΩ	102 kΩ	216,8 kΩ
0,724	12,6 kΩ	35,3 kΩ	81,6 kΩ	174 kΩ

For the comparator a "track-and-latch"-architecture was chosen, since it provides reasonably high gain, low settling time and kickback-noise. The noise was further decreased by using an additional NMOS at the input, used as a source follower. Figure 7 shows the schematic of the comparator.

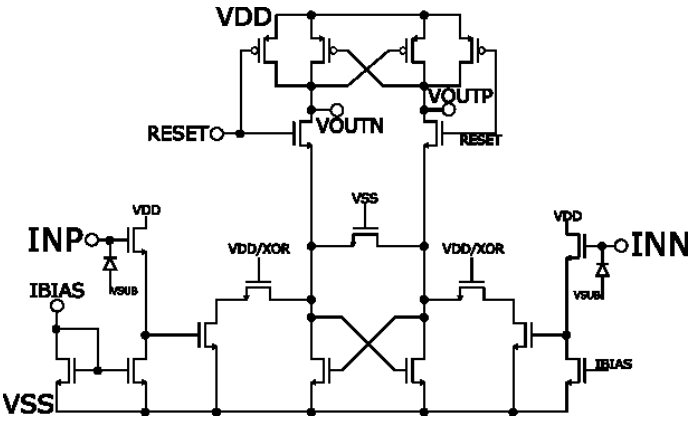

Figure 7. Schematic of the comparator.

The DAC-unit is used to generate synchronous and non-overlapping control signals for the feedback switches based on the comparator output. The Clock-Delay-unit produces a delayed clock for the DAC-unit, since, due to the settling time of the comparator the output needs a little time to reach the correct output value.

4. Layout and simulation results

The layout of the DSM was realized within Cadence Virtuoso. The amplifiers are positioned in the middle surrounded by resistor-arrays in left and right sides. The comparator, DAC-unit and Clock-Delay-unit are placed in the top. The full layout can be seen in Figure 8.

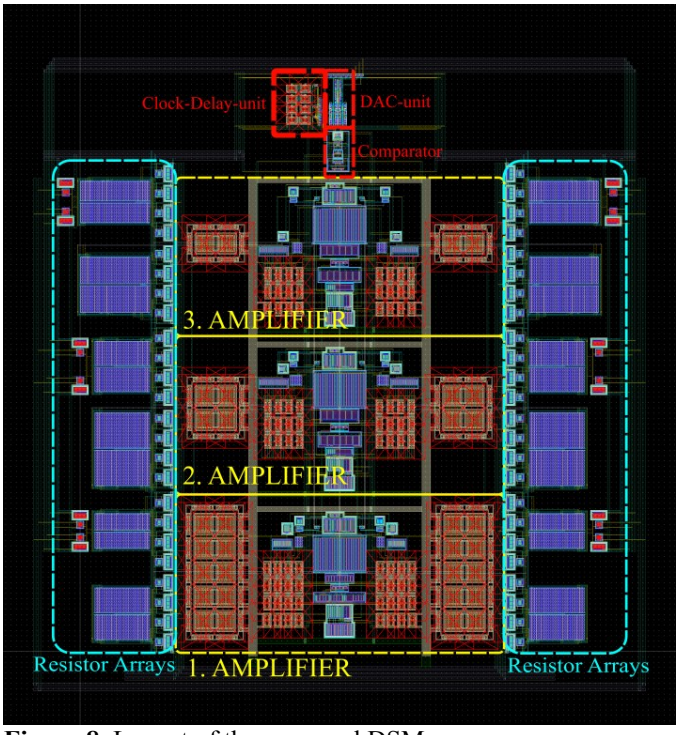

Figure 8. Layout of the proposed DSM.

A sinewave with 200 mV amplitude and 242187.5 Hz (for 64 MHz clock frequency) was used as input signal during

the simulations. The runtime for the simulation was 160 µs, resulting in 8192 samples [8]. The output-waveform was analyzed using MATLAB. Figure 9 shows the resulting SNDR of the proposed DSM (schematic only).

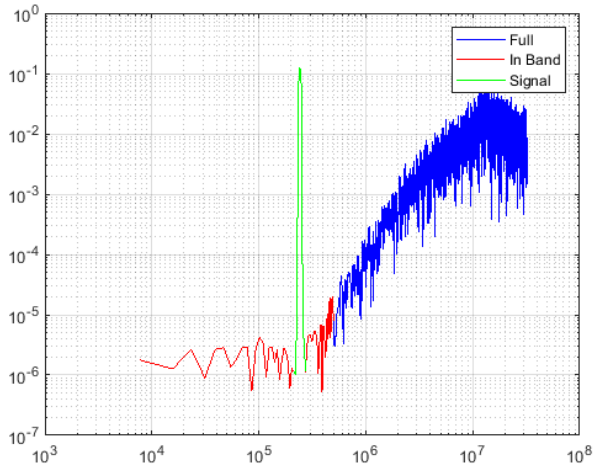

Figure 9. SNDR of the proposed DSM.

The highest achievable SNDR based on MATLAB simulation of the ideal model is 81.6 dB. The schematic of the DSM reaches 70.7 dB (Figure 9). It is important to note, that because of resistor adjustments (due to layout matching) the coefficient values differ from the ideal values. Furthermore, simulations for other clock frequencies, temperatures or with partial extractions have shown improvements up to 78.9 dB.

5. Conclusion

A time-continuous, 3rd-order DSM was presented. Thanks to the switchable resistor-arrays, which proved efficient in maintaining the coefficients for four different clock frequencies (64/32/16 and 8 MHz). Therefor, it can be used in adaptive ΔΣ-ADCs, where the clock frequency can be adapted based on the input signal and to have a lower power consumption.

References

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