3rd URSI AT-AP-RASC, Gran Canaria, 29 May – 3 June 2022

Active and continuous compensation of clock jitter in CT Delta-Sigma ADCs

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Abstract

This paper presents a new technique and circuit arrangement for reducing the influence of clock jitter in a continuous-time delta-sigma analog-to-digital converter (CT-ΔΣADC). A compensation signal is generated by successive continuous-time integration of a reference signal and is added to the converter's input for compensation. The proposed compensation circuit comprises a measuring circuit and a coupling circuit. The jitter compensation is verified on a 12-bit 3^{rd} order CT-ΔΣADC with an oversampling ratio of 64. In the end, this methodology is compared with the most popular technique from the literature and proves to be more efficient in terms of jitter compensation.

1 Introduction

Analog-to-digital converter (ADC) is a fundamental block in contemporary electronic systems. The ΔΣ ADC architecture provides high resolution without the need of high precision devices [1], making it a popular choice for low-power applications. CT-ΔΣADCs are sensitive to clock jitter, as the pulse width of the digital-to-analog converter (DAC) in the feedback loop depends on the clock edge influenced by the jitter. Noise generated by the clock jitter degrades the performance and is a fundamental limitation of signal-to-noise ratio (SNR) in a CT-ΔΣADC [2]. For a high-resolution ΔΣADC, a clock signal with very low jitter is required, otherwise, it would limit the effective resolution of a converter. It is, therefore necessary to restrain the influence of clock jitter in CT-ΔΣADC.

State of the art

Some of the most popular techniques used for reducing clock jitter effects in CT-ΔΣADCs include switched-capacitor, switched current, FIR and multi-bit DACs [3]. Switched-capacitor circuit in conjunction with a resistor (SCR-DAC), is used to compensate for the uncertainty of the DAC pulse shape due to clock jitter [4]. This method requires a short RC time constant, which increases the slew rate and bandwidth requirements. Another possibility is using a switched-current technique (SI-DAC). By discharging the capacitor into a separate resistor and controlling a current source by the generated exponential current, this technique achieves jitter insensitivity [3]. The parasitic capacitances in the current mirrors and longer recharging time of capacitors when the output current fades are the disadvantages of this method.

A multi-bit DAC architecture eases the clock accuracy requirements [5]. This is because the clock jitter contribution is proportional to the DAC's step height. As the number of bits in DAC increases, the output height is decreased yielding to a lower jitter sensitivity. But on other hand, this leads to more power consumption and limits linearity. High linearity can be maintained in multilevel DACs by using finite impulse response (FIR) DAC [3]. However, the jitter cancellation in this method is dependent on the input signal and has stability problems.

Interestingly in the prior art, few methods were attempted on active compensation of clock jitter. The basic principle was to compare the charge of a capacitor with the charge integrated by DAC reference in each clock period. A correction value is derived from comparison and is applied to the integrator's input in the subsequent clock period for compensation. In [6], SI-DAC and SC-DAC are compared, the resulting correction value is fed to the integrator one clock period later via a switched capacitor and resistor path. In [7], a CT-ΔΣ modulator with an SC-DAC uses a similar compensation method to reduce the remaining jitter sensitivity of the SC-DAC due to non-finite settling during reloading. But, using an additional switched-capacitor circuit for compensation brings in more charge injection and *kT/c* noise. Few other proposals for compensation methods such as in [8, 9] also exist, but to the best of our knowledge, they have not been implemented in practice.

2 Methodology

As discussed in the previous section, multi-bit DACs and SCR-DACs are the most commonly proposed methods for reducing errors caused by clock jitter, and they are also verified on silicon. However, multi-bit DACs are often undesirable for various reasons, after all, it is the basic idea of the modulators to use one comparator for the quantization.

In addition, the use of SCR-DAC has a disadvantage when switching from SC to CT in ΔΣ modulators. This makes it desirable to have a jitter compensation circuit that works continuously over time and manages without switched capacitance.

A time-continuous compensation circuit could also work with lower bandwidths and would have the potential to be less noisy. With all methods for jitter compensation, it is important to note that the compensation circuits themselves are also subjected to noise and therefore are an additional source of error.

2.1 Proposed compensation method

The principle is based on alternative positive and negative integration of a clock/reference signal. For an ideal clock without any jitter, there will be a uniform up and down integration as shown in figure 1a. For even multiples of T_S, the integrator always reaches the initial voltage.

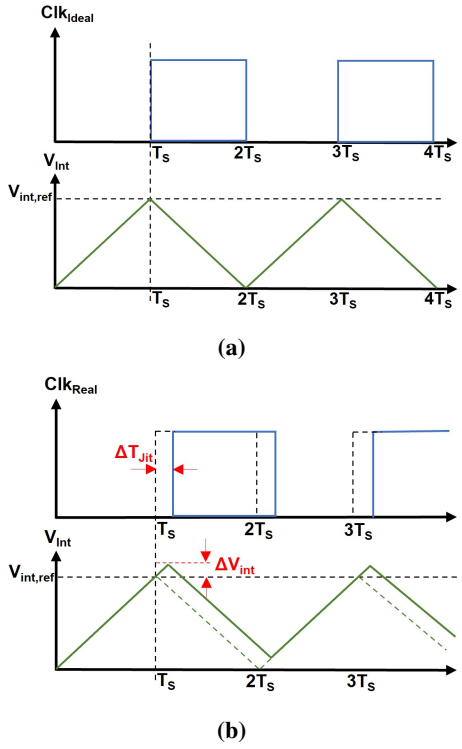


Figure 1. Integration of clock cycles (a) Ideal clock cycle without jitter (b) Clock cycle with jitter

In the case of a real clock with jitters, the clock period varies from its ideal value randomly or periodically based on the type of jitter i.e independent or accumulated jitter [11]. Up and down integration of a real clock signal is shown in figure 1b, where the integrated values fail to reach their initial position due to jitter. The deviation of the end value (ΔV_{int}) is extracted to generate a correction signal, which is fed back to the integrator in subsequent clock phases and thus compensates for the error in clock jitter. Fortunately, this technique can compensate any type of jitter irrespective of accumulative, independent and absolute jitter.

2.2 Continuous jitter compensation

The proposed technique for continuous compensation of clock jitter needs a circuit arrangement operating in parallel with the ADC. Figure 2, illustrates a possible arrangement for extraction of jitter and its compensation in a 1^{st} order modulator. The compensation circuit comprises a measuring circuit and a coupling circuit. In order to have a complete integration profile for each cycle of the system clock, a signal V_{meas} is fed as an input to the compensation circuit whose frequency is half of the system clock. The output of the compensation circuit is an error voltage V_{Err} which is applied at the modulator's input to reduce jitter sensitivity.

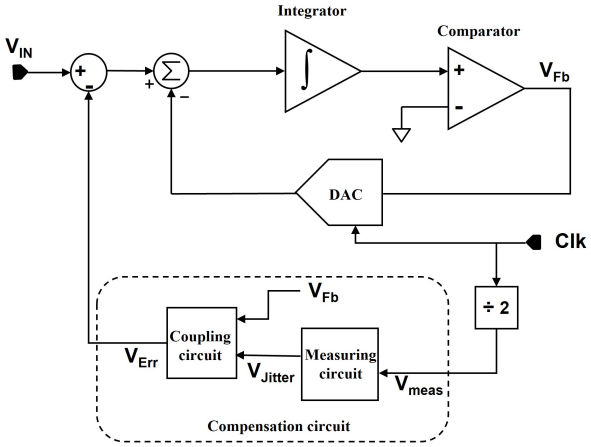


Figure 2. Circuit arrangement for continuous jitter compensation in a 1^{st} order ΔΣ ADC

2.2.1 Measuring circuit

The measuring circuit is made up of first and second switching arrangements, an integrator, delay device, sample & hold circuit and summing amplifier. V_{meas} is the input signal carrying jitter, which has to be extracted and measured. As shown in figure 3, V_{meas} controls the first switching arrangement in selecting between the reference signals $+V_{ref,int}$ and $-V_{ref,int}$. The selected signal is then forwarded to the integrator to generate V_{int}, which is further compared with reference signals $+V_{ref,dif}$ and $-V_{ref,dif}$. Since we are using a non-return-to-zero (NRZ) coding, $V_{ref,dif}$ is selected to be half of $V_{ref,int}$ considering the range for integration [10]. In case of RZ coding, $V_{ref,dif}$ would be a quarter of $V_{ref,int}$.

Due to jitter, at the end of an integration phase, V_{int} may deviate from reference limits as shown in figure 4. An integration phase preferably corresponds to one cycle of the system clock (the frequency of V_{meas} is half of the system clock). The difference obtained is directed to sample &

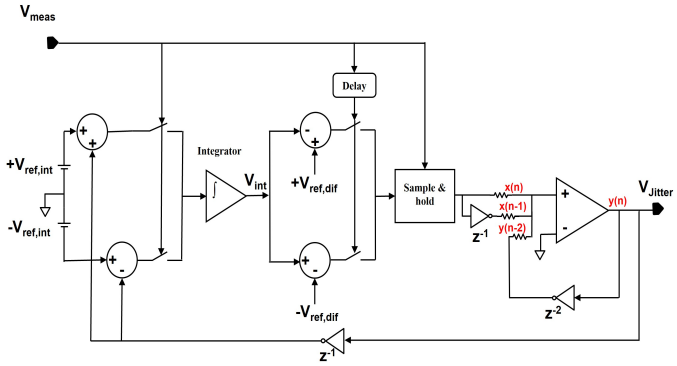


Figure 3. Circuit arrangement for measuring the clock jitter

hold through the second switching arrangement, which is controlled by delayed V_{meas}. The delay of V_{meas} is necessary to ensure that the sampling point is not at the switching time of switches [10]. The difference signal is sampled by sample & hold circuit at the edges of V_{meas}. The output of sample & hold is not only used for compensation, but also fed back to the integrator in subsequent clock phases to reset the end value of integrator after each integration phase [10]. For real applications, a delay is necessary for the feedback path and a delay of one integration phase is added. Along with this delay in the feedback path, few modifications are done in the feed-forward path ahead of the sample & hold circuit. Now the correction voltage (V_{Jitter}) is given by,

$$V_{Jitter} = y[n] = x[n] + x[n-1] + y[n-2] \qquad (1)$$

where x[n] and x[n-1] are the output values of sample & hold circuit, y[n-2] is the time delayed value of the correction voltage itself.

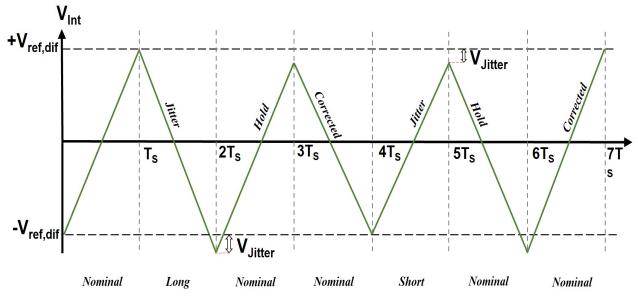


Figure 4. Integration of a jittery clock

For example consider figure 4, in the first phase where there is no jitter (nominal phase), the integrator output settles to $+V_{ref,dif}$. At the end of the second phase, V_{int} goes beyond $-V_{ref,dif}$ and this is due to the integration of lengthened clock period (long phase). This gives rise to a correction voltage (V_{Jitter}), which is held for one integration phase and then fed back in the next phase for compensation. Next, a similar observation can be seen for shortened clock period (short phase).

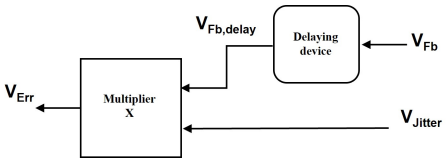


Figure 5. Generation of compensation signal by coupling V_{jitter} and $V_{Fb,delay}$

2.2.2 Coupling circuit

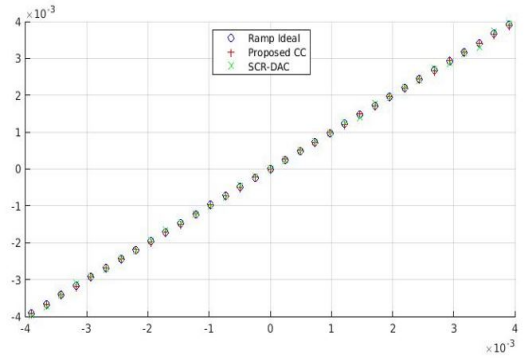
The coupling circuit consists of a multiplier and a delay device. Inputs to the coupling circuit are the correction signal (V_{Jitter}) from the measuring circuit and the feedback signal (V_{Fb}) from the $\Delta\Sigma$ modulator. The delay device delays V_{Fb} by half a period with respect to V_{meas}. This ensures that the multiplier receives both V_{Fb} and V_{Jitter} at the correct point of time, because the latter is available one clock period later from the measuring circuit. A compensation signal, V_{Err}, is formed by coupling V_{Jitter} and $V_{Fb,delay}$ using a multiplier. V_{Err} is the final output of the proposed compensation circuit, which is added to the modulator's input signal V_{IN} (figure 2) to continuously compensate for the clock jitter.

3 Results and Discussion

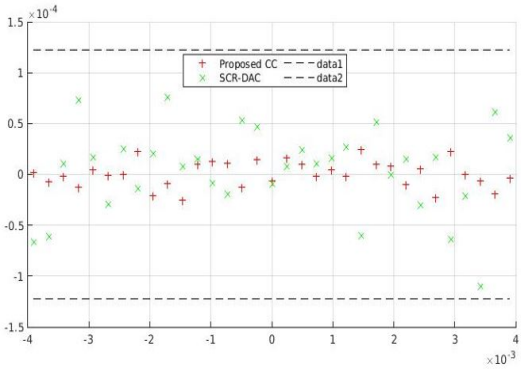
The jitter compensation capability of the proposed circuit is first examined and then compared with that of SCR-DAC. In a CT-$\Delta\Sigma$ADC, the sensitivity of clock jitter decreases with an increase in OSR [2]. On using a SCR-DAC, lowering the time constant lowers the jitter sensitivity, but lowering the time constant drastically would reduce the minimum requirement for the slew rate and gain [11]. Taking these into consideration, we use two 3^{rd} order modulators with a moderate OSR of 64 and a resolution of 12-bits. Where one uses a single bit SCR-DAC with a time constant of 5% and the other uses a compensation circuit for compensating clock jitter. A clock generator is modelled which provides a 64 MHz jittery clock signal for both the ADCs.

The circuit arrangement is modelled using MATLAB Simulink. A ramp signal is given as input to the ADCs to observe the direct current (DC) staircase waveform. Figure 6a shows the output plot of the two ADCs for the applied ramp input. It is observed that the ADC with SCR-DAC, and the ADC with compensation circuit, both follow the ideal ramp in the form of a staircase. This is a fundamental simulation to analyse the proper functionality of any ADC. A monotonic waveform at the output ensures that the converter lies within its non-linearity limits ($\pm$ 0.5 LSB). A deeper insight into the jitter compensation can be observed in figure 6b, where the staircase waveform from two compensation methods is subtracted from the ideal ramp. Minor deviations from the ideal ramp gives us the error profile of the ADC output. Since the modelled ADCs are nearly ideal except for the jittery clock, the obtained error profile can be approximated as the error due to clock jitter. In figure 6b, both the error profiles lie within the $\pm$ 0.5 LSB range. It

can be observed that with the proposed compensation circuit, higher compensation is achieved, as its error variance (σ) is less than that of SCR-DAC.



(a)



(b)

Figure 6. Simulation of modelled CT-ΔΣADCs (a) DC stair case for ramp input (b) Compensation of clock jitter w.r.t ± 0.5 LSB error

4 Conclusion

The proposed method and circuit arrangement successfully reduce the influence of clock jitter in a CT-ΔΣADC. Continuous compensation appears to be more efficient than the other popular techniques, yielding a very low error profile. The advantage of this method is the successive continuous-time integration over the clock periods, which results in a lower sensitivity to *kT/c* noise and charge injection in the compensation circuit. Next, while realising the compensation circuit on silicon, it has to be designed with precise specifications so that the circuit itself is not subjected to "significant interference and noise".

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