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Designing a low-cost DMR module for use in M2M/IoT applications

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Abstract

This paper presents the design and realization of a small, robust, and low-cost Digital Mobile Radio (DMR) module, acting as a gateway between a wireless sensor network (WSN) and an Internet of Things (IoT) center for voice communication and collection of sensors' data. The module consists of an Advanced RISC Machine (ARM) microcontroller unit (MCU), a power supply unit (PSU), and a radio frequency unit (RFU). The DMR module was successfully tested and its use demonstrated.

1. Introduction

The Internet of Things (IoT) is seen as another information and industrial wave following those of personal computers, the Internet, and mobile communication networks [1]. It will become the main driving force of the future global economic development. The worldwide IoT market will reach $1.7 trillion compared to $655.8 billion in 2014, with a compound annual growth rate of 16.9 percent [1].

Considering that the machine to machine (M2M) wireless communications infrastructure underpinning most IoT applications are low-speed, and are required in many places without a 2G/3G/4G/5G signal coverage, e.g., in a railway tunnel, underground urban complex, coal mine, etc., alternative wireless communications technologies need to be considered (both as primary backhaul but also as a back-up). The international Digital Mobile Radio (DMR) standard [2], defined by the European Telecommunication Standards Institute (ETSI), could be utilized in such cases. Nowadays, the typical 200€ price of an off-the-shelf (OTS) DMR module is too high for M2M/IoT applications. Here we propose a low-cost (~20€) DMR module design, adequate for to the M2M/IOT purpose, which is based on typical OTS components; e.g., our one uses an STM32F103 microcontroller, a HRC3000 baseband chip, and an AMBE3000 vocoder chip. The (free) Real-Time Operating System (RTOS) was used to support a multi-tasking DMR system, e.g., capable of performing different tasks, such as sensor data collection, broadcasting, configuration, etc.

2. DMR Design

The DMR hardware includes three main units, as shown in Figure 1.

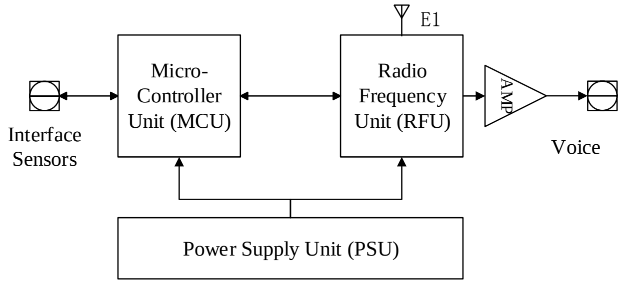

Figure 1. A high-level design of the DMR hardware.

1) *Microcontroller unit (MCU)*: The 72-MHz STM32F103 32-bit microcontroller was selected as the core 'intelligence' of this unit. It includes a 256-KB flash memory, a number of timers, analog-to-digital converters (ADCs), and communication interfaces. The 48-pin low-profile Quad Flat Package (LQFP) version, with 3.7V DC and a 3.3V DC power supply options, was used;
2) *Radio frequency unit (RFU)*: The DMR comms protocol was implemented by a HRC3000 baseband chip and a Phase Locking Loop (PLL) is used for tracking. The DMR works in the Very High Frequency (VHF) band (130-170 MHz) and Ultra High Frequency (UHF) band (400-470 MHz), and supports 16 digital channels;
3) *Power supply unit (PSU)*: A PSU utilizing a 3.7~4.2V lithium battery was designed. This is fine for both the MCU and the RFU.

3. Implementation

Figure 2 shows the schematic design of the PSU. The chipset TP4056 was selected for battery charging with 5V DC supply. The BATA (at the bottom, right) is a 3.7~4.2V lithium battery input point. The LED-RGB-0603 is a light indicator showing the battery status.

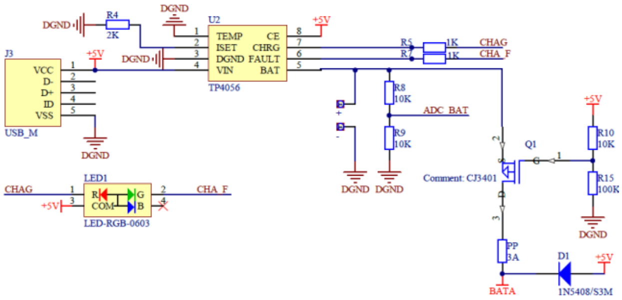

Figure 2. The PSU's schematic design.

The schematic design of the STM32F103 32-bit MCU is shown on Figure 3. It includes a number of general-purpose inputs/outputs (GPIO). For instance, the PA GPIO ports could be used for temperature sensing, J-Link software downloading, power supply, RFU's status, serial port debugging, and flash.

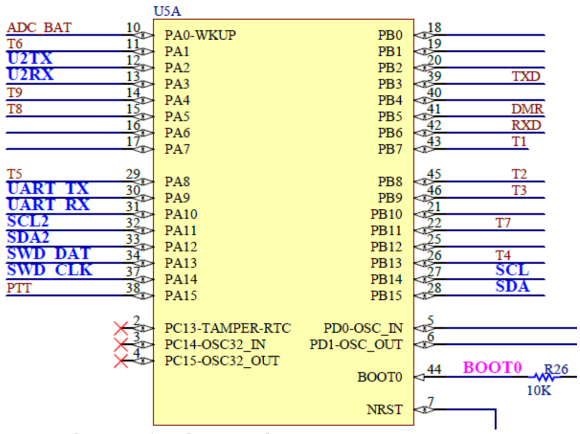

Figure 3. The MCU's schematic design.

The RFU is used for supplementary data/voice transfer in IoT networks. Its schematic design is depicted on Figure 4. It includes RX/TX ports for connection with PA9 and PA10, an ANT for connection with the antenna, and a MIX2009 chip for audio operational amplifier.

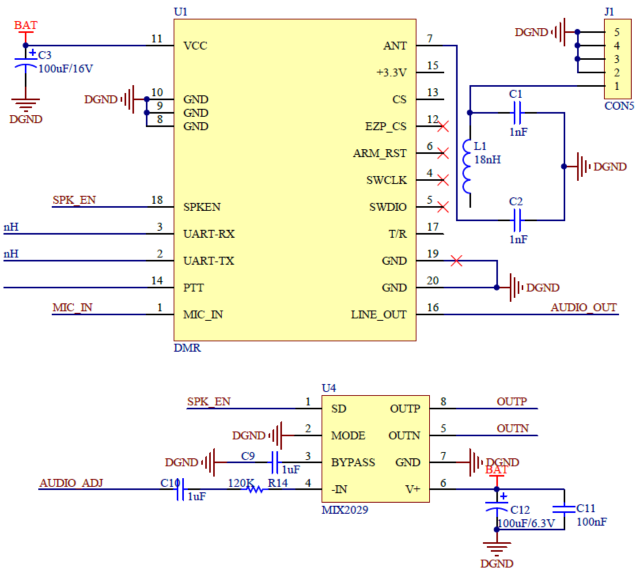

Figure 4. The RFU's schematic design.

4. Results

The RFU's PCB layout was designed with six layers, shown in the multi-colour coded schematic in Figure 5.

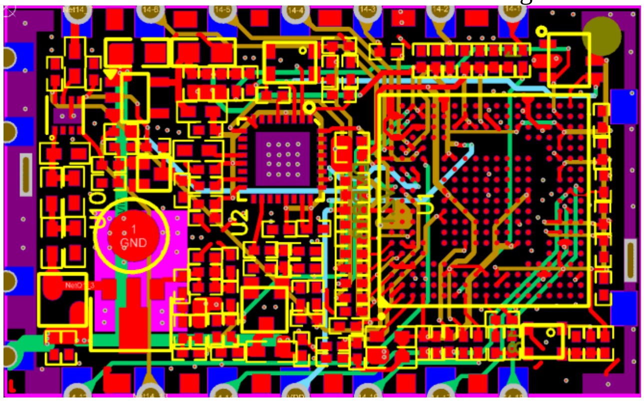

Figure 5. The 6-layer colour-coded PCB design of the RFU.

Figure 6 shows the hardware design of the described DMR module. The design meets the cost goal of ~20€. It includes 100 different electronic components. The voice communication is clear and the data communication is robust with FEC encoding/decoding algorithms.

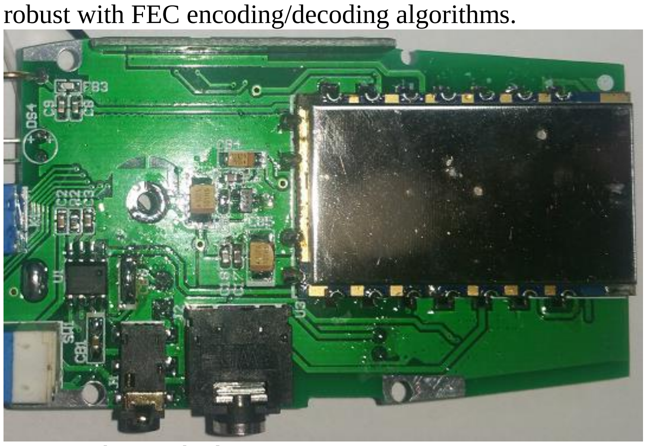

Figure 6. The DMR hardware.

6. Acknowledgements

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7. References

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