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Wideband Digital Technology for Radio Astronomy

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Abstract

As radio astronomy receiver bandwidth increases, it is necessary to increase the speed of analog-to-digital conversion (ADC) as well as the digital signal processing (DSP) in the telescope's back end. Otherwise a complex and expensive mixer-filter system is needed, to break the IF bandwidth into smaller blocks for digital sampling and signal processing. Analog-to-digital converters (ADC) capable of sample rates five gigasamples-per-second and faster are now available and DSP technology has been following Moore's law to provide matching processing power. In current wideband instruments, usable bandwidth blocks $\sim$2 GHz can be processed digitally, and we envisage a near term future where blocks $\sim$10 GHz might be handled by a single compact module. This paper reviews ultra-wideband ADC and DSP technology, and describes examples of wideband processing in radio astronomy correlators and phased arrays.

1 Introduction

In a sampled data system the width of a single block of processed bandwidth is set by the ADC sample rate through the Nyquist critereon. If the block is narrow, the processor must be preceded by an IF system with many channels; a so called "hybrid" implementation, which, if large, is likely to be cost-prohibitive. While digital technology becomes exponentially more economical with time per unit processing power, according to Moore's law, this law does not apply to analog IF electronics, which typically increases in cost over time. Thus costs of large systems—where the non-recurring cost of high performance design is amortized over many units—are reduced if they are designed with using ADCs which are as fast as possible.

It is necessary that the fast ADC chip must be matched to DSP technologies with commensurate input-output data bandwidth, and processing power. A useful technology is the Field Programmable Gate Array (FPGA). FPGAs are now equipped with asynchronous serializer-deserializer input output devices (SERDES). For the newest *GTY* series of SERDES included on the Xilinx Ultrascale+ family input-output data rates in excess of 30 gigabits-per-second (Gbps) is possible. An essential function of the SERDES is to *demultiplex* the very high bitrate from the fast ADC chip, so that the FPGA, with typical maximum *fabric* speeds of around 500 MHz, can process the data stream in real time over many parallel logic paths. The availability of this fast SERDES silicon intellectual property is one key factor giving the FPGA an edge over Application Specific Integrated Circuits (ASICs) when considered for fast DSP applications—even in relatively high volume radio astronomy applications. Another key benefit is the provision of large numbers of wide fixed point multipliers, with as many as 12,288 *DSP Slices* each equipped with one multiplier in the Xilinx Ultrascale+ VU13P DSP optimized device.

The widest radio bandwidths encountered are typically in the submillimeter region at the high frequency end of the radio spectrum. Wideband techniques are also applicable to direct-RF sampling at lower frequencies. This paper will discuss relevant technologies and techniques using, as examples, submillimeter astronomy developments.

2 The Wideband ADC Landscape

Many ADCs achieve high sample rates by interleaving multiple slower ADC cores. Distortion results from misalignment in offset, gain and phase of the cores, as well as non-linearity. It is possible to align the cores and calibrate non-linearity resulting in substantially improved fidelity. Successful wideband instruments have been designed using multicore ADCs. Still, absent other constraints, single core devices are preferred. The faster the sample rate of an ADC the greater the Nyquist bandwidth, but the ability of an ADC to handle a wideband analog signal is determined by a distinct specification, analog bandwidth. The number of bits of conversion is also key, typically, though, single core fast devices have relatively few bits. We view four bits as effectively the minimum requirements for current instrument development. In case of correlators four bits delivers 99% digital efficiency.

An important document covering the evaluation of the performance of ADCs is IEEE Standard 1241-2010 - Terminology and Test Methods for Analog-to-Digital Converters. For the noiselike signals common in radio astronomy the Noise Power Ratio (NPR) specification is of particular interest. Please see table 1 for a listing of various ADCs with sample rates 5 gigasamples-per-second and greater.

Table 1. Summary table of high speed ADC devices 5 GSa/s and greater, with relevant specifications and pricing

f_s (GSa/s)	cores	BW (GHz)	bits	Manuf.	Part #	∼cost	remarks
5	4	2.0	8	e2v	EV8AQ160	$300	ASIAA/Jiang SWARM
6.4	4	>10	12	TI	ADC12DJ3200	$2196	COTS in stock
12	1	20	4	Adsantec	ASNT7120-KMA	$800	3.5 ENOB, 2W, ZDOK
12.5		8	8	Tektronix Comp.	—	$17k	formerly Maxtek
15	1	20	4	Adsantec	ASNT7122-KMA	$1.9k	7120 w/ SERDES, PRBS
20	4/2	8	5	e2v	EV5AS210	$7k	used for NOEMA, discont.
20		13	8	Keysight	—	—	
20	1	10	3+oflow	Analog Dev.	HMC5401LC5	$2,863k	was Hittite, SAO eval. bd.
20	4/5		6	Pacific Microchip	SBIR	$3-5k	JESD204B, Esistream
25	1	22	4	Alphacore	SBIR		w/ SERDES, avl Dec 2017
34	4	20+	6	Micram	ADC3401/2	$47k	module, ADC30 old price
56	64	20	8	Pacific Microchip	SBIR	$3-5k	avl Q1 2019
56		13	68	Guzik	WDM5121	—	snapshot, 4 Gpt memory
42 - 68		25	10	Jariet	Williamson ADC	$??	ASIC IP macro only, NDA
56	320	15	8	Fujitsu	Robin/Blackbird	$20k	CHAIS, Vadatech

3 Case Study: SWARM

An example of the current state-of-the-art is the SMA Wideband Astronomical ROACH2 Machine (SWARM) [5] a 32 GHz bandwidth VLBI capable correlator and phased array designed and deployed at the Smithsonian Astrophysical Observatory's Submillimeter Array (SMA) in 2017. The SMA is an eight-element radio interferometer located atop Maunakea in Hawai'i. Eight six-meter dishes may be arranged into configurations with baselines as long as 509 m, producing a synthesized beam of sub-arcsecond width at 345 GHz. The SMA has in the last two years expanded the bandwidth of its receiver sets to 8 GHz in each sideband. Dual polarized receivers can be operated simultaneously in a single band. Counting both sidebands and both polarizations, the total bandwidth of the SMA is 32 GHz. This sets the most fundamental and demanding requirement for SWARM, that the instantaneous processed bandwidth match the aggregate bandwidth of the receivers.

Figure 1. Plan view photo of the ROACH2 platform configured for SWARM. Two 5 GSps Quad Core ADCs are plugged into connectors towards the bottom, providing samples at a data rate approaching 80 Gbps. Eight 10 GbE ports on the mezzanine board towards the top provide matched data rate throughput to the network switch. Photo credit: Derek Kubo.

The four core 5 GSa/s e2v EV8AQ160[1] has been studied in depth [1]. The device provides register controls to align the cores to reduce the impact of spurs which arise due to misalignment in offset, gain, phase (OGP), or threshold Integral Non-Linearity (INL). All the cores are clocked by the same external clock input. The quad 1.25 GSa/s interleaved mode has an equivalent sampling frequency of 5 GSa/s. A Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) [2] compatible printed circuit

[1] `http://www.e2v.com/resources/account/download-datasheet/2291`

board is available based on this ADC, designed by Jiang et al. [3]. Reference [1] details how the OGP and INL corrections are derived, and Fig 2 shows the autocorrelation spectra obtained with one of the ADCs, and the improvement obtained using core alignment.

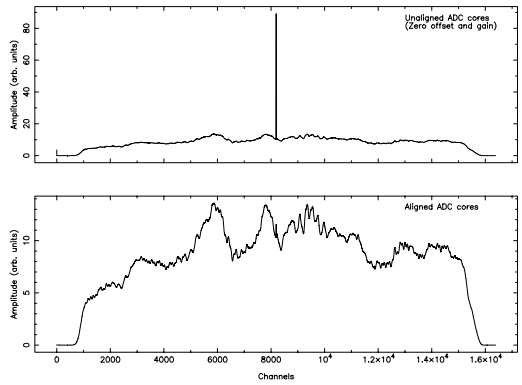

Figure 2. Autocorrelation spectrum obtained from one of the ADCs, over a 30 second integration. The top panel shows the spectrum with the offset and gain parameters set to zeroes, for the four cores of the ADC. It shows a strong spur near the center, and a weaker spur in the first channel. The bottom panels shows that setting the offset and gain values removes the spurs effectively.

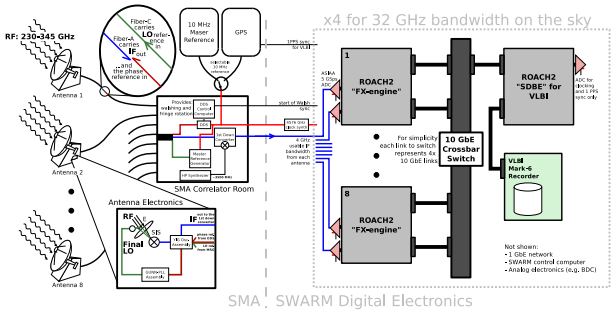

Figure 3. Block diagram showing at the top level a quadrant of SWARM, on the right of the dotted line, in the context of legacy SMA systems on the left. There are eight ROACH2s on the left of the 10 GbE crossbar switch, which contain F- and X-engines, as well as coarse and fine delay tracking, phase control and deWalshing, a phased array summer, visibility accumulator, network logic, and assorted transposes and other memory. On the right hand side of the switch is shown the "SDBE" and Mark6 data recorder, both required for EHT VLBI.

The SWARM sample rate of 4.576 GHz results in an approximately 2.3 GHz Nyquist bandwidth, with the upper edge of the usable 2 GHz band at 2.15 GHz. While the bandwidth of the *e2v* ADC in the data sheet is 2.0 GHz, our frequency response measurements show that the device responds beyond that limit, with the attenuation at 2.15 GHz about 6 dB (including any loss on the PC board). A sample rate of 4.6 GSps is within the maximum specified rate.

CASPER pioneered the use of a commercial Ethernet switch as DSP interconnection fabric [6]. Data is packetized prior to transmission via Ethernet switch "crossbar" from F-engine to X-engine and to VLBI recorders. SWARM [5] uses this approach to integrate two instruments: a correlator with 140 kHz spectral resolution across its full 32 GHz band, used for connected interferometric observations, and a phased array mode [7] used when the SMA becomes a station in the Event Horizon Telescope (EHT) Very Long Baseline Interferometry (VLBI) array.

For each SWARM quadrant ROACH2 units, see Figure 1, shared under open source by CASPER are equipped with a pair of ultra-fast Analog-to-Digital Converters (ADCs), a Field Programmable Gate Array (FPGA) processor, and eight 10 Gigabit Ethernet ports. A VLBI data recorder interface designated the SWARM Digital Back End, or SDBE, is implemented with a ninth ROACH2 per quadrant, feeding four Mark6 VLBI recorders with an aggregate recording rate of 64 Gbps. See Figure 3 which shows the architecture of a single SWARM quadrant at the top level, with the right hand side of the drawing showing the basic CASPER concept of processing engines organized around a 10 Gigabit Ethernet (GbE) switch.

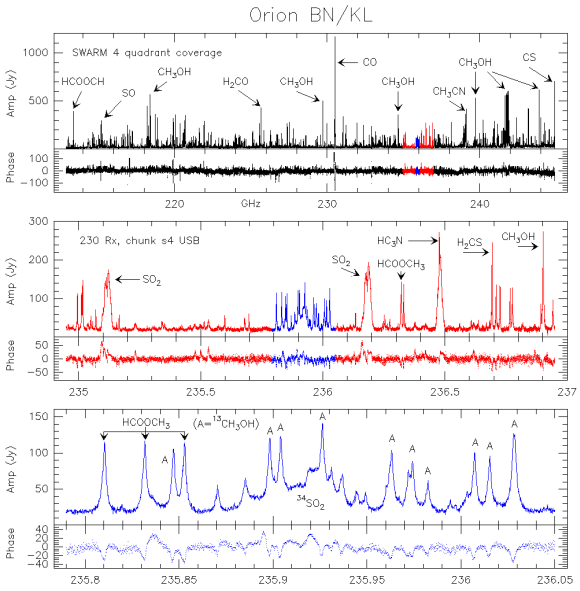

Figure 4. The spectrum of Orion BN/KL covering an instantaneous 32 GHz on the sky with 140 kHz resolution across the full bandwidth. The data were taken on 26 January 2017 UTC with SWARM. From the top the three panels show: the full 32 GHz, a single 2.0 GHz 'chunk' from one of 16 IF-ADC channels; and a detail of just over 200 MHz span, revealing the fine structure available in *all the data*—the 200 MHz blue fragment could be placed anywhere to reveal similar detail.

The developments at the Submillimeter Array (SMA) demonstrate the feasibility of ultra-wide band digital processing with fine uniform spectral resolution and VLBI capability. Figure 4 is a 32 GHz wide instantaneous contigu-

ous spectrum with 140 kHz uniform spectral resolution, an impressive demonstration of what is possible. A ROACH2 configured identically with dual 5 Gsps ADC boards is used as the primary digital back end at single dish EHT stations. The ROACH2 runs with a different FPGA bitcode or "personality", and in this mode is called the *R2DBE* [8].

4 Future Wideband Systems

An upgrade of the SMA designated *wSMA* envisions a quadrupling of the present 32 GHz SMA bandwidth to 128 GHz. This is achieved by a further doubling of bandwidth in each sideband to 16 GHz, two polarizations, and the new feature allowing two simultaneous receiver bands active (230 and 345 GHz). wSMA hinges on significant advances being made in wideband receiver design, and the availability of a dichroic plate to split the receiver bands. A back end to support the wSMA bandwidth without an increase in the number of analog IF channels—presently 32 across the eight antennas and two polarizations—is currently under development. The plan is to expand the sampled contiguous usable bandwidth to 8 GHz per block. This is on the margin of the devices listed in Table 1.

A single core 26 gigasample per second (GSa/s) 3-bit ADC is commercially available from Analog Devices Inc (ADI). Using this device 3-bit 20 GSa/s conversion with data captured by the Xilinx Virtex 7 XC7VX690T Field Programmable Gate Array (FPGA) has been demonstrated [4]. That this device is only 3-bits plus overflow is a fly in the ointment, and *sparkle code* artifacts were noticed in the output data. We are studying the ADC devices listed from Pacific Microchip, Alphacore, and Adsantec, with the Adsantec ASNT7112 being the most mature. In recent private communication with Vladimir Katzman of Adsantec an upgraded version of the ASNT7112 designated the ASNT7113 was discussed. This unit has a sample rate of 16 gigasamples-per-second, which is close to supporting an 8 GHz usable processed bandwidth but not quite there yet. Our current research is aimed at interfacing this device to the Ultrascale+ family of Xilinx FPGAs, specifically the VU9P chip, which is conveniently packaged on the economical VCU118 evaluation board.

A Cycle 3 ALMA Development Study entitled *Digital Correlator and Phased Array Architectures for Upgrading ALMA* was completed in 2017. SAO led a consortium staffed with an international group of domain experts. The team developed science-driven architectures that greatly enhance bandwidth, continuum sensitivity, fine spectral resolution and native phased array VLBI recording. Increased reliability, as well as reduced size, power consumption and life-cycle costs, are important benefits. A detailed and practical system design is documented and justified in a comprehensive ALMA technical memo[2].

[2] `https://library.nrao.edu/public/memos/alma/main/memo607.pdf`

Driven by the needs of telecommunications and other industries, FPGAs optimized for digital signal processing, with as many as ∼12,000 wide multipliers in a single chip, and ∼30 Gbps asynchronous I/O on a single serial transceiver have become a powerful and flexible technology for astronomical DSP. The use of industry-driven wideband switch as the interconnect backbone has also been validated, and faster data rates are on the road map. While a number of interesting ADC devices to support the next tier of wideband instruments have been identified it is appropriate to recognize that presently the pace of development of this key technology somewhat lags the others.

5 Acknowledgements

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