Design of High Performance CMOS Power Amplifiers for 60 GHz Applications

A. Ghiotto[(1)], A. Larie[(1),(2)], E. Kerhervé[(1)], B. Leite[(1),(3)], B. Martineau[(2), (4)], V. Knopik[(2)], L. Vogt[(2)], and D. Belot[(2), (4)]

(1) Univ. Bordeaux, Bordeaux INP, CNRS, IMS, UMR 5218, F-33400, Talence, France

(2) STMicroelectronics, 850 rue Jean Monnet, F-38926, Crolles, France

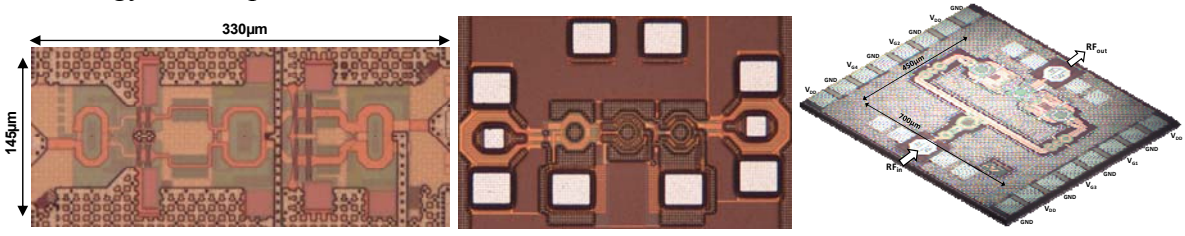
(3) GICS-UFPR, Federal University of Paraná (UFPR), Curitiba 81.531-980, Brazil

(4) CEA, LETI, MINATEC Campus, F-38054, Grenoble, France

Nowadays, wireless system data rates are limited to a few hundreds of Mbits/s due to the available spectrum limiting their bandwidth. However, due to a growing demand for very high data rate transmissions, as for example for HD video transfer or HDMI cable replacement, several standards have been proposed in the 60 GHz IMS band. With 9 GHz of available bandwidth, this frequency band is appropriate for short range multi-Gbit/s transmission. III-V technologies, such as GaAs or InP, are commonly used at such high frequencies as they provide higher performances than CMOS technologies. SiGe silicon technologies are also a good alternative to III-V technologies. However, all those technologies are too expensive with a manufacturing capacity and integration density much lower than CMOS technologies. There are therefore not competitive compared to CMOS for 60 GHz mass markets. To address 60 GHz emerging applications, most of millimeter wave transceiver parts have been recently integrated with success on the same substrate using CMOS process. Nevertheless, the integration of the power amplifier remains challenging as CMOS transistors have low gain and breakdown voltages. Furthermore a high quiescent power is inevitable to achieve high linearity required by the complex modulation scheme used to achieve high data rates.

This presentation will first introduce the considerations for the design of high-performance millimeter-wave power amplifiers based on CMOS technologies. A design methodology suitable for millimeter wave frequencies will be presented. Possible architecture and topologies, operating classes to adopt depending on the application, and the dimensioning of the various components will be detailed. The stability will be also analyzed. Finally, various stabilization techniques will be compared.

As an illustration, some recent designs will be introduced. First, two power amplifiers based on transformers in 65 nm (Fig 1(a)) and 28 nm (Fig 1(b)) CMOS technologies from STMicroelectronics will be introduced and compared to the state of the art. The study of the first circuit will focus on the bandwidth while the efficiency is optimized for the second PA. Then, a highly linear 65 nm CMOS PA shown on Fig. 1(c) will be presented. It is based on a new low-loss 8-way power combiner and achieves 32.4 dB of gain, 20 dBm of output saturated power (P_{SAT}) and 20% of peak power added efficiency (PAE). Currently, it offers the highest ITRS figure of merit among 60 GHz PAs using silicon bulk technologies. Finally, a highly linear PA based on distributed active transformer on 28 nm FDSOI CMOS technology will be presented.



(a) **(b)** **(c)**

Figure 1. (a) Pseudo-differential 65 nm and (b) 28 nm bulk, and (c) 65 nm bulk DAT CMOS PAs.