Reducing Power Consumption by Switching between Serial Mode and Parallel Mode

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Modern Field Programmable Gate Array (FPGA) is becoming favorable for designing Software Defined Radio (SDR) and Cognitive Radio (CR) equipments, because it has good performance and is providing increasingly flexibility. Several kinds of embedded processors are integrated inside FPGAs, and especially, some FPGAs support Dynamic Partial Reconfiguration (DPR) technique, which is a quite useful ability that could implement different functionalities in the same area of the device. This feature enables the implementation of multimode multiband radios in the same device, and at the same time gives the potential win of resources as well as power consumption.

Filter is a basic component for signal processing, therefore, we have implemented a FIR filter in serial mode and parallel mode respectively on Xilinx Virtex5 FPGA, and studied the power consumption of the filter when changing its working frequency. The results are quite interesting, which show that the filter consumes less power when it is implemented in serial and working at lower frequencies, but as the working frequency goes higher, the power consumption in serial mode overtakes the power consumption in parallel mode, which is because the working frequency of the serial mode is higher than the parallel mode if they have the same performance and the power consumption of the clocks becomes higher as the frequency increases.

The results are quite useful if a multimode multiband system is implemented on Virtex5 FPGA. A possible scenario is that the filter could work in GSM with the throughput 200KHz and in WiFi with the throughput 20MHz. Table I shows the dynamic power consumption of the filter with throughput 200KHz and 20MHz. In GSM, it is better to work in serial mode, which consumes 0.004W less and uses less resource than the parallel mode. But when the working standard is changing from GSM to WiFi, the serial mode consumes much more power, so it is better to switch to parallel mode by taking advantage of the DPR technique, which could save 0.106W.

TABLE I. POWER CONSUMPTION OF THE FILTER IN SERIAL MODE AND PARALLEL MODE

Throughput (Hz)	200 K	20 M
Serial	0.011 W	0.142 W
Parallel	0.015 W	0.036 W