Different strategies to improve sensitivity and power of the wake-up receivers

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Abstract - In this paper different alternatives of wake-up receiver in ultra-low power wireless sensor nodes are studied. The limitations of power dissipation, area or cost require a holistic approach to the problem, taking into account every stage of design such as the architecture and the radio frequency sub-system. Reduce data communication only when necessary can be achieved using two radios, one for standard communication as transceiver and another devoted to wake-up receiver. The wake-up receiver listens the input signal to detect the addressed bit sequence.

This work deals with the wake-up receiver design of different architectures. A comparison of the trade-off between them is performed. In each case characteristics such as sensitivity or distances with low power consumption are exposed. The input signal of the wireless sensor node is a 125 kHz on-off keying modulated at 868 MHz and the circuits are designed to operate in 868 MHz band. A first option is used a tuned radio frequency architecture with a discrete detector with Schottky diode to demodulates the OOK signal. The following structure is with an envelope detector where the envelope detector is designed in weak inversion to have a low consumption. Is possible improve the voltage gain including an impedance matching in the input of the detector. Other option is including an amplifier before the detector to improve detector sensitivity. The amplifier with active inductor has to be in subthreshold region to have moderate power consumption. The circuits are designed in UMC CMOS 65 nm technology with 1.2 V supply.