Simulation of 100 Gbps using Parallel Sequence Spread Spectrum modulation (PSSS) with 240 GHz Radio

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This paper assesses the impact of the imperfections in radio components on the delay spread and bit error rate (BER) by simulating both analog and digital domains. Parallel Sequence Spread Spectrum (PSSS) is used for physical layer (PHY) baseband technology, which considerably alleviates both transmitter and receiver design. Authors investigate the performance of the PSSS systems using a 240GHz transmitter and receiver radio. In the Mililink project [1] the 240 GHz RF (Radio Frequency) front-end was developed. The RF front-end parameters like e.g. power amplifier, mixer, striplines and low noise amplifier have been used in our baseband simulation models to emulate radio impairment losses. The BER is simulated for the PSSS modulation with several cyclic prefix and spectral efficiencies.

In our application, transmitter and receiver are used in a line of sight communication scenario with horn antennas and collimating lenses, providing a gain of 43 dBi. The delay spread depends mostly on the imperfections in radio components compared to wireless channel link. The chip-rate is set to 25 Gcps for simulating the PSSS system and using RF frontend parameter of the Millink system, simulation results shows that for a PSSS system with 1 bit/s/Hz spectral efficiency, we need cyclic extension of at least three chips to achieve a BER of 1e-4. For a PSSS system with 4 bits /s /Hz spectral efficiency, we need cyclic extension of at least eight chips to achieve BER of 1e-4.

Thus, we can infer that the length of cyclic extension depends on the spectral efficiency and length of strip lines. However, we can achieve BER of less than 1e-6, depending on system noise figure and power amplifier linearity.

[1] Millilink Project
(http://www.iaf.fraunhofer.de/content/dam/iaf/documents/komponenten/12_Produktblatt_Millilink_engl.pdf)