Design of a SiGe BiCMOS Canceller for Low Frequency Noise Reduction in Direct Conversion Receivers

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Direct-conversion receivers are increasingly employed in many applications, such as wireless communications and radars. Indeed, they represent an effective alternative to heterodyne receivers, as they allow a higher level of integration. However, performance limitations are imposed by the leakage of the local oscillator (LO) toward the RF port of the mixer (Figure 1(a)). This causes the LO self-mixing phenomenon, which is responsible of a significant DC offset at the output of the receiver (Figure 1(b)). In turn, this DC offset gives rise to a high level of low frequency noise affecting the signal recovery at baseband (R. S. Michaelsen et al., *IEEE Microwave and Wireless Components Letters*, Vol. 23 No. **2**, 2013, pp. 66-68).

In this work, a technique for lowering the DC offset has been investigated and implemented in SiGe BiCMOS technology (Figure 2(a)). The basic idea is to inject in the RF path of the receiver a cancelling signal out of phase with respect to the LO leakage, and having the same amplitude. Meeting these two conditions ensures a significant reduction of the LO self-mixing, and hence an attenuation of the DC offset at the output of the receiver.

The cancelling signal is obtained from the LO itself, which is manipulated by means of a phase shifter cascaded by a variable gain amplifier (VGA). A priori, the phase and the amplitude of the LO leakage are unknown, so the phase shifter must be able to provide whatever value over the range 0°-360°, with a fine resolution. Similarly, the gain range of the VGA has to be as wide as possible. The phase shifter is implemented as a 3-bit digital type connected with a continuous phase shifter. A cascode architecture has been used for the VGA. Tuning the control voltages of the two devices, the output DC offset can be reduced by several orders of magnitude, while the IF component remains nearly constant (Figure 2(b)).

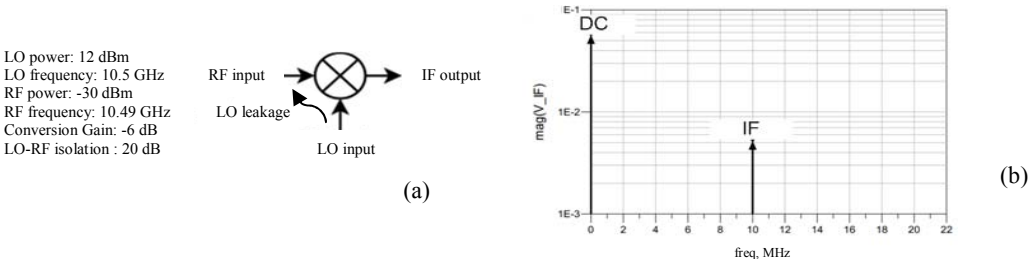

Figure 1: Mixer model with LO leakage (a), and related IF output spectrum (b)

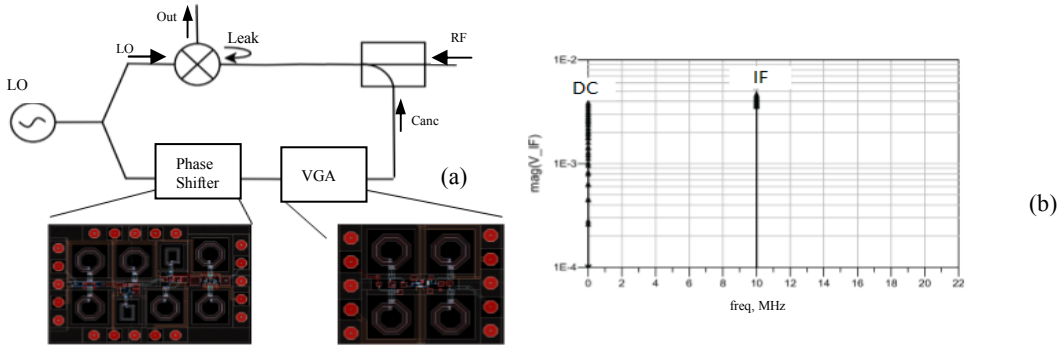

Figure 2: DC canceller with chip micrographs (a), and IF output spectrum for several combinations of the control voltages (b)