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Systematic Load-pull and Impedance Matching for Enhanced Efficiency Power Amplifier

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Abstract

This paper presents the design of a Class-E power amplifier (PA) using GaN transistor, achieving high efficiency through optimized matching networks. The proposed PA employs a systematic matching network optimization strategy to enhance power transfer and minimize losses, while utilizing a fixed bias circuit for stable operation. Measurement results demonstrate an output power around 37 dBm, a drain efficiency and power added efficiency of more than 85% and 80% respectively, and a gain of around 11 dB at 1 Ghz operating frequency, validating the effectiveness of the design. The results confirm suitability of GaN technology for high-efficiency RF power amplification, with potential applications in wireless communication and radar systems.

1 Introduction

In today's wireless communication and radar systems industry power amplifiers (PAs) play a crucial role, where high efficiency and linearity are essential for minimizing power consumption and improving system performance. Among various PA topologies, the Class-E amplifier gained attention due to its ability to achieve high efficiency by operating in a switched-mode configuration. Reduce power dissipation by reducing voltage and current overlap area at the transistor drain, makes class-E well-suited for high-frequency applications.

The advent of Gallium Nitride (GaN) technology has further enhanced the potential of Class-E amplifiers. Characteristics like Superior power density, high breakdown voltage, and low parasitic capacitances, make GaN transistors ideal for high-efficiency RF power amplification. Several studies have demonstrated the benefits of GaN-based Class-E PAs, achieving efficiencies above 80% in GHz-range applications. To ensure maximum power transfer while maintaining efficiency by optimizing the matching network remains a critical challenge.

Significant research has been conducted on Class-E power amplifiers, with a particular focus on achieving high efficiency through transistor selection, load network optimization, and biasing techniques. Early works established the fundamental design principles of Class-E operation, demonstrating its theoretical efficiency limits and practical implementation challenges. Over time, advances in semiconductor technology, particularly with GaN devices, have enabled improved performance at higher frequencies.

Several researchers in past few decades have studied GaN-based Class-E PAs, highlighting their ability to achieve efficiencies exceeding 80% while maintaining high output power. Notably, research has demonstrated that GaN transistors, such as the Cree CGH40010F, provide substantial advantages over traditional silicon-based devices due to their high breakdown voltage and reduced parasitic effects. These characteristics allow efficient switching operation, which is crucial for minimizing power dissipation [1], [2], [3].

Matching network design has been a critical area of focus in recent literature. Conventional approaches rely on analytical impedance transformation techniques to ensure maximum power transfer, but practical implementations often suffer losses due to non-ideal circuit elements. Recent advancements have introduced optimization methods that incorporate nonlinear device models and electromagnetic simulations to refine impedance-matching strategies. Studies have shown that optimized matching networks can significantly enhance overall efficiency and bandwidth while minimizing harmonic distortion [4], [5], [6], [7], [8], [9], [10].

Despite these advancements, challenges remain in designing compact and low-loss matching networks for GaN-based Class-E PAs. This work builds upon existing research by systematically optimizing the matching network to achieve improved power transfer and efficiency at 1 GHz. By leveraging complex load pull and advanced circuit modeling and experimental validation, this study provides insights into enhancing Class-E PA performance through refined impedance matching techniques.

This work presents the simulation results of a Class-E power amplifier using the Cree CGH40010F GaN transistor, focusing on matching network optimization to enhance efficiency and power transfer. Unlike conventional designs that rely on standard impedance matching techniques, this study systematically analyzes and optimizes the matching networks to minimize losses and improve performance. The proposed amplifier achieves 85% efficiency, 37 dBm output power, and 11 dB gain using a fixed bias

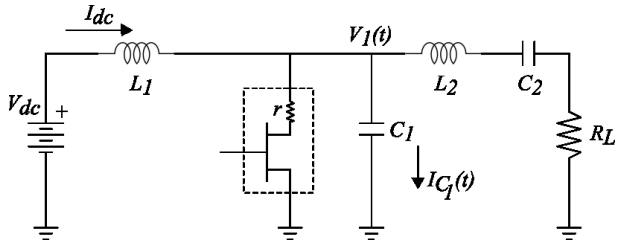

Figure 1. Class-E topology.

circuit, demonstrating its suitability for high-efficiency RF applications.

The remnant paper is structured as follows: Section II discusses related work and key literature on Class-E amplifiers and matching network optimization. Section III details the proposed amplifier design methodology, including impedance matching and circuit implementation. Section IV presents simulation and experimental results, followed by a discussion on the observed performance improvements. Finally, Section V concludes the study and outlines potential future developments.

2 Class-E PA Principle

The Class-E power amplifier is a highly efficient switch-mode amplifier topology that minimizes the overlap between the transistor's drain voltage and drain current waveforms. This technique significantly reduces power dissipation and enhances efficiency, making it suitable for RF applications. A typical Class-E PA (Fig.1) consists of: a switching transistor which operates in ON/OFF states (assumed no internal impedance), a series resonant load network (L_2C_2) to shape voltage and current waveforms, a shunt capacitance (C_1) for absorbing transistor output capacitance and shaping voltage waveform, a choke inductor (L_1) acting as a DC feed and isolating RF signals from the power supply.

In an ideal operation, the voltage at the drain of the transistor $V_1(t)$ is zero when the transistor turns on, and the current is zero when it turns off; this ensures soft-switching operation, which minimizes power dissipation. The design must ensure proper impedance matching to maintain these conditions at the desired operating frequency.

The efficiency of Class-E amplifiers theoretically can reach nearly 100% under ideal conditions, but practical factors such as parasitic elements, device non-linearities, and circuit losses reduce the achievable efficiency. By employing GaN transistors, which exhibit low parasitic capacitance and high breakdown voltage, Class-E operation can be optimized for high-frequency applications.

3 Design

The design is based on the standard Class-E topology, consisting of a switching transistor, bias networks, a load network, input and output matching networks. The key design objectives include achieving high drain efficiency, minimizing switching losses, and optimizing impedance matching for maximum power transfer. The design methodology follows the standard Class-E amplifier, ensuring that: **A.** The transistor drain voltage minimally overlaps the drain current to reduce power dissipation. **B.** The load network provides appropriate impedance transformation to ensure high-efficiency operation. For this design: the Cree CGH40010F GaN transistor is selected due to its high breakdown voltage, low parasitic capacitances, and superior power handling capability. For biasing network the amplifier employs a fixed bias circuits for gate and drain bias, to set the transistor's quiescent point, ensuring stable and proper class-E operation. The gate bias voltage $-3V$ and drain bias voltage $28V$ is chosen based on the transistor's transfer characteristics, ensuring proper Class-E switching operation. A decoupling network having quarter wave transformer is included to prevent unwanted RF feedback and maintain stable biasing. Ensuring the stability of the Cree CGH40010F GaN transistor in a Class-E power amplifier is crucial to prevent unwanted oscillations and ensure reliable operation. Stability analysis involves examining the small-signal and large-signal behavior of the transistor under different operating conditions. Stability Circles (Smith Chart Analysis) are done to identify potentially unstable regions, and the RC Stabilization Network at the input of the transistor is used to suppress high-frequency instability. A complex load-pull analysis determines the optimal load impedance that maximizes power efficiency and output power. The process involves: Performing load-pull simulations to identify the impedance region where the transistor operates with peak efficiency. Fig.2 shows the performance parameters and the source and load optimum impedance after load-pull. Harmonic load-pull techniques extracting the optimum impedance values for further matching network design are used to ensure proper harmonic terminations and minimize power losses. Matching Network Design and Optimization: The matching network designed transforms the optimal impedance found in the load-pull analysis to the required system impedance (typically 50Ω). This involves:

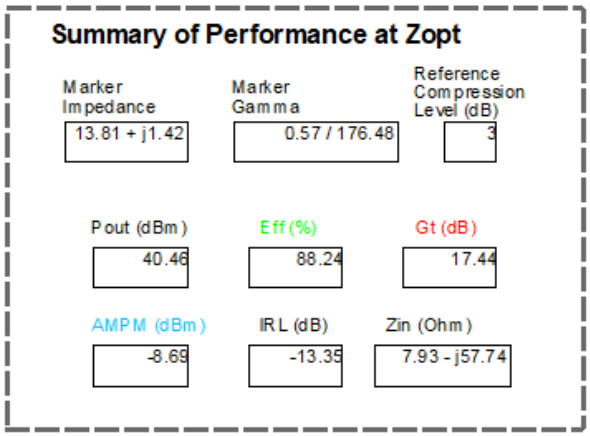

Figure 2. Load-pull Result.

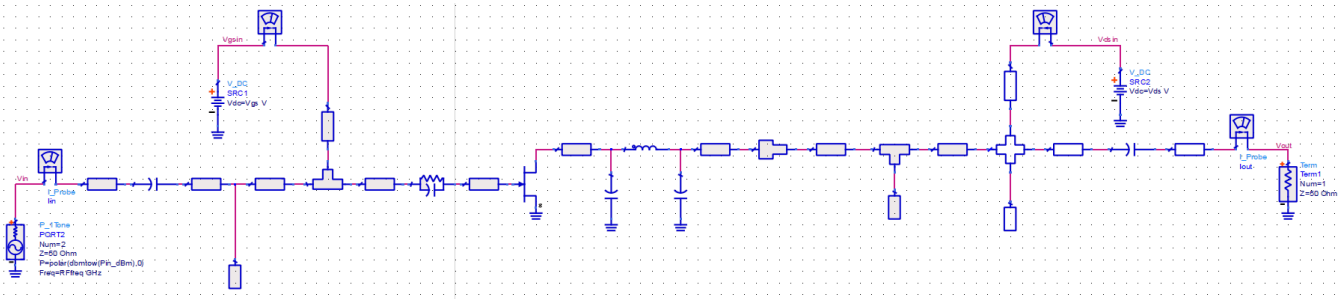

Figure 3. Simulated Power amplifier.

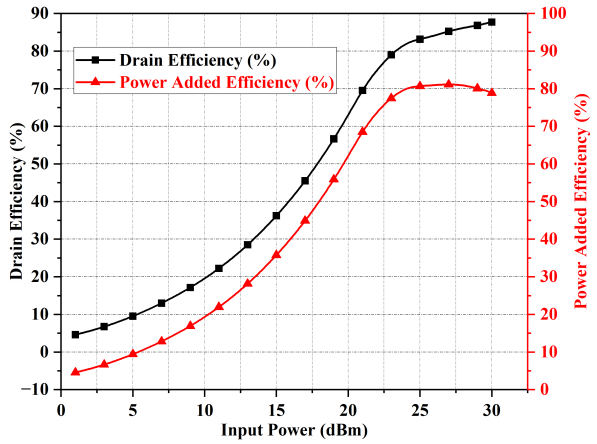

Figure 4. Variation of drain efficiency and power added efficiency with input power.

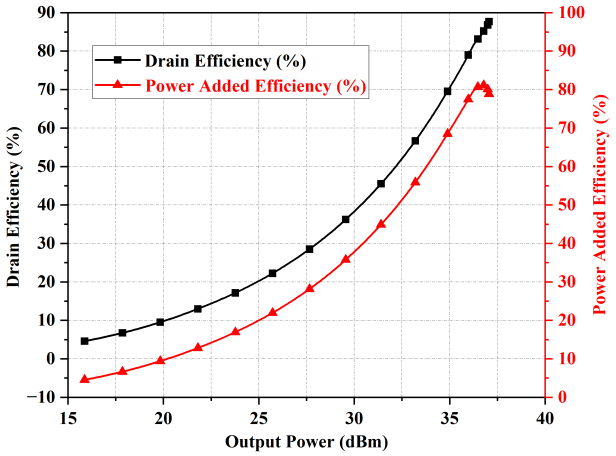

Figure 5. Variation of drain efficiency and power added efficiency with output power.

Utilizing L-section and multi-section impedance transformation networks. Minimizing insertion loss through careful selection of high-Q components.

4 Simulation Results

Evaluated the performance of designed GaN-based Class-E power amplifier through simulation. Key performance parameters, including efficiency, output power, gain, and

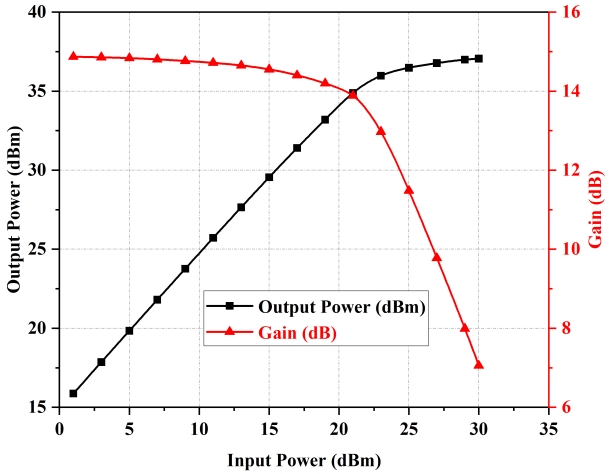

Figure 6. Output power and Gain of the amplifier

Table 1. PERFORMANCE OF PROPOSED AMPLIFIER COMPARED TO THE PREVIOUS WORKS

Ref.	Year	Freq. (GHz)	Eff. (%)	Output Power (dBm)	Gain (dB)
[2]	2013	3.6	80	37.5	NS
[8]	2018	2.14	70	43	NS
[3]	2021	2.0	82	37	10
[9]	2021	2.0	80	40	10
[10]	2023	2.6	76.8	38.9	9
This work	2025	1	85	37	11

ref: reference, Freq.: Frequency, Eff.: Efficiency.

impedance matching, were analyzed to verify the effectiveness of proposed design and matching network optimization. Fig.4 shows variation of drain and power added efficiency with input power, whereas with output power is shown in Fig.5. There is always a trade-off between efficiency and output power in power amplifier design. Fig.6 shows the output power and gain plotted with input power, and it can be seen that the PA can transfer significant power while maintaining good efficiency.

5 Conclusion and future work

This paper presented the design and optimization of a Class-E power amplifier, focusing on matching network optimization to enhance efficiency and power transfer. The proposed amplifier achieves 85% efficiency, 37 dBm output power, and 11 dB gain, demonstrating its suitability for high-efficiency RF applications. The design methodology incorporated complex load-pull analysis to determine the optimal load impedance, followed by an optimized matching network to minimize insertion loss and maximize power transfer. By systematically refining impedance matching techniques and leveraging the superior performance of GaN transistors, this study successfully improved Class-E PA efficiency while maintaining significant gain. A comparison with recent studies (Table 1) is done which highlights the competitive performance of the proposed amplifier, particularly in achieving higher efficiency while maintaining output power. These results reinforce the practical viability of Class-E PAs for modern wireless and radar applications.

The Doherty Power Amplifier (DPA) remains one of modern wireless communication systems' most crucial power amplifier architectures. With the increasing demand for high efficiency and linearity in 5G, satellite communication, and radar applications, the DPA is widely adopted due to its efficiency enhancement at back-off power levels[11]. For future research class-E amplifier designed in this paper can be possibly used as main or peaking power amplifier or both.

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