URSI AP-RASC, Sydney, Australia, 17 – 22 August 2025

A Single-Chip Wideband Digital Receiver for the Australia Telescope Compact Array Upgrade

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1 Extended Abstract

The Australia Telescope Compact Array (ATCA) is one of the three primary radio telescopes in Australia's National infrastructure for radio astronomy science. The ATCA is a six-antenna interferometer with a maximum baseline of length 6km and an observing frequency range of 1 GHz to 105 GHz. To maintain the ATCA's standing as a world-class instrument, it is in the advanced stages of a major upgrade project: Broadband Integrated GPU Correlator for ATCA (BIGCAT). BIGCAT will see the upgrade of some of the front-end RF electronics and, of relevance to this talk, the replacement of the aging Compact Array Broadband Backend (CABB) DSP subsystem. CABB [1] has been the workhorse of the ATCA for more than a decade but the hardware platform has become unsupportable, with key components such as the Xilinx Series-4 Field Programmable Gate Array (FPGA) devices reaching end-of-life (Virtex-4 discontinued in 2015).

In 2018 Xilinx Inc. (now AMD) released the first Radio-Frequency System-on-Chip (RFSoC) devices aimed primarily at military applications such as radar and electronic warfare. The evolution of these devices to the latest generation now combines multiple high-speed, high dynamic range Analogue-to-Digital Converters (ADC's) tightly integrated on the same chip with the latest FPGA fabric and IP cores, along with several conventional processor units. These RFSoC devices are ideally suited to the growing demands from radio astronomers for instruments with greater instantaneous processed bandwidth, multi-RF-channel architectures and power-efficient operation.

The digital front-end for the BIGCAT upgrade is a modular design that centers on a single AMD/Xilinx XCZU47DR Zynq UltraScale+ RFSoC device and is code-named *Jimble* in the project, see Figure 1. The Jimble is configured with four RF inputs that are simultaneously sampled at 4096 MSamp/sec. The large FPGA fabric and associated IP (BRAM, DSP48E cores, etc) in the RFSoC device is used to implement dual 32-channel polyphase filterbank channelisers that produce 16 x 128 MHz output subbands for each of the four RF input channels. The output subbands are fractionally oversampled by a fator of 32/27 to provide 80dB of image rejection at a modest increase in the output data rate. Packetised output products are streamed over two 100Gbps Ethernet connections to a network switch and down-stream GPU-based correlator. The FPGA firmware design also includes ancillary modules to provide monitoring of input and output statistics for dynamic range control and an integrating spectrometer for real-time monitoring of the output data streams.

The modular design of the Jimble digital receiver incorporates high-quality, ultra low-jitter sample-clock regeneration as well as precise timing control that ensures synchronous sampling on multiple Jimble modules across the six antenna systems from a central time and reference distributor.

In this talk, we will provide an overview of the BIGCAT upgrade and details of the Jimble hardware, FPGA firmware architecture and the software that is used to control and monitor the system. We will present the latest commissioning measurements from the Jimble processing system obtained both from lab testing and testing on the array.

References

[1] W. E. Wilson, et. al., The Australia Telescope Compact Array Broad-band Backend: description and first results, Monthly Notices of the Royal Astronomical Society, Volume 416, Issue 2, September 2011, Pages 832–856, https://doi.org/10.1111/j.1365-2966.2011.19054.x

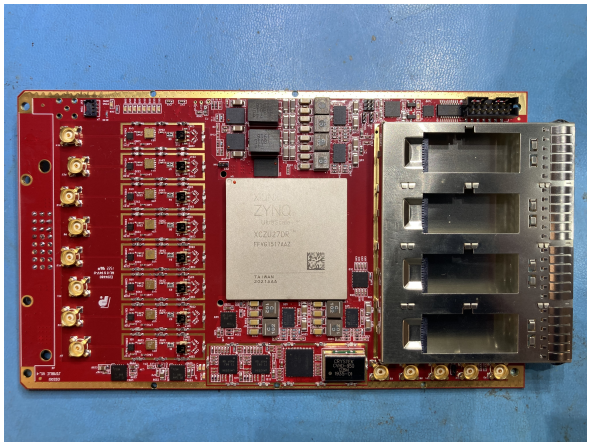

Figure 1. Jimble digital receiver module based around the AMD/Xilinx Zynq Ultrascale+ RFSoC.