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HPM-Induced Logic Hold in CMOS Circuits Featuring Industry-Standard ESD Clamping Diodes

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Abstract

Complementary Metal-Oxide-Semiconductor (CMOS) circuits are a cornerstone of modern electronic devices, but are innately vulnerable to high-energy transients. To mitigate such risks, it is industry-standard to equip CMOS logic systems with input/output periphery featuring Electrostatic Discharge (ESD) protection diodes. However, under High Power Microwave (HPM) exposure, these ESD diodes become the catalyst for a disruptive HPM-induced vulnerability: The ESD diodes rectify HPM stimuli, creating a dc offset capable of reaching the CMOS logic switching threshold. This effect, which we term 'Logic Hold', compromises CMOS circuits by forcing the input logic high during HPM exposure, thus preventing proper downstream logic functionality. In this paper, for the first time, we make a real-time observation of the HPM-induced Logic Hold effect disrupting the operation of a commercial-grade CMOS microchip processing a digital input.

1. Introduction

When High Power Microwaves (HPM)[1] illuminate CMOS (Complementary Metal-Oxide Semiconductor) logic circuits protected by unidirectional Electrostatic Discharge (ESD) clamping diodes, the circuit is at risk of HPM-induced upset [1, 2]. Figure 1.a illustrates a representative circuit where such an upset condition manifests when HPM is AC coupled to the input through a low-impedance capacitor (C).

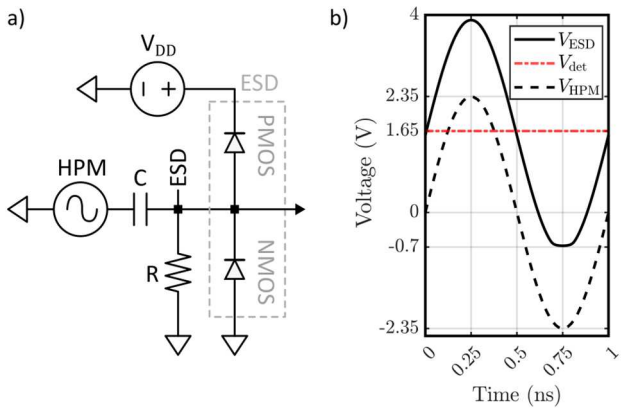

Figure 1. a) Structure S1 **b)** Probe station setup

Upon exposure, the ESD diodes rectify the coupled HPM stimulus, producing a net positive dc component referred to as 'detected voltage' (V_{det}) [1-4], which develops across the dc path provided by resistor R. If R is large, such as a typical CMOS logic pull value of $10\mathrm{k}\Omega$, and the ESD diodes are matched, V_{det} is bound by a limit of $\frac{V_{\mathrm{DD}}}{2}$, where V_{DD} is the rail voltage. The minimum peak HPM voltage ($V_{\mathrm{HPM}}\mathrm{pk}$) required to meet this condition is $\frac{V_{\mathrm{DD}}}{2} + V_{\mathrm{on}}$, where V_{on} is the diode turn-on voltage. Therefore, when an ESD protection circuit operating at $V_{\mathrm{DD}} = 3.3\mathrm{V}$ is exposed to an HPM stimulus of $2.35\mathrm{Vpk}$, and if $V_{\mathrm{on}} = 0.7\mathrm{V}$, the resulting steady-state V_{det} is $1.65\mathrm{V}$, as illustrated in Figure 1.b.

In this condition, subsequent CMOS circuitry interprets V_{det} as a valid logic high [2], overriding any logic low state present at the input. We term this HPM-induced effect 'Logic Hold', which describes a circuit state where CMOS logic is held high, preventing proper digital functionality of downstream circuits for the duration of HPM exposure. Since ESD diodes are a prevalent feature in most commercial-grade integrated circuits [6], this vulnerability represents a widespread and disruptive HPM threat.

Studies investigating this phenomenon rely on an RF network at the input to establish a low-pass node, which is necessary to interface with the CMOS input without HPM interference. While the implementation of this network has varied across studies, it has primarily been used for dc functions such as measuring V_{det} or providing a static bias, making the bias tee a prevalent choice. However, our work requires that this node also supports distortion-free square wave injection, as our objective is to observe the effects of Logic Hold as it compromises the output of a CMOS circuit processing digital logic in real time; this renders the bias tee an unsuitable choice for our purpose. The generic low-pass filter adaptation in [2] could satisfy our requirements, although the first contribution in this paper is instead to introduce an optimisation for the RF network that can be directly substituted into all prior studies known to the author, regardless of their specific focus.

The RF network that meets this design objective is a two-component CR network (shown with a $0\mathrm{V}$ bias in Figure 1.a) which offers a simple, cost-effective, and reliable solution that also converges with conventional circuit topologies. In Section 2, we demonstrate through a simulated Bode plot that this network establishes a node

[1] In this work, HPM is defined as a large-signal microwave excitation.

with a high-frequency cut-off of 200kHz when using common components ($R = 10\text{k}\Omega$, $C = 68\text{pF}$), providing the necessary foundation for the Logic Hold experiments. In Section 3, we then implement the new RF network and simulate Logic Hold upsetting the typical operation of a CMOS inverter protected by industry-standard input periphery. The model parameters provided by the foundry of our 0.35µm CMOS microchip, manufactured specifically for this study [5], are assigned to the MOSFETs to converge the simulated results with experiments. Finally, we validate the simulation with experiments on the fabricated microchip. This is performed by conducting HPM into the microchip by using a probe station and observing, for the first time, the Logic Hold effect disrupting the normal operation of an industry-standard CMOS circuit while processing a digital input. Section 5 concludes this paper.

2. RF Network

The RF network (topology shown in the Figure 2 inset) at the input of the device under test (DUT) must fulfil two key functions in our experiment: enabling efficient RF coupling and establishing a low-pass node. An individual capacitor is well-suited for the first function, as the component can be selected to provide a low impedance RF path while inherently blocking the dc return path between the HPM source and the DUT.

The low-pass node serves a dual purpose in our experiment: enabling the measurement of V_{det} generated by the ESD diodes in response to HPM, which allows us to first confirm if the resulting dc offset is sufficient to induce the Logic Hold condition. Once verified, this same port then facilitates square wave injection, ensuring the CMOS inverter is processing digital logic throughout HPM exposure. To establish the low-pass node, we use a large resistor, which functions as an open circuit when compared to the RF return path provided by the HPM source impedance (R_{sig}) in parallel.

In this work, we apply an HPM excitation at 1 GHz, which is a representative microwave frequency well-suited to our experimental setup and instrumentation. To ensure efficient RF coupling at this frequency, we selected a 68pF capacitor (C) which acts as a near short at 1GHz, presenting an impedance $\left(\frac{1}{j\omega C}\right)$ of approximately 2.34Ω. The resistor R was chosen as 10kΩ to converge on a typical value found in commercial digital logic circuits.

When $R_{\text{sig}} = 50\Omega$, this configuration delivers approximately 46dB of isolation at 1GHz, as demonstrated by the Bode plot in Figure 2. This result was obtained from an AC swept LTspice simulation of the circuit inset Figure 2, with the frequency response measured at the combination node while the source is applied to the low-pass node. With a high-frequency cutoff of approximately 200kHz, this network reliably supports digital square wave injection up to 10kHz while preserving harmonic content up to the 9th order. If higher square wave frequencies are required, then both CR component values can be adjusted, making this a practical and scalable solution for investigating this HPM effect. This CR network therefore meets all our functional requirements and is well-suited for simulation and experimentation due to its simplicity and predictable behaviour.

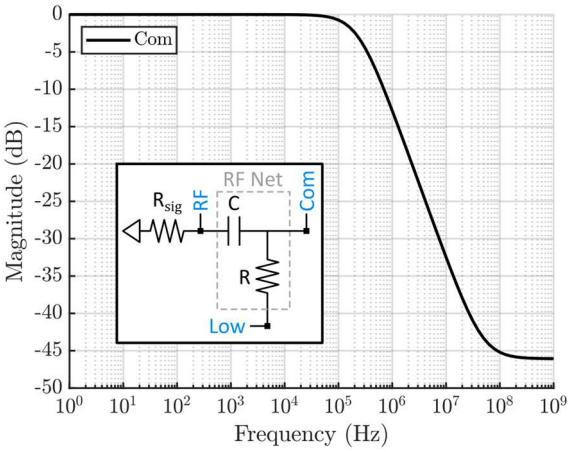

Figure 2. *CR* network Bode plot.

3. Simulated Logic Hold

The simulation schematic depicted in Figure 3 was modelled to match the front-end of the first test structure (S1, shown in Figure 6.a) of our custom 0.35µm CMOS microchip. The input pad protection of structure S1 follows the standard AMS (Austriamicrosystems) library's ICP (Input Clamp Protection) design, which includes ESD diodes and a buffering circuit. The ESD protection mechanism consists of NMOS and PMOS transistors configured as unidirectional clamping diodes, modelled using ideal MOSFETs from the default LTspice library. The logic device in S1 is the standard minimum size inverter 'Inv1' from the AMS 0.35µm CMOS C35B4C3 library [7]. The associated widths of the PMOS and NMOS of this CMOS inverter are 1.6µm and 1µm, respectively. The inverter and buffer circuits are assigned NMOS and PMOS model parameters provided by the foundry of structure S1, after fabrication of the microchip with these specifications.

The applied HPM is a 1GHz, 2.35V peak sinusoid with a 50Ω output impedance. This HPM voltage is the minimum required for V_{det} to reach 1.65 V, and hence reliably trigger the Logic Hold condition in the CMOS logic circuit shown, which has a 3.3V rail voltage (V_{DD}). The HPM signal is pulsed into the circuit for 400µs with a 225µs delay, and is depicted in the first plot of Figure 4. This pulse length was chosen to observe the Logic Hold effect over multiple digital cycles. In this simulation, the low-pass port of the RF network is configured to function in one of two mutually exclusive modes: either to measure V_{det}, or to inject a digital signal. These two operations cannot be

performed simultaneously, as each requires full utilisation of the low-pass port, making them inherently incompatible.

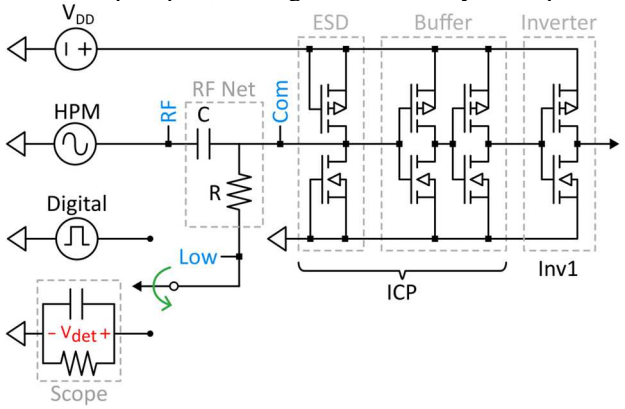

Figure 3. Logic Hold simulated circuit.

In the first mode, the low-pass port is connected to a simulated oscilloscope, modelled by a 15pF capacitor in parallel with a 1MΩ resistor. These values correspond to the high-impedance input characteristics given in the product brochure of the R&S (Rohde & Schwarz) RTO6 oscilloscope utilised for experimental measurements in a later section. The simulated V_{det} results, shown in the second plot of Figure 4, demonstrate that V_{det} rises to 1.65V during the HPM pulse.

In the second mode, the low-pass port is used to apply a digital logic signal consisting of a 3.3V, 10kHz square wave with a 50µs delay. This configuration ensures that there is a digital signal present at the inverter's input throughout the simulation, and is shown in the third plot of Figure 4.c

The Logic Hold effect, induced by the HPM pulse coupled to the input of the ESD diodes, forces the input logic of structure S1 to remain high for the duration of the pulse, irrespective of the applied digital input state. Therefore, Logic Hold disables the ability of the inverter to correctly track the applied digital input, directly resulting in a temporary logic error at the output during HPM application, as demonstrated in the fourth plot of Figure 4.

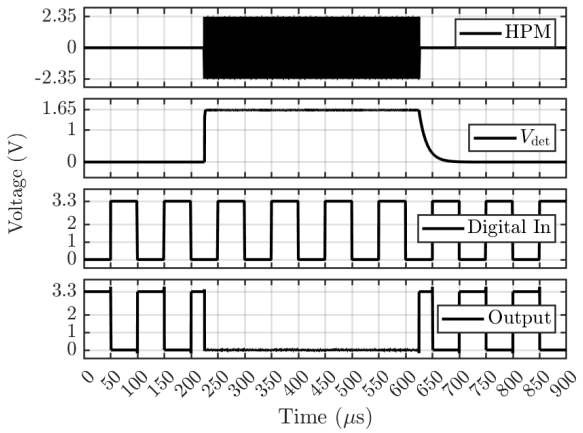

Figure 4. Simulation results from Figure 3.

4. Experimental Validation

In this section, we present the experimental results for the high-level circuit shown in Figure 5. The inverter under test is structure S1 from our custom 0.35µm CMOS microchip, captured in Figure 6.a using digital microscopy. This structure also includes BU1P (1mA output pad periphery) from the standard AMS library which completes the manufactured commercial-grade CMOS logic circuit.

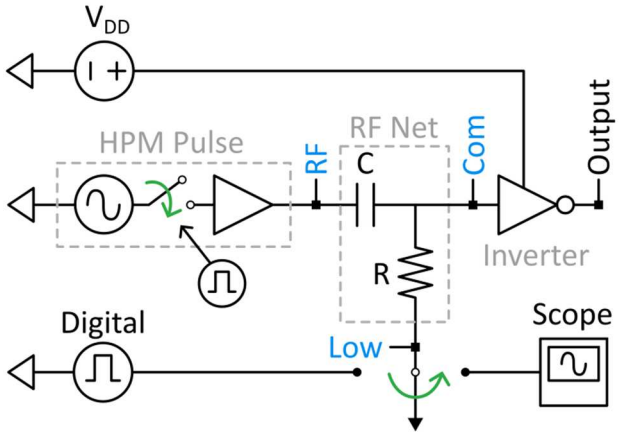

Figure 5. Logic Hold experiment circuit

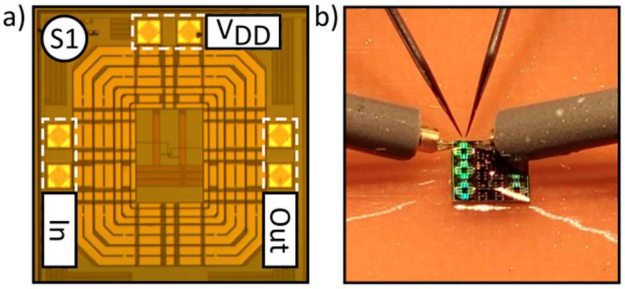

Figure 6. a) Structure S1 **b)** Microchip die under test.

To construct the HPM pulse, we used an E8257D signal generator to produce a 1GHz sine wave. The output of the signal generator is managed using an external F2932 high-speed RF switch, gate controlled by a 33604B function generator. The function generator is configured to inject a single 400µs pulse into the switch, thereby creating the desired microwave pulse length. The microwave pulse is subsequently amplified using a ZHL15W-422-S+ power amplifier, which provides a typical gain of 46dB.

The HPM pulse is conducted into the RF port of the RF network, which is built using a 68pF capacitor in parallel with a 10kΩ resistor (shown inset Figure 8), both in 0603 packages. The combination port of the RF network delivers HPM to the DUT through a C-4-RF probe station, where the probe tips interface with structure S1 of the microchip die as pictured in Figure 6.b.

We first ensured that the conditions for Logic Hold were satisfied by exposing the DUT to the HPM pulse and measuring the detected voltage (V_{det}) through the low-pass node using a high-impedance oscilloscope port. We then adjusted the output power of the signal generator until V_{det} reached the target value of 1.65V (not shown). The corresponding signal generator output power that produced this response, was $-27.3\mathrm{dBm}$.

Finally, we inject a 3.3V peak-to-peak, 10 kHz digital square wave with a 1.65V dc offset into the low-pass node of the RF network. This ensures that the CMOS inverter has a digital signal present at the input. While being subjected to HPM, the Logic Hold effect forces the input pin to remain high, thereby driving the output low throughout the duration of the HPM pulse. This manifests a state of induced logic error, shown on the oscilloscope in Figure 7, where an RF coupler was used as the primary trigger. A picture showing the complete Logic Hold experiment is shown in Figure 8.

Figure 7. HPM-induced logic error from Logic Hold.

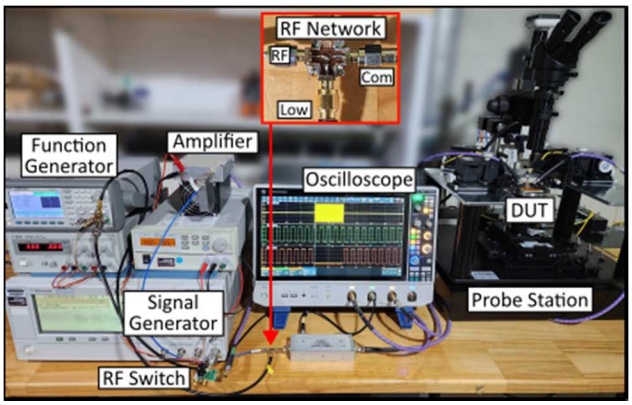

Figure 8. Full Logic Hold experiment.

5. Conclusion

In this work, we demonstrated the HPM-induced Logic Hold phenomenon compromising a CMOS circuit, with an industry-standard topology, actively processing digital logic during HPM exposure. This observation was made using the RF network optimisation that facilitates the injection of a square wave. This approach was simulated and experimentally validated, highlighting that many commercial CMOS systems relying on this common ESD protection topology may be vulnerable to this effect.

6. Acknowledgements

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