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Design and FPGA implementation of a polyphase filter bank channelizer for UWB radio astronomy

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Abstract

This paper presents the design and FPGA-based implementation of a polyphase filter bank channelizer (PFBC) for real-time channelization of ultra-wideband radio astronomical signals. The PFBC efficiently divides 4 GHz bandwidth input signal into multiple 128 MHz subband signals using a polyphase filter bank (PFB), and then packs the data for transmission to downstream computational or storage systems via high-speed Ethernet. Implemented on FPGA, the PFBC optimizes resource utilization while ensuring performance. The results from actual pulsar observation experiments validated the functionality and reliability of the PFBC.

1 Introduction

With the continuous advancement of radio astronomy research, the demand for higher sensitivity in radio telescopes is steadily increasing. As the range of observation targets becomes more diverse, radio telescopes require enhanced sensitivity to capture increasingly faint signals. Expanding the bandwidth of the observed signal is an effective approach to improving sensitivity. This imposes higher requirements on the subsequent signal processing system, which needs to perform high-speed sampling, real-time analysis, and data pre-processing with wider bandwidth, higher time resolution, and higher frequency resolution [1].

To address these challenges, channelization techniques are often used to divide the wideband signal into multiple subband signals. By adopting a parallel processing approach, these subband signals are processed and analyzed to achieve real-time processing of the ultra-wideband signal. Polyphase filter bank (PFB) is a commonly used real-time channelization method in FPGA. Hobbs et al. used an FPGA to subband the 3328 MHz bandwidth astronomical signal from the ultra-wideband receiver, dividing it into 26 subbands of 128 MHz each using a PFB [2]. Bindu et al. used PFB in an FPGA for software-defined radio to divide the input signal into 32 subband signals, enabling spectrum sensing of these signals [3].

The signal processing of the Qitai radio telescope's (QTT) ultra-wideband low-frequency receiver requires real-time division of the 4 GHz bandwidth signal into a series of 128 MHz subband signals. For this application, a polyphase filter bank channelizer (PFBC) has been designed and implemented on an FPGA platform. In the following sections of this paper, section 2 will introduce the system requirements of PFBC. Section 3 will cover the basic principles of PFB technology, and sections 4 and 5 will respectively present the hardware signal processing flow of the PFBC system and the pulsar observation experimental results.

2 System requirement

The QTT will be the world's largest fully steerable radio telescope, covering over 75% of the sky and reaching up to -40° in declination. Its early scientific focus for low-frequency bands below 4 GHz is primarily on pulsar research, including using Pulsar Timing Arrays (PTAs) to detect nanoHertz gravitational waves (GW) [4]. To achieve this, QTT's ultra-wideband low-frequency receiving system will divide signals from 704-4032 MHz into 26 subbands, each 128 MHz wide. Figure 1 shows the architecture of the entire signal processing system. The ultra-wideband signal is initially split into three analog subbands, with each processed by a separate PFBC system. The PFBC operates in two modes. The first and third PFBCs operate in Mode-I, sampling at 4096 MSps for signals in the 704-1344 MHz and 2368-4032 MHz ranges (first and second Nyquist zones) respectively. The data from each system is divided into 32 subbands, and the subbands within the target frequency range are selected for output. The second PFBC operates in Mode-II, sampling at 2560 MSps in the 1344-2368 MHz range (second Nyquist zone) and dividing the data into 20 subbands. The subband data are then packaged into VDIF format (VLBI Data Interchange Format) and Ethernet packets, which are transmitted via high-speed Ethernet to downstream storage systems for data recording, or to GPU computing systems for more refined data processing.

3 Polyphase filter bank

A digital filter bank consists of a set of M bandpass Finite Impulse Response (FIR) filters that share a common input signal, decomposing the input into M subband signals. Each subband has a bandwidth equal to $1/M$ of the

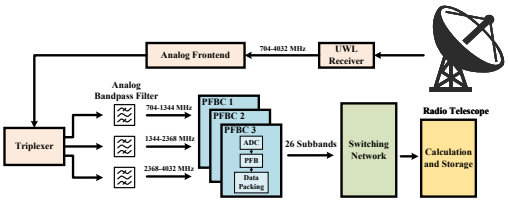

Figure 1. Signal processing system.

original bandwidth. As a result, each subband signal can be downsampled by a factor of M without introducing spectral aliasing, thereby reducing the data rate.

The computation of each subfilter is independent, requiring significant FPGA resources. Additionally, data extraction occurs after filtering, so the FIR filter's clock must remain synchronized with the original data rate, posing a challenge for hardware implementation. PFB is an effective solution to these challenges. By combining the polyphase decomposition of the filter with the Discrete Fourier Transform (DFT), the remaining filters in the filter bank are derived by modulating the prototype filter, enabling the PFB to perform a series of bandpass filtering functions [5]. Figure 2 illustrates the basic structure of the PFB.

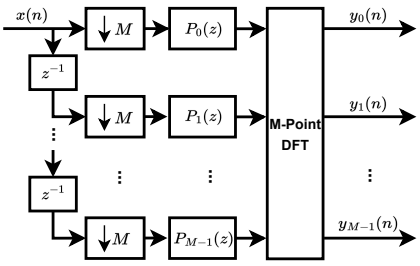

Figure 2. PFB structure.

4 Hardware implementation

In the design and implementation of the PFBC, the RFSoC chip was used. It integrates with high speed ADCs, ARM controllers, and programmble logic into a single chip. A signal processing flow diagram of the PFBC is shown in Figure 3.

4.1 Signal sampling and PFB

The signals from the radio telescope are amplified and filtered within the analog frontend. Afterward, they are fed into three analog bandpass filters through a power splitter to produce three analog subbands, which are then sampled by the ADCs in the PFBC system. The ADC delivers 8 samples of data at a time to the FPGA. For the 32-subband (Mode-I) design, the PFBC further uses a 1:4 DMUX to correctly sequence and feed the ADC data into the 32 branches of the PFB. For the 20-subband (Mode-II) design, the PFBC uses asynchronous FIFOs to buffer and align the signals to achieve the same operation. The PFBC uses a Kaiser window to design the prototype low-pass filter for the PFB. For the Mode-I design, the prototype filter order is 639, resulting in 20 coefficients per sub-filter. For the Mode-II design, the prototype filter order is 399, with each sub-filter also containing 20 coefficients. This ensures that the group delay between the digital systems remains consistent, guaranteeing the accuracy of the subband combination. These coefficients are quantized using 16-bit fixed-point representation.

The channelizer in the PFBC requires parallel DFT modules. A 32-point and a 20-point parallel DFT are needed for Mode-I and Mode-II, respectively. However DFT IP core only supports serial DFT and does not meet the parallel processing requirements. The implementation of the parallel DFT computation module in the channelizer is as follows

32-point DFT : In Mode-I type, a 32-point DFT is needed. The PFBC utilizes the Radix-2 FFT algorithm to implement the parallel 32-point DFT module. This is a commonly used approach, and therefore, further elaboration will not be provided in this paper to save space.

20-point DFT : In Mode-II type, a 20-point DFT is needed. Since 20 can be factored into the coprime factors 4 and 5, the prime factorization algorithm could be used to simplify the computation. First, the Radix algorithm is applied to remap the index n of the input sequence $x(n)$ of the 20-point DFT module. The next step is to remap the index k of the output sequence $X(k)$ of the DFT module using the Chinese Remainder Theorem, where

$$\begin{cases} n \equiv 4l + 5m \,(\mathrm{mod}\, 20) \\ k \equiv 4pt_1 + 5qt_2 \,(\mathrm{mod}\, 20) \end{cases} \tag{1}$$

Where t_1 and $t2$ satisfy $4t_1 + 5t_2 \equiv 1 \,(\mathrm{mod}\, 20)$, and here $t_1 = 4$ and $t_2 = 1$ can be selected. Then 20-Point DFT can be obtained

$$X(p,q) = \sum_{l=0}^{4} \sum_{m=0}^{3} x(l,m) W_5^{lp} W_4^{mq} \tag{2}$$

Based on Equations 1 and 2, the computation flowchart for the 20-point DFT can be derived, as shown in Figure 4. This method avoids the steps involving multiplication with rotation factors in the Cooley-Tukey algorithm. In the 4-point and 5-point DFT modules, the Winograd FFT algorithm is used in the implementation, further simplifying the computational complexity.

4.2 Data packaging and transmission

After completing the data processing, the data needs to be packed for subsequent transmission and re-analysis. The PFBC data packing uses the VDIF format. Each data packet is 8224 bytes in size, consisting of a 32-byte frame header and 8192 bytes of data. The quantization precision of the PFBC output data is 32 bits, composed of a 16-bit real part

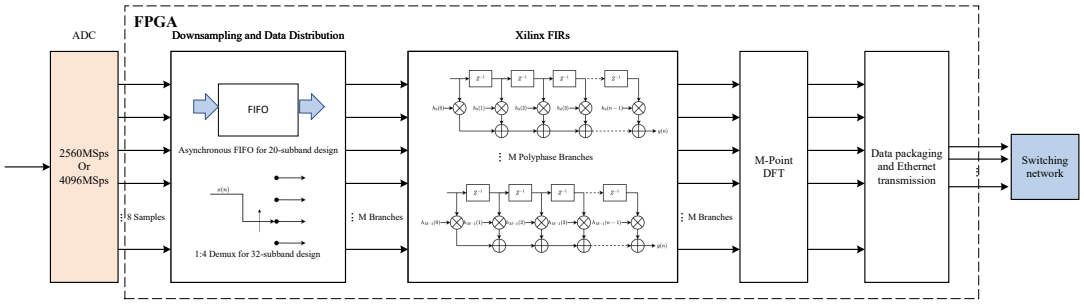

Figure 3. PFBC signal processing flow.

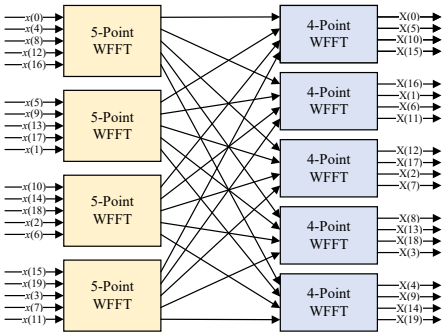

Figure 4. 20-Point DFT calculation flowchart.

and a 16-bit imaginary part. Each subband has a bandwidth of 128 MHz, with an output rate of 4096 Gbps, transmitting 62,500 VDIF data packets per second. The composition of the VDIF frame header is shown in Figure 5, with key information highlighted in red.

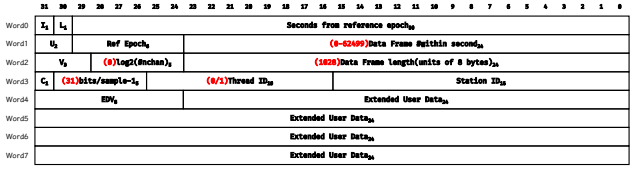

Figure 5. The structure of the VDIF format frame header.

To ensure data transmission through the switching network, VDIF data packets need to be further encapsulated into Ethernet frames. The PFBC system is equipped with eight 25 Gbps SFP28 Ethernet interfaces, and Ethernet transmission follows the 25G BASE-R standard. Ethernet frames use the Ethernet V2 format, with IPv4 at the IP layer and the UDP protocol at the transport layer. In actual pulsar observation applications, Ethernet data is typically transmitted to fixed network devices. To save design resources, the PFBC transmission directly reads and writes the target MAC and IP addresses via the ARM module, eliminating the need for logic to send and receive Address Resolution Protocol (ARP) messages. The PFBC high-speed Ethernet transmission module mainly consists of the data buffering module, data packing module, and MAC framing module, as shown in Figure 6.

The data caching module is responsible for storing channelized data and key information required for data packing, such as the signal acquisition timestamp, VDIF epoch number and epoch seconds, and the destination MAC and IP addresses of the Ethernet packet. The PFBC manages clock domain crossings by using two asynchronous FIFOs for data buffering. Once a complete VDIF data packet is assembled, the data packaging module is required to append the VDIF packet header and the UDP/IP packet header to the data packet. The MAC framing module is responsible for further encapsulating the IP data packet for transmission through the XGMII interface. It employs a state machine to handle Ethernet frame delimiters, preamble, packet assembly, and Frame Check Sequence (FCS) computation and transmission. Additionally, the module incorporates data flow arbitration to combine multiple subband signals into a single output for the SFP28 port.

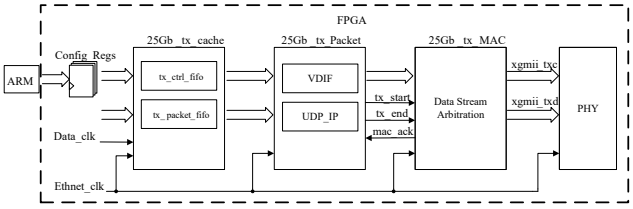

Figure 6. PFBC high-speed ethernet transmission module.

4.3 Implementation results

This design was implemented in RFSoC. The resource requirement of each mode is shown in Table 1.

Table 1. Resource utilization for one FPGA.

Operating mode	Subband number	LUTs	Registers	Block RAM	DSP48
Mode-I	32	13653	25097	4.5	1328
Mode-II	20	8872	15912	4	857

A comparison of parameters with other implementations of the PFB was also conducted, and the results are presented in Table 2.

5 Observation results

In order to validate the functionality and reliability of the PFBC system, a pulsar observation experiment was conducted in Nanshan astronomical observation station in

Table 2. PFB comparison.

Signal processing system	Input bandwith	Output channels	Subband bandwidth
PFBC Mode I	4096MHz	32	128MHz
PFBC Mode II	2560MHz	20	128MHz
Reference [2]	4096MHz	32	128MHz
Reference [3]	10MHz	32	312.5kHz
Reference [7]	62.5MHz	16	390.625kHz

Urumqi , China. Since the 704-4032 MHz analog frontend is still under construction, the L-band receiver system of the Nanshan Radio Telescope (NSRT) was used for the experiment as a substitute. The frequency range of the L-band astronomical signals is between 964 and 1732 MHz, which was subsequently downconverted to 64-832 MHz with a bandwidth of 768 MHz. It was then divided into 6 subbands of 128 MHz each by PFBC. In line with the ultra-wideband design goal, three PFBC systems were used, with sampling rates configured to 4096 MSps, 2560 MSps, and 4096 MSps, respectively. Each system was responsible for outputting two 128 MHz subbands. The data was then sent to the downstream GPU cluster for folding, dedispersion, and other processing tasks.

A 5-minute observation of the pulsar J0332+5434 was conducted. After more refined processing the signals from the 6 subbands output by the PFBC [6], the dynamic spectra for each subband are displayed in Figure 7. The dynamic spectrum of the combined wideband signal is shown in Figure 8. The pulsar profiles of each subband are accurate, and the pulsar profile of the wideband signal synthesized across subbands is precisely aligned and a finer pulsar contour waveform was given. This validates the functionality and reliability of the PFBC system, as well as the accuracy of its inter-system time synchronization.

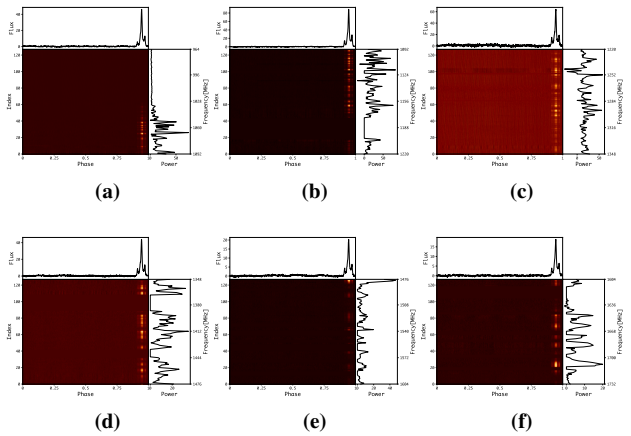

Figure 7. J0332+5434's subband dynamic dpectrum diagram.

6 Conclusion

This paper designs and implements the PFBC, addressing the real-time processing and transmission challenges of ultra-wideband radio astronomy signals. The 4 GHz bandwidth ultra-wideband signal is divided by the PFBC into a series of 128 MHz subband signals by using PFB, which are then packaged in VDIF format and encapsulated into Ethernet frames for transmission to downstream computation and storage systems. The PFBC is efficiently implemented using the RFSoC platform, with flexibility to adapt to other FPGA platforms. Actual pulsar observation results validate the functionality and reliability of the PFBC.

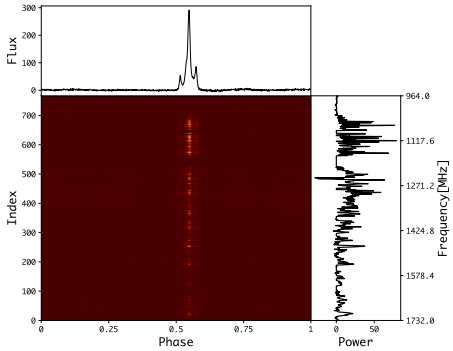

Figure 8. J0332+5434's dynamic spectrum diagram.

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