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Clock Synchronisation Architecture for the Calibration of Timepieces

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Abstract

This paper presents the clock synchronisation architecture developed at the Standards and Calibration Laboratory (SCL) for the calibration of timepieces. This architecture includes a precise reference frequency system and the development of distribution and synchronisation designs for the reference timing equipment, which ensures the accuracy and stability of elapsed time measurement.

1. Introduction

Accurate timing devices are essential to ensure reliable time measurement across a variety of applications, such as sports, forensic investigation and scientific research. The accuracy of timing devices is determined through calibration, which could be conducted through comparing the elapsed time recorded by the device under test (UUT) with that of a reference timing equipment. SCL employs the video totalize method [1] to carry out this type of calibration. The method utilizes an in-house designed synchronous counter and a commercially available high speed video camera to capture the time readings of a reference counter and the UUT. The elapsed time data is then extracted from the corresponding recorded video frames, which provides an effective way in the evaluation of the accuracy of the elapsed time of the UUT.

The SCL has defined the clock synchronisation architecture to systematically enhance the reliability of the calibration of timepieces, as illustrated in Figure 1. The laboratory time scale system [2] generates the reference frequency, and provides precise phase reference for a signal generator to generate accurate clock signal for elapsed time measurement. The reference timing equipment consists of three major components: 1) The clock signal distribution unit handles and redistributes the clock signal signals to facilitate the counting and synchronisation processes; 2) The counter unit counts the cycles of input clock and uses the counting results to calculate the elapsed time; 3) The display unit presents the elapsed time result. These components in the architecture play a crucial role and form a robust system to ensure the accuracy of elapsed time measurement for the calibration of timepieces.

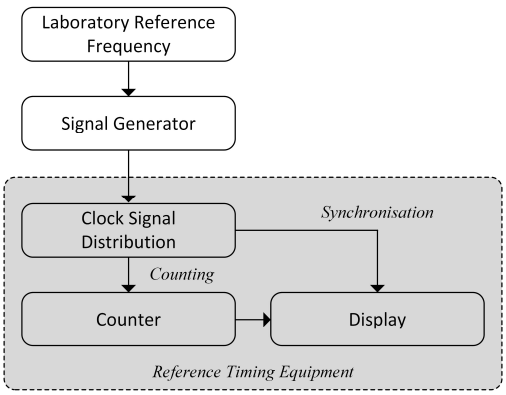

Figure 1. Component diagram of the clock synchronisation architecture for calibration of timepieces.

2. Time Data Synchronisation

The elapsed time data is represented by multiple electrical signals from the counter unit. In practice, the signals could exhibit timing mismatches along their propagation paths, which could potentially affect the integrity of the elapsed time data, especially in the measurement condition that a long elapsed time is required. A time data synchronisation process is therefore implemented in the display unit to align the timing of signals from different paths, which ensures all data signals to be simultaneously presented at a predetermined interval.

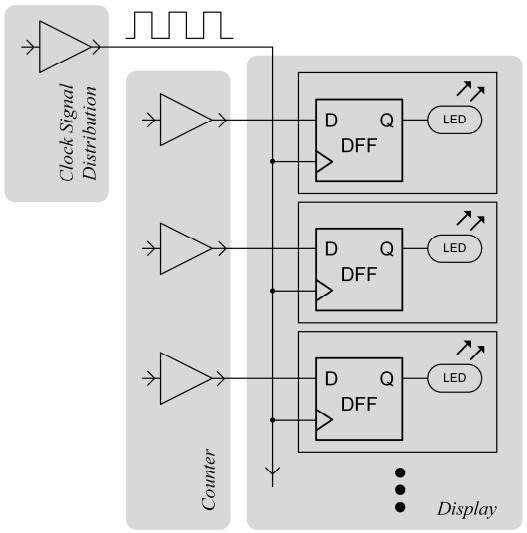

Figure 2. Simplified diagram of the time synchronisation circuitry.

The simplified diagram of the time synchronisation circuitry is shown in Figure 2. The electrical signals from the counter unit are buffered and fed to the display unit through the inputs of D flip-flops. A synchronisation clock signal, generated by the clock distribution unit, is connected to all clock inputs of the D flip-flops. Hence, all the input data are synchronised by the D flip-flops at the rising edges of the synchronisation clock, which could effectively eliminate any non-uniform time delays from different signal paths. The outputs of the D flip-flops are connected to LED devices, resulting a synchronised update of all LED's states in each counting steps. This circuitry maintains the visual representation of the elapsed time through the LEDs, which minimizes the likelihood of display errors due to timing mismatches between the data signals. The timing sequence between the data signals and time synchronisation clock is properly controlled by the clock distribution unit, which fulfils both the setup time and hold time margins of the D flip-flops. The implemented time data synchronisation in the reference timing equipment could effectively enhance the measurement accuracy, especially for long elapsed time measurement with very fine resolutions.

3. Measurement Setup

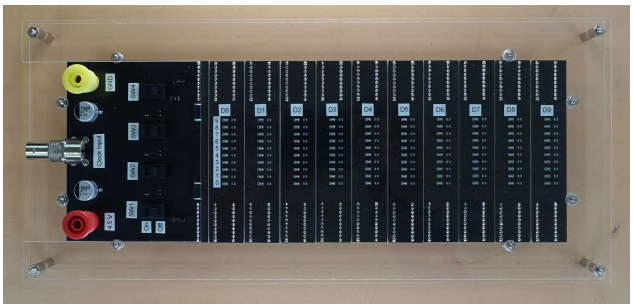

Figure 3. Second generation of the SCL synchronous counter.

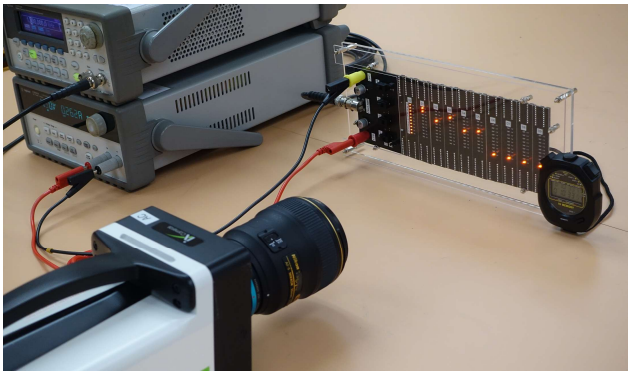

Figure 4. Measurement setup for the calibration of timepieces.

The SCL has built the second generation of the synchronous counter to realise the reference timing equipment based on this architecture. The counter is implemented with modular inter-connected features to offer flexibility, scalability and customization for the elapsed time measurement [3]. A 10-digit version is shown in Figure 3 and an example of the measurement setup for the calibration of timepieces is illustrated in Figure 4. During measurement, the signal generator is phase-locked to the laboratory reference frequency to generate a phase referenced and traceable 1 kHz clock signal, which is then phase-locked by the synchronous counter.

The built-in clock signal distribution unit provides the counting and synchronisation of clock signals and ensures the elapsed time counting is precisely performed at a 1 ms resolution with a maximum measurement range of 9,999,999.999 s, which is sufficient for many types of UUT. A high speed digital camera is set to a frame rate of 2,000 frame-per-second (fps) to simultaneously capture the elapsed time readings of both the synchronous counter and the UUT. The relative correction of the elapsed time of the UUT and its associated measurement uncertainty is evaluated using Monte Carlo Method in accordance with JCGM 101:2008 [4]. Experiments and validation have demonstrated that the measurement setup based on this architecture could effectively enhance both measurement accuracy and capability for the calibration of timepieces.

4. Conclusion

The SCL has developed a clock synchronisation architecture that effectively serves as a reference system for the calibration of timepieces. This architecture facilitates the reduction of timing discrepancies, which also provides a better resolution and enhances the system accuracy and reliability for elapsed time measurement.

References

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