Physical Insights into the Recessed Gate Architectures for High Gain Applications

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The GaN HEMTs portfolio offers reliable performance for high-power RF applications due to its high critical field and saturation velocity. GaN's intrinsic properties, such as a high direct band gap, make it viable at high temperatures. Despite technological advancements, poor aspect ratios ($L_G/t_{Barrier}$<15) degrade device performance, necessitating the adoption of gate recess techniques [1].

This work delves into the large signal analysis of GaN HEMT with recessed gate architecture. To mimic the actual behavior of the device, Silvaco's Victory TCAD simulations have been performed in accordance with the experimental devices reported by Raja *et al.* [2]. The device schematic is shown in Fig. 1(a) and the calibrated transfer characteristics at 25°C and 100°C is depicted in Fig. 1(b). The electrostatic control of the gate over the 2DEG channel increases as the gate is recessed into the AlGaN barrier. This accounts for a positive shift in the threshold voltage (-2.8 V @ 5nm recess) accompanied by an increase in the transconductance (31.57 % compared to Conventional). For evaluating the recessed gate architecture for RF applications, load pull simulations have been performed at 3 GHz for Class AB operation. Class AB operation is ensured by biasing the devices at a drain current of 100 mA/mm [3]. The load pull simulations for the conventional architecture at V_{DS} of 28 V reveals a saturated output power density (P_{SAT}) of 2.59 W/mm and Gain of 23 dB @ 3 GHz, as shown in Fig. 1(c). Recessing the gate architecture by 5 nm reduces the P_{SAT} to 2.53 W/mm accounting for an overall decrease in P_{SAT} by 2.3 % as a result of channel depletion. A better electrostatic control in recessed architecture is evident from the load pull simulations shown in Fig. 1(c) revealing a Gain of 25 dB (8 % increment) at 5 nm due to a reduction in the distance between the Gate and the 2DEG channel. To investigate the reliability of recessed gate architectures, load pull simulations were performed at 100 °C for 3 different recess depth as compiled in Table 1. It is observed that the deterioration in P_{OUT} is significant as far as the conventional architectures are present, while the recessed architectures maintain their comparatively larger gain even at higher temperatures.

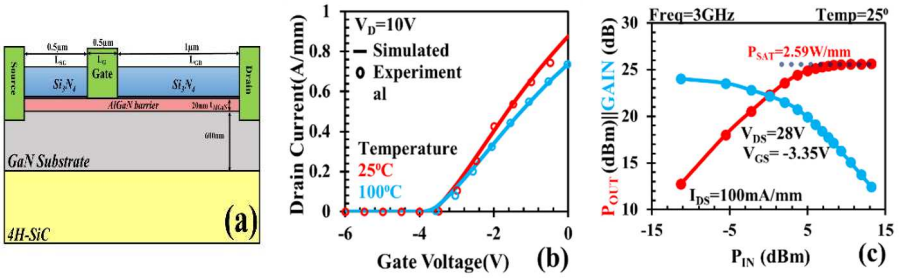

Figure 1. (a) Schematic view of the GaN HEMT device along with its (b) transfer characteristics at 25°C and 100°C (experimental data: [2]), and (c) load pull simulations @ 3 GHz depicting saturated output power density of 2.59 W/mm.

Table 1. Comparison of RF performance of Conventional and Recessed Gate architecture at 25°C and 100°C.

Device Architectures		Δ (25°-100°) Pout (W/mm)	Δ (25°-100°) Gain (dB)
Conventional		0.43	0.6
Recess	2nm	0.39	1.4
	3nm	0.23	1.5
	5nm	0.22	2.2

References:
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