MONDAY 15TH JUNE, 2009

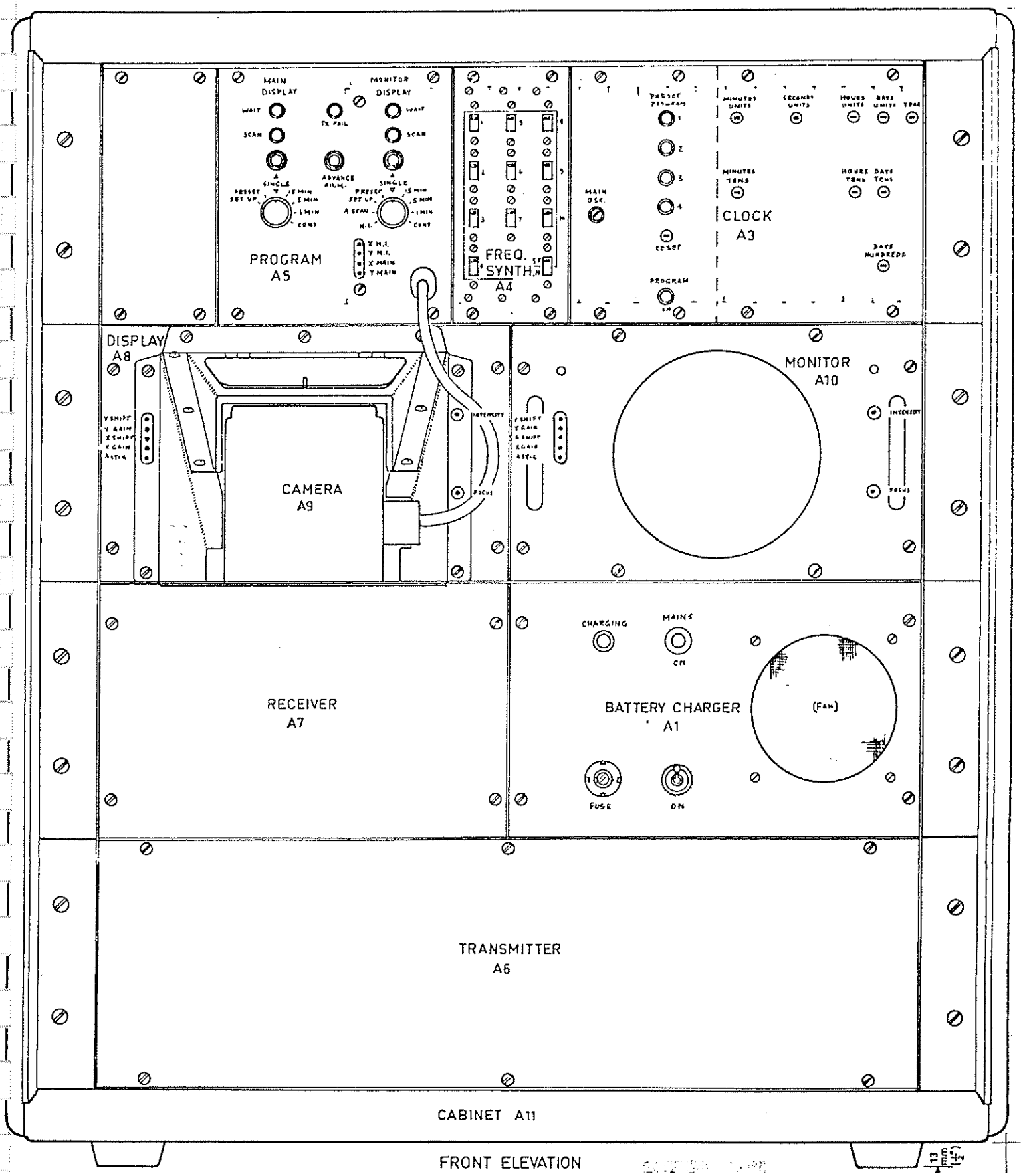
THIS IS A COMPLETE AND UNMARKED TYPE 4B, HANDBOOK, THAT IS REQUIRED FOR THE DIGION SERVICE.

INDEX BY SECTIONS.

INDEX BY ASSEMBLIES

UNIT	ASSEMBLY	RELEVANT SECTION PARAGRAPHS
A1 MAIN POWER SUPPLY	A1A1/A1A2	3.10.1. to 3.10.4
A2 BATTERY		
A3 CLOCK	A3A1 YEARS	3.1.1, 3.1.22, 3.1.16, 3.1.18.
	A3A2 DAYS	" , 3.1.21, " , " .
	A3A3 HOURS	" , 3.1.20, " , " .
	A3A4 NUMERAL GENERATOR	3.6.1 to 3.6.4
	A3A5 SECONDS	3.1.1, 3.1.14, 3.1.15, 3.1.16, 3.6.5, 3.6.6, 3.7.20.
	A3A6 STN No./MASTER COMM.	3.6.1, 3.6.5, 3.6.7.
	A3A7 MINUTES	3.1.1, 3.1.17, 3.1.18, 3.1.19, 3.6.5.
	A3A8 CONTROL LOGIC	3.7.1, 3.7.8 to 3.7.16.
	A3A9 PRESET PROGRAM	
	A3A10 COMM. GENERATOR	3.6.1, 3.6.5, 3.6.6, 3.7.18.
	A3A11 OP'N'L DIVS, GRATICULE GEN.	3.1.1, 3.1.5, 3.1.7 to 3.1.12.
	A3A12 CLOCK OSCILLATOR	3.1.1, 3.1.3, 3.1.4, 3.5.1, 3.5.2, 3.5.3, 3.7.20, 3.8.16, 3.8.17.
A4 SYNTHESIZER	A4A1 DIGITAL SECTION	
	A4A2 RF SECTION	
A5 PROGRAM	A5A1 TIMEBASES/FUNCTION CONTROLS	3.7.1, 3.7.2 to 3.7.7, 3.8.8 to 3.8.15.
A6 TRANSMITTER	A6A1 POWER SUPPLY/PULSER	3.3.1, 3.3.2, 3.3.3.
	A6A2 DRIVER	3.3.1, 3.3.4.
	A6A3 POWER AMPLIFIER	3.3.1, 3.3.5.
	A6A4 Tx TAIL DETECTOR	3.3.1, 3.3.6.
A7 RECEIVER	A7A1 BANDPASS FILTER	3.4.1, 3.4.2.
	A7A2 VFO AMP./1st MIXER	3.4.1, 3.4.2.
	A7A3 70MHz FILTER	3.4.1, 3.4.3.
	A7A5 1st IF/2nd MIXER & OSC.	3.4.1, 3.4.3.
	A7A6 2nd IF/3rd MIXER & OSC.	3.4.1, 3.4.4.

	A7A7 3rd IF/DETECTOR	3.4.1, 3.4.5.
	A7A8 AGC & PULSE SHAPING	3.4.1, 3.4.6.
A8 MAIN DIAPLAY	A8A1 18V REGULATOR	3.8.1, 3.8.2, 3.8.3.
	A8A2 POWER SUPPLY	3.8.1, 3.8.2, 3.8.4.
	A8A3 EHT DIVIDER	3.8.1, 3.8.2, 3.8.5.
	A8A4 DEFLECTION CIRCUIT	3.8.1, 3.8.2, 3.8.6.
	A8A5 Z MODULATION CCT.	3.8.1, 3.8.2, 3.8.7.
A9 CAMERA	A9A1 MOTOR DRIVE CCT.	3.9.1, 3.9.2.
A10 MONITOR DISPLAY	AS FOR A8	
A11 CABINET		
A12 IC POWER SUPPLY	A12A1 IC POWER SUPPLY	3.10.1, 3.10.5.
	A12A2 REFULATORS	3.10.1, 3.10.6.
A13 HARNESS		



FRONT ELEVATION

SECTION 1

INTRODUCTION

1.1 PURPOSE OF THE EQUIPMENT

The general purpose of this equipment is to sound the ionosphere at regular intervals by the pulse-echo technique at vertical incidence, and to plot the relationship of the virtual height of reflection of the pulse echoes against the transmitted frequency.

The operating frequency of a pulsed transmitter is varied over the range 1 MHz to 22.6 MHz. The resulting echoes from the ionosphere are then detected by a receiver tuned, automatically, to the same frequency as the transmitter. The echoes received are processed to remove noise and interference and are displayed on a cathode ray tube along with a graticule indicating virtual height along one axis and frequency along the other. The trace is then photographed by an automatically operated camera, and the records produced are called ionograms. From these records the necessary ionospheric data are obtained and used for prediction and research purposes.

The style of ionogram produced by the 4A ionosonde is illustrated in figure 1.1.1. A simplified block diagram is given in figure 1.1.2.

1.2 GENERAL DESCRIPTION

This instrument is a largely solid state, swept-frequency, pulse ionosonde designed for routine vertical-incidence sounding of the ionosphere. It employs a digital frequency synthesizer and digital programming, control, signal processing and display techniques with an absolute minimum of electromechanical components to ensure high reliability and provide the possibility of remote, unattended operation.

Only six vacuum tube devices are used in the instrument. Four valves are employed in the transmitter final power amplifier, producing 5 kW peak pulse-power output. Two conventional CRT's are employed in the recording and monitor displays.

The digital frequency synthesizer provides coverage from 1 MHz to 22.6 MHz in 576 logarithmic steps. A complete frequency sweep to produce an ionogram takes 12 seconds of a 20 second program cycle. A group of front panel switches allows the operator to manually select any of the synthesizer's 576 channels so that single frequency soundings can be made in conjunction with the A-scan display facility. It is an entirely electronic frequency control system.

The instrument features selectable programming, there being four basic programs. These range from one sounding every 15 minutes ('normal' programming) to three per minute ('continuous'). An optional 'preset programmer' can be set to vary the selected program for chosen periods in twenty four hours. The programming and control is derived from a crystal-controlled chronometer, which also provides a digital date/time output for recording on the ionogram and which may be displayed on the monitor CRT for the operator's convenience. The numerals are 8-segment, rather than 7-segment, characters to improve clarity.

Signal processing of the received echoes is employed to remove noise and interference from the ionogram. The ionogram is uncluttered by bands of noise or interference from HF transmissions, reducing uncertainties and ambiguities in interpretation and scaling.

The ionogram is recorded on 16 mm film. Consumption is 750 mm per day when normally programmed at four soundings per hour. The recorded ionogram is orietated such that the film can be projected by a standard 16 mm movie projector providing a speeded-up, time-lapse view of the ionosphere. The use of a CRT having a small spot size and a low distortion optical system provides more than adequate scaling accuracy.

Power consumption is about 100 watts, derived from a mains-operated power supply. In the event of mains failure two 40 amp-hour lead-acid batteries may provide power for periods up to 10 hours. The batteries are charge-maintained from the mains power supply.

Standard ISEP rack and cabinet mechanical components are widely used throughout the ionosonde assembly, standardising mechanical components and simplifying construction. The overall size, together with a weight less than 60 kg, allows bench mounting.

Digital circuitry throughout the instrument is all commonly available TTL logic.

Two prime design objectives of this instrument were simplified, reliable routine operation and improved date retreival. To this end, the electronics have been designed to provide easy setting-up and simple, but flexible program selection and operation with a range of useful alternatives. Also, the ionogram format and recording have been designed to reduce film usage and processing and greatly improve the speed and ease of extracting data.

1.2.1 Ionogram Presentation

The method of producing the ionogram, and its format, differ from previous practice and techniques.

Traditionally, an ionogram was produced by drawing film past an intensity-modulated CRT display having range (i.e. virtual height) along the timebase and the return echo pulses blanking the trace at the suitable intervals. Frequency marks were obtained by momentarily blanking the whole trace as the VFO passed frequency markers, usually at 1 MHz intervals, derived from a crystal oscillator and harmonic generator. Date, time and station identification were recorded on the film by momentarily flashing lamps to illuminate the date/time wheels of an electromechanical clock device.

In the 4A ionosonde, the ionogram is slowly 'written' on the face of the CRT by a scanning process, in a similar manner to the way a TV picture is scanned across a picture tube. The line scan goes from 0 to 800 km and moves along the frame, from left to right, with increasing frequency. The complete ionogram, including the graticule and numerals, is written on the CRT while the camera shutter remains open and the film stationary. The film is advanced after the shutter has closed. The received echoes are prevented from being superimposed on the graticule or numerals to avoid ambiguity or confusion.

1.2.2 Removing Interfering Signals

Interference from HF transmissions is prevented from being displayed in the following way. The receiver AGC circuit samples the level of signals received, in the particular frequency channel, following each transmit pulse and adjusts the receiver gain accordingly. If the echo pulses, or any other pulse-type interference, exceeds this level by a small threshold they are detected and converted to a digital-level pulse for processing by the signal processor. If the echoes do not exceed the level of received signals then nothing will be displayed on the CRT, leaving a small hole in the ionogram. Very little information is lost as interference has to spread over a wide frequency band before large holes become apparent in the recorded trace.

The signal processor first blanks all signals in the first 50 km of the ionogram, removing the ground pulse. As the graticule and the transmit pulse are derived from the same circuitry in the ionosonde, displaying the ground pulse is unnecessary.

1.2.3 Noise Interference Suppression

Atmospheric static is essentially random in nature and ignition noise, while repetitive, does not exhibit a stable interval between pulses. The repetitive characteristics of the received pulses are used to exclude noise and pulse-type interference from the ionogram.

Three RF pulses are transmitted on each frequency channel. The detected first echoes and noise are stored in a shift register and then compared with echoes from the second transmitted pulse along with noise and any spurious pulses. Any coincident pulses, predominantly echoes, are recirculated into the shift register and the comparison repeated following the third transmitted pulse. At the end of this cycle, echoes, most likely being the only coincident events, are virtually the only surviving signals and are subsequently displayed on the CRT.

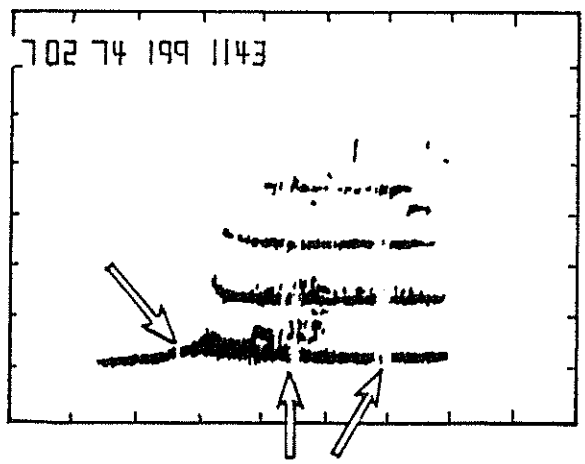


FIG. 1. 2.1. Ionogram, showing holes produced by AGC operation under conditions of severe interference.

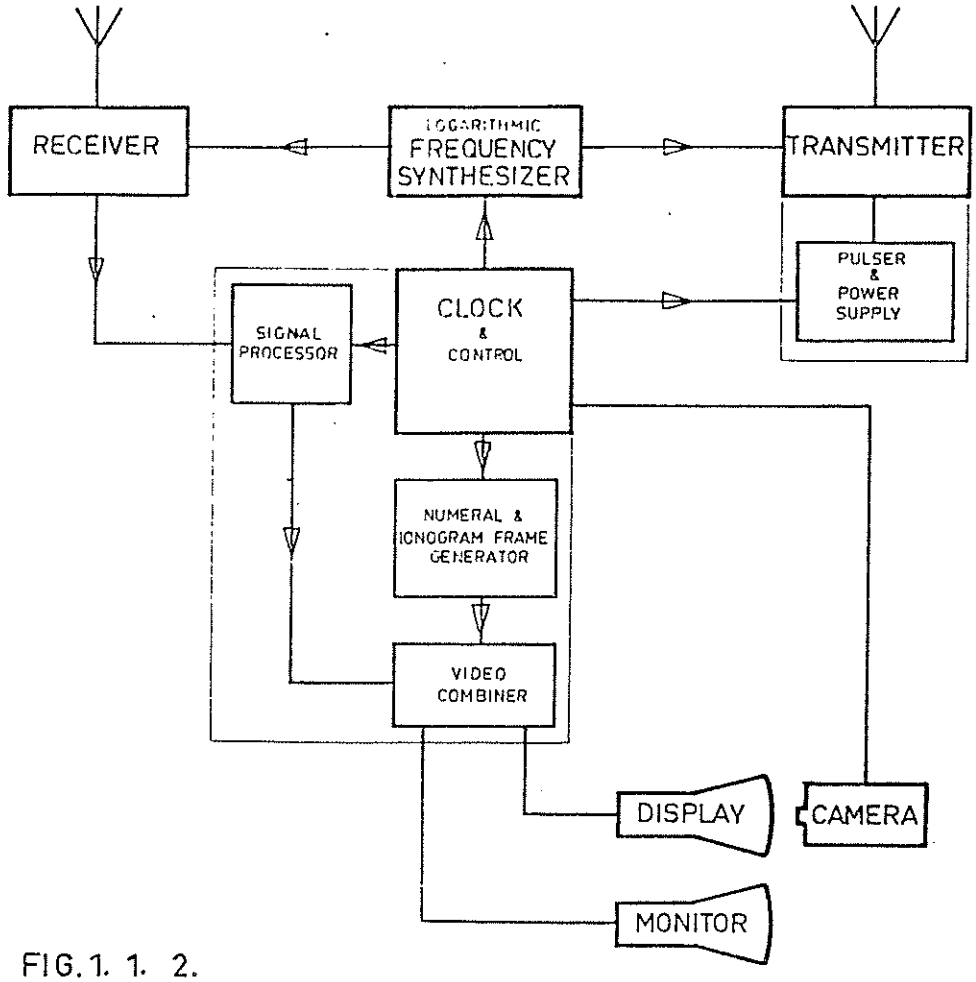


FIG. 1. 1. 2.

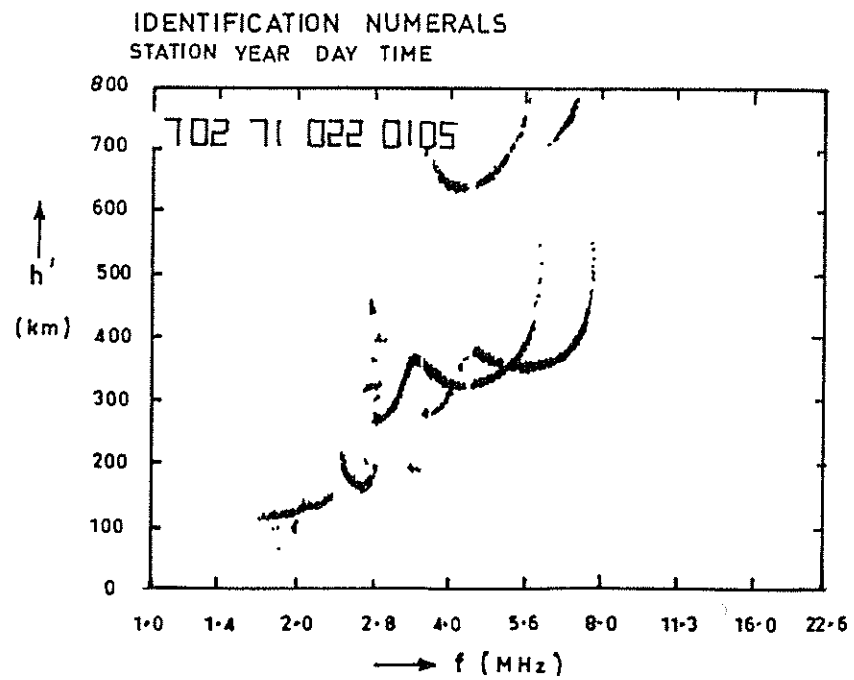


FIG. 1. 1. 1. Style of Ionogram produced by 4A 'Sonde.

1.2.4 Date/Time/Ident. Numerals and Graticule

The numerals are produced by digital techniques, eight-segment characters being used. Improved clarity over seven-segment characters is obtained. The appearance of the numerals is illustrated in fig. 1.2.2.

Three identification numerals are provided. The last two digits of the year, a three digit day number, and four digit hours/minutes numbers are displayed on the ionogram.

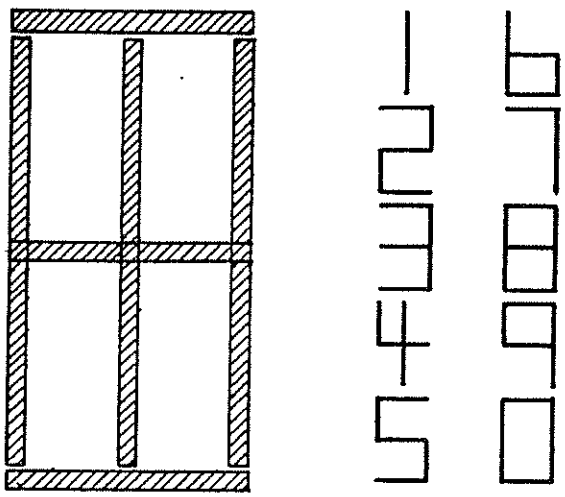


FIG. 1.2.2. Arrangement of 8-Segment Numerals

The graticule is also digitally produced. The range and frequency timebases are synchronised from the same source that produces the graticule brightening pulses, and the transmit pulses.

Height markers are at 100 km intervals to 800 km, the maximum range of the instrument. Frequency markers are derived from the chronometer dividers and not by comparing a wideband frequency comb with the transmit frequency. Frequency markers are at even intervals along the frequency axis, there being ten all told, at 1.0, 1.4, 2.0, 2.8, 4.0, 5.6, 8.0, 11.3, 16.0 and 22.6 MHz. The edges of the graticule indicate the 1.0 MHz and 22.6 MHz markers.

1.2.5 Frequency Generation

The frequency synthesizer is controlled by a 10-bit binary number which steps the output through 576 channels increasing logarithmically in frequency with each step. The synthesizer may be manually set to any of the 576 channels by a group of ten front panel switches for single-frequency soundings.

The synthesizer provides two outputs, one to drive the transmitter and one as the first conversion signal for the receiver.

1.2.6 The Receiver

The receiver is a triple-conversion design employing IF's of 70 MHz, 10.7 MHz and 1.6 MHz. The receiver bandwidth of 40 kHz is obtained in the 1.6 MHz IF stage which employs L-C circuits to achieve the narrow bandwidth with steep skirt selectivity. Overall gain is about 90 dB. Double-balanced ring-diode mixers are employed for their large signal-handling characteristics and to reduce spurious responses. No RF amplification is employed, the antenna signals are fed to the first mixer via a bandpass filter consisting of a low-pass filter with a cutoff of 1.6 MHz and a high-pass filter with a cutoff of 23 MHz. Both cutoff frequencies can be varied. The low-pass filter attenuates possible strong local AM broadcast band transmitters which may cause receiver overload and cross-modulation of signals above the cutoff frequency. The high-pass filter attenuates upper-HF and VHF transmissions that may also cause cross modulation or breakthrough into the first IF.

1.2.7 The Transmitter

The transmitter employs a solid-state, pulsed, wideband amplifier to drive the power amplifier. The PA employs four tubes which were designed for TV vertical output stages. This allows a low EHT to be used and 1.5 kV is supplied to the anodes, the screens being pulsed with a 500 V, 40 μs pulse in synchronism with the driver.

The peak pulse-power output is 5 kW which falls to about 1 kW near 12MHz and about 500 W above 20 MHz.

1.2.8 Monitor and Recording CRT's

The monitor and recording CRT's are electrically identical, and mechanically interchangeable. The recording CRT however, is rotated 90° to the monitor so that the ionogram is correctly orientated on the film. Operationally the two units are independent. They can be individually programmed to perform separate individual functions.

The programming functions are selected by front panel switches. The recording CRT has seven programmable functions and the monitor, nine. The seven functions for the recording CRT are also common to the monitor.

The seven common functions are as follows:

SET UP: A 5 x 7 dot matrix is displayed on the CRT to facilitate the adjustment of CRT brightness, focus and geometry as well as camera focussing.

PRESET: This initiates the Preset Programmer.

SINGLE: A single ionogram can be produced by pressing a push button on the front panel.

15 MIN: 'Normal' programming. The ionosonde will automatically make a sounding every 15 minutes.

5 MIN: The ionosonde will automatically make a sounding every five minutes.

1 MIN: The ionosonde will automatically make a sounding every minute.

CONT.: 'Continuous' sounding. As the complete sounding cycle lasts 20 seconds, the ionosonde will record three ionograms per minute.

The two functions unique to the monitor are:

N.I.: 'Numeral Indication'. The date and time are displayed, in large format digital numerals, on the monitor CRT. The seconds are also included in this display. This facility enables operator to 'set' the clock.

A-SCAN: A standard A-scan is displayed each programmed sounding.

It is possible for a second camera to be mounted on the monitor unit and two separate, independently programmed recordings to be made simultaneously.

1.3 GENERAL SPECIFICATIONS

Frequency Range	1 to 22.6 MHz
Frequency Generation	Digital Synthesizer
Number of Channels	576
Frequency Sweep Configuration	Logarithmic
Frequency Sweep Time	12 seconds
Transmitter Pulse Power Output	5 kW
Transmitter Pulse Width	41.67 μs
Pulse Interval	5.33 ms, three on each frequency channel
Maximum Virtual Height Range	800 km
Height Marker Interval	100 km
Frequency Markers	Ten equally spaced markers at 1.0, 1.4, 2.0, 2.8, 4.0, 5.6, 8.0, 11.3, 16.0, 22.6 MHz
Date/Time/Ident	8-segment digital numerals 'written' on ionogram.
Programming	Four manually selected automatic programs: 1 each 15 min. 1 each 5 min. 1 each 1 min. and 3 per min. Optional 'preset programmer' can provide selectable variation of normal program.
Film	16 mm
Film consumption	750 mm per day at four soundings per hour
Power Supply	Mains operated, or 22 to 28V @ 4A max. from two lead-acid batteries
Size	H = 609 mm, W = 520 mm, D = 457 mm
Weight	52 kg

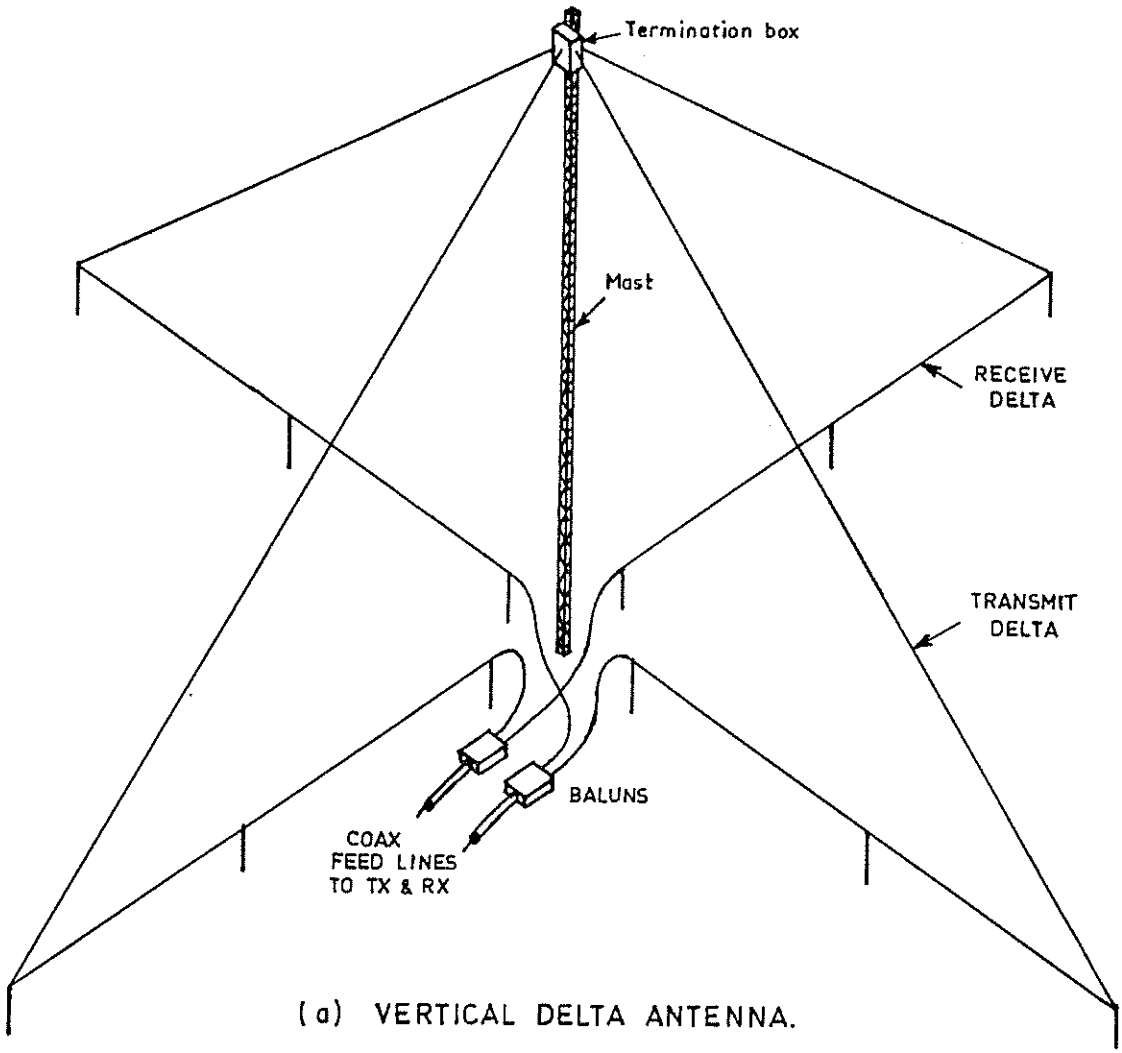
1.4 The Antenna System

Two Vertical Delta antennas are usually employed, one for the transmitter and one for the receiver. The configuration is shown in figure 1.4.1. Each antenna consists of a large, triangular loop of wire, supported at the apex. The two antennas are mounted orthogonally to reduce coupling between them. The feedpoint is at the centre of the base of the loop. A 600 ohm terminating resistor is inserted in series with the loop at the apex so that the antenna provides essentially unidirectional radiation in the vertical direction. A high power terminating resistor is necessary for the transmitting antenna.

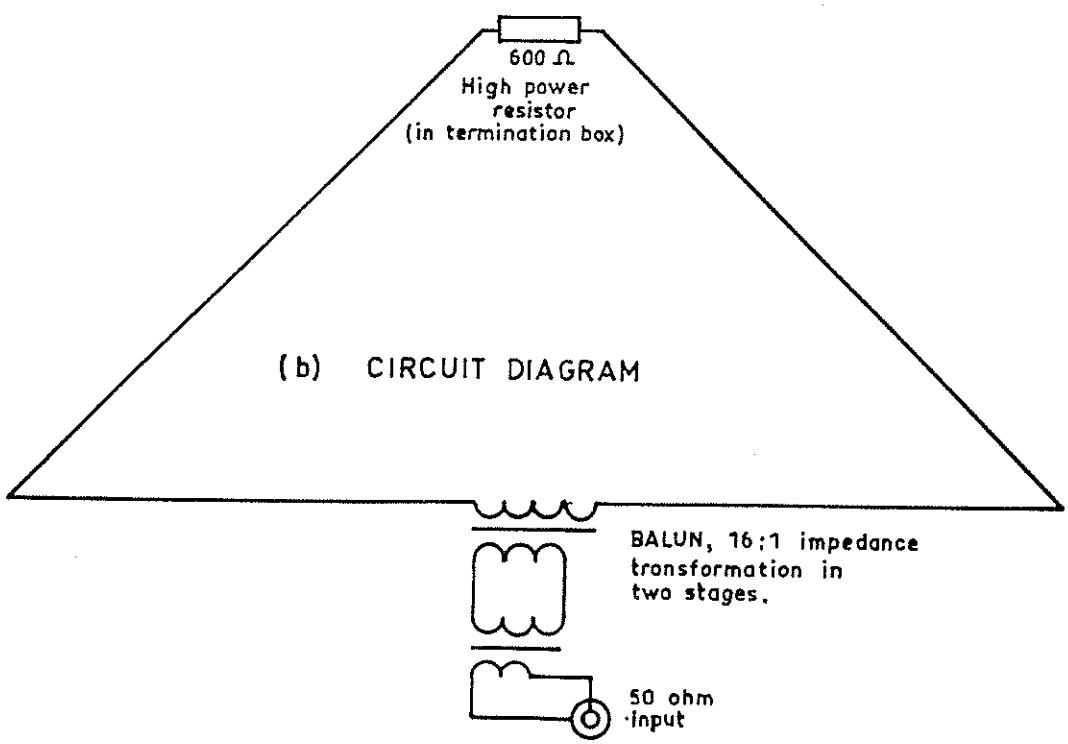
These antennas are used because they may be erected from a single tower, are low in cost, provide an essentially vertical radiation pattern and have reasonable radiation efficiency over the frequency range.

The 4A Ionosonde is designed for low impedance, unbalanced receiver input and transmitter output and employs coaxial cable feedlines to each antenna. This is to avoid problems with transmitter feedline radiation being coupled back into the receiver and digital circuitry in the instrument, which is susceptible to RF interference. It also reduces interaction between the two feedlines, particularly on long runs. Coaxial cable feedlines may be conveniently buried.

The Vertical Delta antenna has an average feedpoint impedance of about 800 ohms and requires a balanced feedline. A balun transformer is used to transform the antenna feedpoint impedance to 50 ohms for the coaxial cable feedline, and converts the unbalanced cable to a balanced configuration to suit the antenna feedpoint characteristics. The balun is located at the antenna and has a turns ratio of 4:1 providing an impedance ratio of 16:1. Essentially, it consists of two transmission line transformers, each wound on several large toroidal ferrite cores, to obtain wide bandwidth, the impedance transformation being obtained in two steps.



(a) VERTICAL DELTA ANTENNA.



(b) CIRCUIT DIAGRAM

FIG. 1. 4. 1.

SECTION 2

SET-UP PROCEDURE

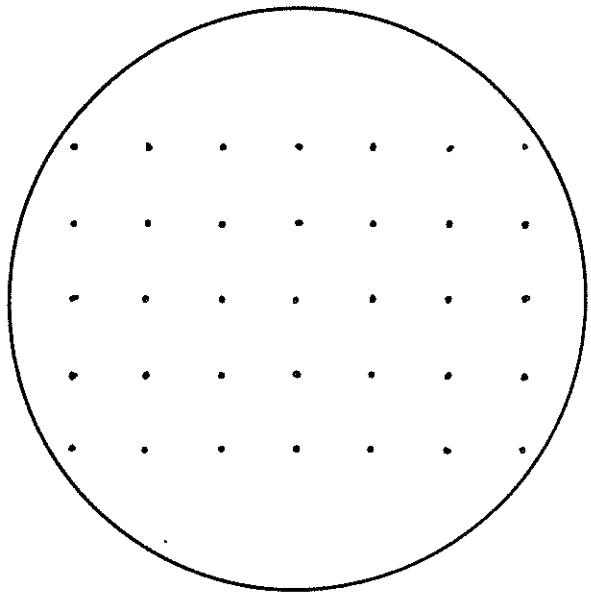


FIG. 2.1.1. The SET-UP graticule adjusted for the best size.

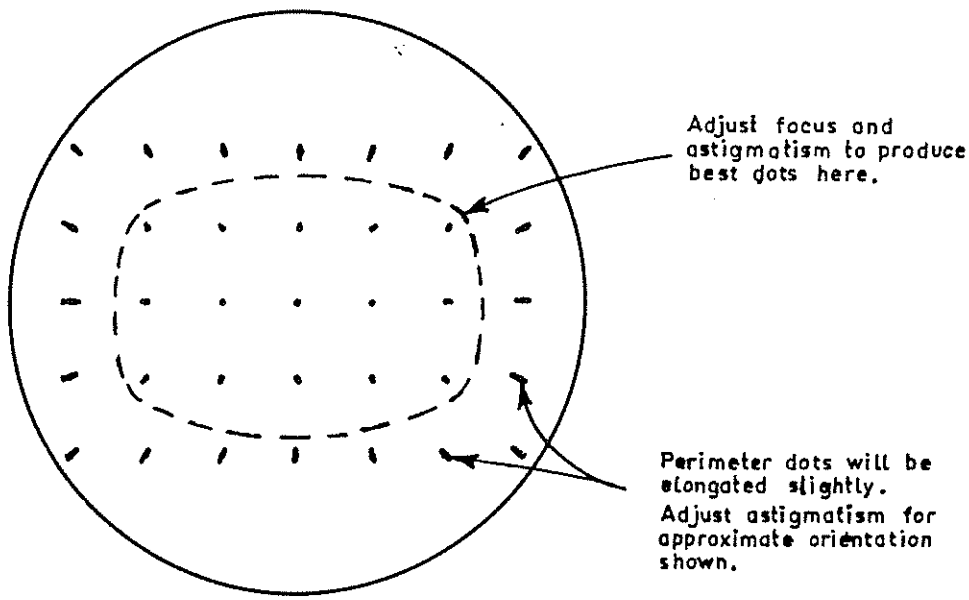


FIG. 2.1.2. The SET-UP graticule adjusted for the optimum focus and astigmatism. Intensity should be kept low. (Elongation of dots exaggerated.)

2.1 SET-UP PROCEDURES

2.1.1 Introduction

Each ionosonde is completely aligned and set-up ready for operation prior to commissioning. Initially however, the date and time will need to be set and some of the preset controls may be adjusted to suit the individual preferences of the operator. In addition, the preset controls may need to be adjusted after an initial "settling" period, following servicing, or when putting a sonde back into regular operation following a period of disuse.

This section only includes the setting of these preset controls accessible from the front panels of the various units.

2.1.2 Setting up the CRT Displays

(1) Turn on the Main Power Supply (A1) and allow 10-15 minutes for the instrument to warm up.

(2) Remove the film magazine from the camera.

(3) Set both display function switches (on the front panel of the PROGRAM unit) to SET-UP.

(4) Adjust intensity and focus on each CRT to obtain a reasonably clear pattern. This is only a rough, initial adjustment.

(5) Adjust the Y-shift and gain, and the X-shift and gain controls on each Display unit in turn so that the whole dot matrix is squarely positioned and not overscanned. See figure 2.1.1. Note that the Main Display CRT is rotated 90° with respect to the MONITOR CRT.

(6) Adjust the intensity, focus and astigmatism controls to obtain small, well-focussed inner dots. The size of the dots is determined by the brightness. The finest dots are obtained at a low intensity. The dots around the perimeter may be slightly elliptical, especially the four corner dots. Adjustment of the astigmatism control will rotate the elongated dots. Set this control so that the dots appear similar to the exaggerated display illustrated in figure 2.1.2.

(7) Set the MONITOR function switch to N.I. Adjust the X-N1 and Y-N1 trimpots for the desired display size. These controls are accessible from the PROGRAM unit front panels.

(8) Set both function switches to SINGLE. Set the TX STOP switch to the UP position (off). This is a slide switch (A13A1.S1) located on the harness channel (see dwg: MD-72Y1), at the right-hand side, opposite the battery input connector. This prevents the Transmitter being pulsed during testing.

(9) Press the SINGLE pushbutton for the MONITOR to initiate a single ionogram. The following sequence of events should occur:-

a) The Monitor WAIT light comes on.

b) A short time later the Monitor SCAN light comes on and a sounding commences.

c) About two seconds later the ionogram will commence at the left hand side of the Monitor CRT screen.

d) At the end of the sounding cycle the SCAN light extinguishes.

(10) Check that the ionogram size is adequate, not overscanned, and that it does not commence or finish partially off-screen. If the ionogram is the incorrect size, adjust the X-MAIN and Y-MAIN timebase controls on the Program unit front panel.

(11) Repeat (9) and (10) for the MAIN display. The ionogram size should be sufficient to fill the film frame. Adjust the shift and gain controls if necessary to adjust the ionogram size and position. The best definition for film recording is obtained with minimal brightness and a wide lens aperture.

(12) Check that all programmed soundings operate for both the MAIN and MONITOR displays.

(13) Connect the antennas and set the TX STOP switch to the DOWN position to allow the transmitter to be pulsed during a sounding.

(14) Set the function switches to SINGLE and initiate a sounding. Alternatively, set the switches to CONTINUOUS.

(15) Observe the ionogram and see that the date/time/ident numerals are being displayed and that reflections are obtained. See that the graticule is not affected by RF interference. If so, check all the earth bonding to the harness channel, particularly to the Receiver and Transmitter chassis and the Synthesizer cables.

(16) Set the Monitor function switch to A-Scan. Initiate a sounding from the Main function switch and observe the A-Scan. Echoes should be readily visible. The A-Scan sweep width can be adjusted if necessary. See section 3.8.11.

(17) Set Main function switch to desired program and return Monitor function switch to SINGLE.

2.1.3 Setting the Clock

The timing of all the ionosonde functions is derived from a crystal-controlled master oscillator. This is adjusted by a trimmer which is accessible through the front panel. It is designated MAIN OSC. and is mounted on board A3A12, located immediately to the right of the Frequency Synthesizer.

The frequency of the master oscillator should be checked using a digital frequency meter (d.f.m.). Measure the frequency at pin 14 of IC2 on board A3A12 (dwg: CD-229Y1). It should be set to within 100 Hz of 6144 kHz. The d.f.m. should be warmed-up for at least one hour beforehand. Note which direction the trimmer is turned to increase or decrease the frequency.

Having set the master oscillator, the chronometer section of the ionosonde clock needs to be set to the station time, together with the day number and year, and the clock synchronised to UT.

Set the MONITOR function switch to N.I. Each of the displayed chronometer numbers can be set by operating the microswitches accessible through the front panel of the clock section of the top rack assembly. Set the numerals in the following order:-

MINUTES UNITS)
)
MINUTES TENS)

Set about 3 mins. ahead of required time

HOURS UNITS

HOURS TENS

DAYS UNITS

DAYS TENS

DAYS HUNDREDS

YEAR UNITS

When this is completed, watch the seconds numerals on the N.I. display and depress the SECONDS microswitch, holding it operated, immediately a "00" is displayed. This stops the clock at the beginning of the minute displayed at that time. It should be by now a minute or so ahead of the correct station time. To synchronise the clock, monitor a standard time signal transmission. When the displayed minute is reached, as indicated by the time signal transmission, release the SECONDS microswitch at the 00 second indicated by the time transmission identification. The ionosonde clock is then synchronised to UT.

If the master oscillator is not within a very close tolerance of the frequency, then a cumulative time error will become apparent. Check the ionosonde time against the time signal transmission each day for a number of days following setting of the clock. If the master oscillator is a little high in frequency the clock will be slightly fast. If it is low, the clock will be slow. Reset the clock, then adjust the MAIN OSC. trimmer slightly to compensate. Monitor the clock time over the next week to determine the effect. Make further adjustments as necessary.

SECTION 3

CIRCUIT DESCRIPTIONS

3.1
CLOCK

Par. No.	Title	Drawing No.
3.1.1	Overall Description	CB-34Y1
3.1.2	Circuit Descriptions	
3.1.3	The Master Oscillator-Divider	CD-229Y1 (A3A12)
3.1.4	Generating the Clock Pulses For the Signal Processor Memory	" " "
3.1.5	THE OPERATIONAL CLOCK	CB-34Y1
3.1.6	The Primary and Secondary Dividers (on A3A5)	CD-227Y1
3.1.7	The Operational Dividers	CD-225Y1 (A3A11)
3.1.8	Additional Outputs and Circuitry .	
3.1.9	The Graticule Generator	CD-225Y1 (A3A11)
3.1.10	The Transmit Pulse Generator	" " "
3.1.11	The Y-Blank Generator	" " "
3.1.12	The Camera Drive Generator	" " "
3.1.13	THE CHRONOMETER	CB-34Y1
3.1.14	The Seconds Dividers	CD-227Y1 (A3A5)
3.1.15	Seconds Dividers Auxiliary Outputs	" " "
3.1.16	Chronometer Dividers Output Multiplexing	
3.1.17	The Minutes Dividers	CD-224Y1 (A3A7)
3.1.18	The 'Advance Count' Circuit	" " "
3.1.19	Program Decoding Circuitry	" " "
3.1.20	The Hours Dividers	CD-221Y1 (A3A3)
3.1.21	The Days Dividers	CD-220Y1 (A3A2)
3.1.22	The Years Dividers	CD-218Y1 (A3A1)

3.1.1 Overall description (Dwg: CB-34Y1)

The Ionosonde Clock times all the operations of the instrument including the programming, frequency synthesizer, transmitter, signal processing, display generation and camera operation. It also provides outputs for the generation of the date/time display on the MONITOR CRT (NI display) and on the recorded ionogram.

A complete block diagram is given in drawing CB-34Y1. There are three major sections to the clock, their titles and functions being as follows:

(a) The MASTER OSCILLATOR/DIVIDER. This provides 96KHz (the PRIMARY FREQUENCY) to the PRIMARY DIVIDER and narrow, two-phase high frequency clock pulses for the operation of the SIGNAL PROCESSOR.

(b) The OPERATIONAL CLOCK. This times all the operations of the ionosonde during a sounding as well as continuous functions such as the numeral generation and date/time display. It provides 1pps to drive the CHRONOMETER and a number of binary coded outputs for the operation of the CONTROL SYSTEM, the FREQUENCY SYNTHESIZER during a frequency scan and the COMMUTATION GENERATOR for the generation of the date/time numeral display. In addition, this section of the clock generates:

* The transmit pulses
* A control pulse for the SIGNAL PROCESSOR shift register
* Camera motor drive pulses which also serve as the Y MAIN and X A-SCAN timebase reset waveform.
* Y-blanking pulses for the ionogram display
* The Graticule for the ionogram display
* Pulses for the generation of the X-Blank control and display pulse.

(c) The CHRONOMETER. This derives five binary-coded outputs for the date/time display, provides outputs for the programming circuitry in the CONTROL SYSTEM and resets the OPERATIONAL CLOCK dividers every 20 seconds. In addition, it generates a pulse to close the camera shutter at the end of a sounding and pulses for the 'Tx-Fail' warning light.

3.1.2 Circuit descriptions

With the exception of the Master Oscillator, the Clock uses digital TTL integrated circuits throughout. Seven plug-in printed circuit boards contain the complete Clock circuitary, these being sub-assemblies:

A3A1
A3A2
A3A3
A3A5
A3A7
A3A11
A3A12

The block diagram in drawing CB-34Y1 indicates which sections of the Clock circuitry are located on each sub-assembly.

3.1.3 The Master Oscillator-Divider (on A3A12)
(Dwg: CD-229Y1)

The Master Oscillator operates at 6144kHz and is divided by 64 to produce the 'Primary Frequency' of 96kHz.

Transistor TR1 is a crystal-controlled Colpitts oscillator. The 6144kHz crystal is adjusted precisely to frequency by a series trimmer capacitor, C2, which is accessible through the front panel. Transistor TR2 interfaces the oscillator output to TTL logic levels, also acting as a buffer. A crystal in the 6MHz frequency range is used owing to its superior temperature stability characteristics compared to lower frequency units.

The Master Osicllator output is first divided by 16 with IC2, a type 7493 binary divider, producing pulses 1.3 us wide which are subsequently used as clock pulses for the Signal Processor shift register or memory.

The output of IC2 is then divided by four in IC1, a 7493, using only two out of its four binary dividers. The output, 96kHz, goes to pin 27 of AeA12/PL1. This signal also clocks the shift register.

The Signal Processor Memory is a dynamic shift register, the operation of which requires clock pulses at a repetition rate of 96kHz to accommodate 512 bits of data in a 5.33mS period. Each data bit occupies 10.4 uS.

3.1.4 Deleted.

3.1.5 THE OPERATIONAL CLOCK (on A3A5 and A3A11)

3.1.6 The Primary and Secondary Dividers (on A3A5)

The Primary Frequency, 96kHz, is divided by 32 to produce the Secondary Frequency, 3kHz. The Secondary Dividers then follow, dividing the 3kHz down to one pulse-per-second to drive the chronometer. The output of the Primary Dividers (3kHz) also drives the Operational Dividers located on A3A11.

The Primary Dividers consist of IC5 and portion of IC6. The first is a 7493 divide-by-16, four-bit binary counter, the output being 6kHz. IC6 is a 7492 divide-by-12 counter, the first flip-flop is the last stage of the Primary Dividers and provides a division of two, the output (pin 12) being 3kHz.

The Secondary Dividers consist of the latter portion of IC6, dividing the 3kHz by six, followed by three 7490 decade counters IC7, IC4 and IC3. The last divider, IC3, provides a division of five. The overall division ratio of the Secondary Dividers is 3000.

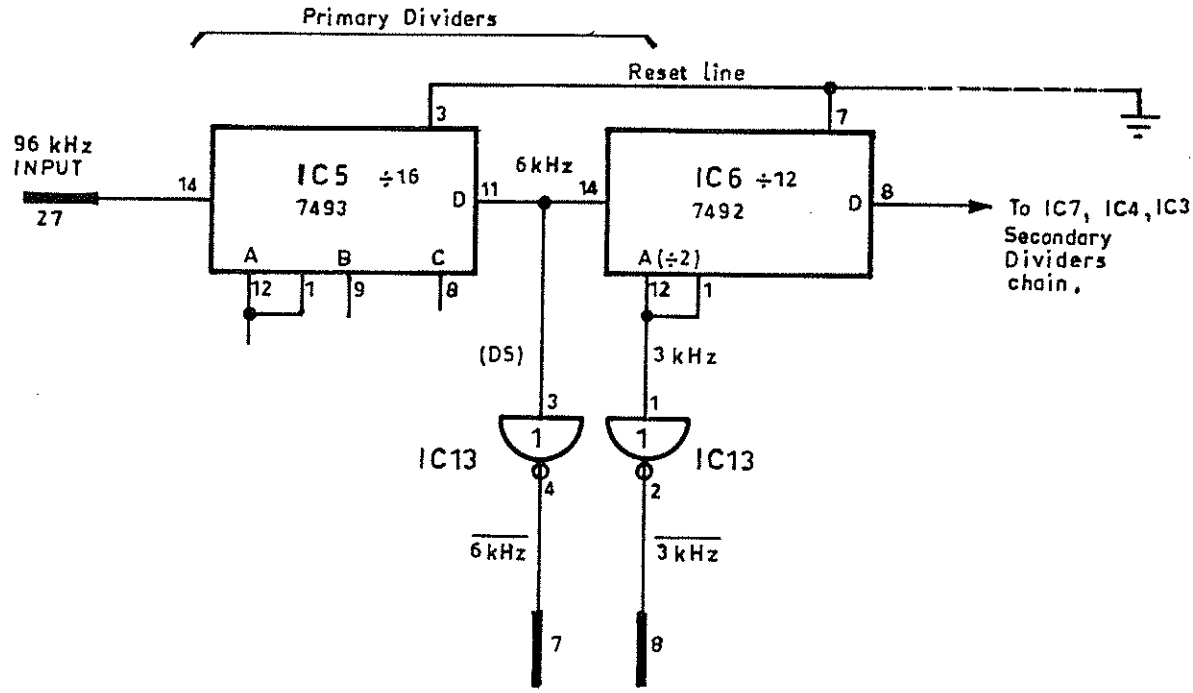


FIG. 3.1.2. Primary Dividers of the clock on A3.A5.

There are a number of outputs derived from the Primary Dividers for external circuit functions:

(a) A six-bit binary output for IC11 and IC12, on A3A5, which is part of the Numeral Generation Circuitry. These derive a four-bit BCD code used to generate the vertical segments of the numerals (see Section 3.6). This output is derived from the 96kHz input and the outputs of each divider in IC5 plus the secondary frequency, viz 96kHz
48kHz (A5)
24kHz (B5)
12kHz (C5)
6kHz (D5)
3kHz (A6)

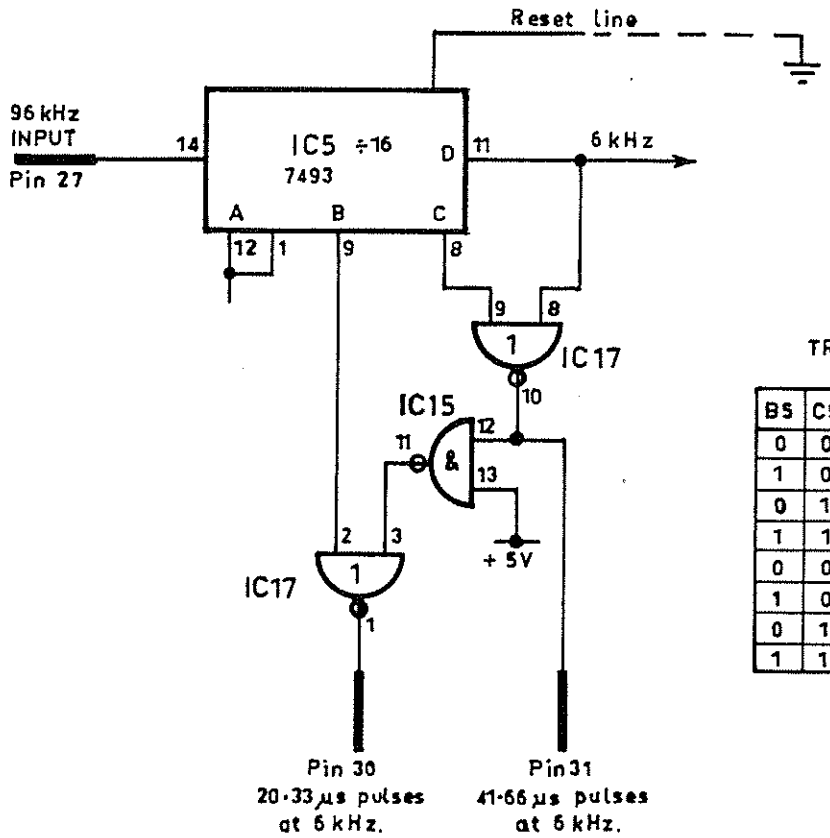
(b) A four-bit binary output for one four-input gate of IC16 which is part of the Control System and generates the Y-NI timebase reset pulse. (See Section 3.7). This output is derived from the input and the A, B and C outputs of IC5.

(c) The 6kHz output of IC5 is inverted (6kHz) and this drives the Transmitter power supply via the CONTROL LOGIC (A3A8) and also provides one input for the other four-input gate of IC16 used to generate the set-up pattern unblanking pulses. (See Section 3.7).

In addition, two other outputs are derived by ancillary circuitry:

(d) 41.66μS pulses at 6kHz for the Transmit Pulse Generator on A3A11.

(e) 20.83μS pulses at 6kHz for the Graticule Generators on A3A11.



TRUTH TABLE

BS	C5	D5	Pin31	$\overline{\text{Pin31}}$	Pin30
0	0	0	1	0	1
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	0

FIG. 3.1.3. Derivation of 41·66 μs pulses and 20·83 μs pulses from Primary Dividers.

A single two-input NOR gate (from IC17) combines the C and D outputs of IC5, as shown in figure 3.1.3, the resulting 41.66μS, 6kHz pulses appearing on pin 31 of A3A5. This output is inverted and becomes one input to another two-input NOR gate (also from IC17), the other input being the B output of IC5. This produces 20.833μS wide pulses at 6kHz, which output on pin 30 of A3A5.

The pulse diagrams for the Primary Dividers showing all the outputs are given in figure 3.1.4.

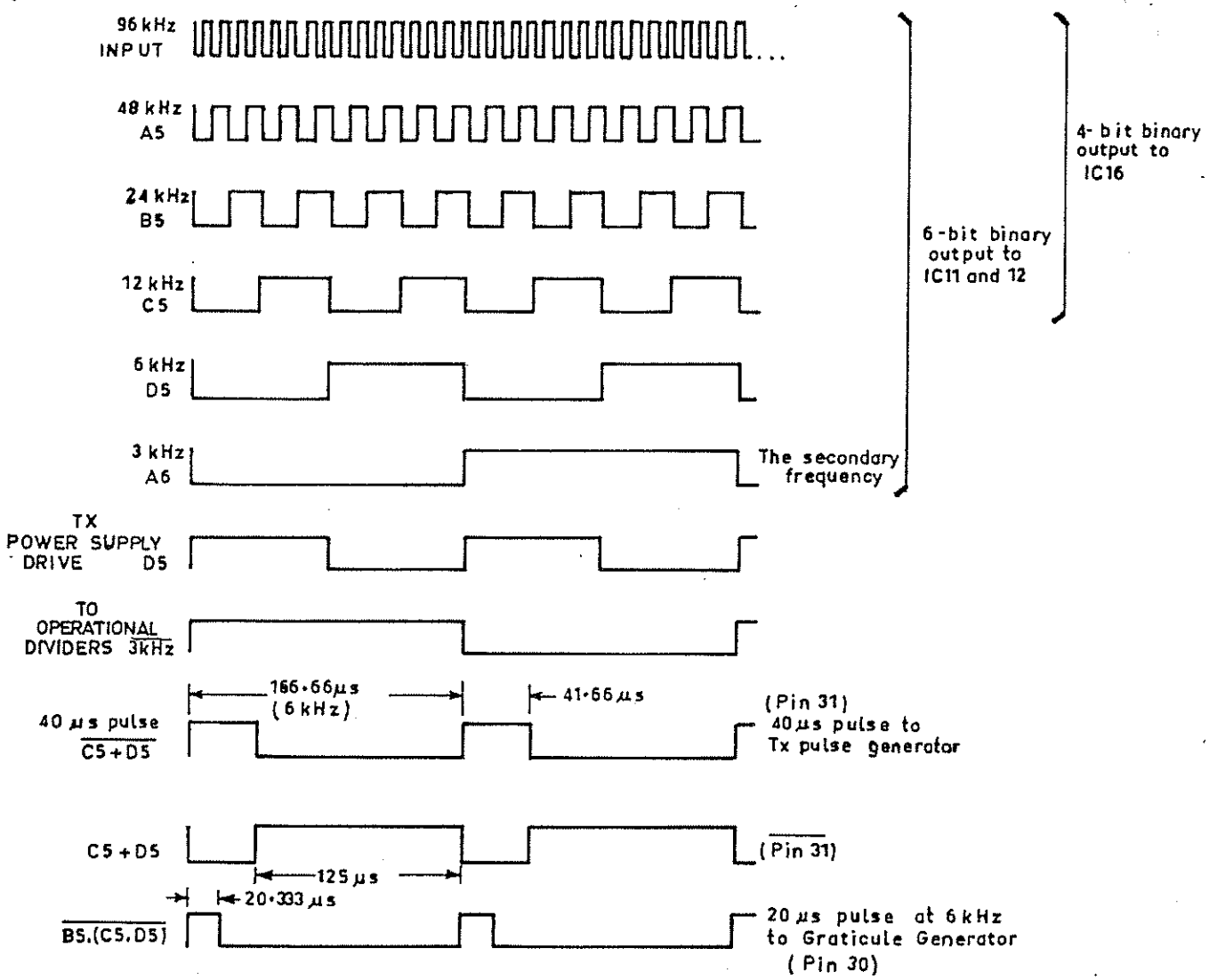


FIG. 3.1.4. Pulse Diagrams, Primary Dividers' outputs.

3.1.7 The Operational Dividers (on A3A11)
(Dwg: CD-225Y1, also refer dwg: CB-34Y1)

This provides sixteen outputs from four 7493 divide-by-16 four-bit binary counters connected in a chain. The A (÷2), B (÷4), C (÷8) and D (÷16) outputs of each IC provide outputs which are, respectively, twice the period of the previous one. The whole divider chain is reset at twenty second intervals by a pulse derived in the seconds dividers of the CHRONOMETER on A3A5.

The first divider in the chain is IC5. The input is the $\overline{3kHz}$ output from the Primary Dividers. An inverter in series with the input to IC5 inverts this again. Each counter output line has an inverter in series with it, three hex-inverters being used; IC6, IC11 and IC16. Outputs to external circuitry and the other circuitry on A3A11 are taken from both inverted and direct outputs of the counters as required.

The reset pulse from the Seconds Dividers on A3A5, via pin 26 of A3A11/PL1, is differentiated and then inverted to provide a narrow, positive-going reset pulse for the four counters, IC5, 10, 15 and 19. The last two counters in the chain (IC15 and IC19) are actually reset before completing their count. The D output period of IC19 would normally be 21.85 seconds but the reset truncates this at 20 seconds. The last pulse of the D output of IC15 is also shortened. This action is illustrated in figure 3.1.5.

The A, B, Cand D outputs of IC5 are designated A5, B5, C5 and D5, the outputs of the other three counters in the chain are also designated accordingly, i.e. A15, B15, etc. for IC15. The inverted outputs are designated $\overline{A5}$, $\overline{B5}$, etc.

The period of each output, from one negative-going edge to the next (encompassing a 0 and a 1) is listed in the following table. The width of each 0 or 1 pulse within that period is equal to half the output period.

Output	Period	Output	Period
A5	666µS	A15	170.666mS
B5	1.333mS	B15	341.333mS
C5	2.666mS	C15	682.666mS
D5	5.333mS	D15	1.3653S
A10	10.666mS	A19	2.7306S
B10	21.333mS	B19	5.4613S
C10	42.666mS	C19	10.9226S
D10	85.333mS	D19	21.8453S

The input period is 333µS (3kHz)

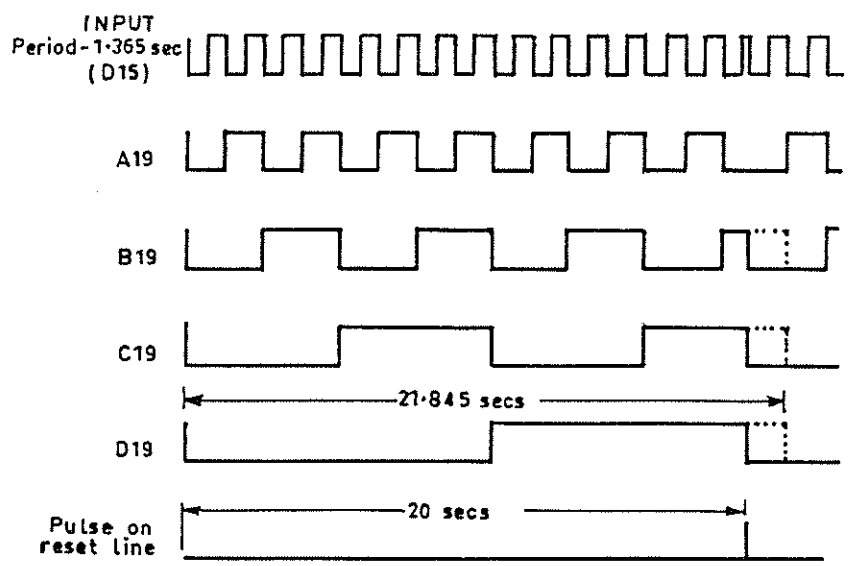


FIG. 3.1.5. Illustrating the action of the 20 second reset pulse on the final binary counters in the Operational Dividers.

The sixteen inverted outputs are on pins 9 to 25 inclusive of A3A11/PL1.

Four groups of the inverted outputs drive external circuitry. These are as follows:

1. Pins 9 to 23, $\overline{A5}$ to $\overline{B19}$ inclusive

   These outputs are used by part of the Numeral Generation Circuitry for commutation of the Chronometer outputs and derive a four-bit BCD code used to generate the horizontal segments of the numerals. (See Section 3.6.)

2. Pins 9 to 13, $\overline{A5}$ to $\overline{A10}$ inclusive

   These outputs drive circuitry, located on A3A12, which is part of the Control System and Signal Processing System (see Sections 3.7 and 3.5).

3. Pins 15 to 25, $\overline{C10}$ to $\overline{D19}$ inclusive

   Provides a naturally advancing 10-bit binary number for frequency scan operation of the Frequency Synthesizer.

4. Pins 22 to 25, $\overline{A19}$ to $\overline{D19}$ inclusive

   These outputs go to the Control Logic, A3A8, for circuitry which derives the X-blank pulse for the Ionogram display and portion of the NI-changeover pulse (see Section 3.7).

In addition, pin 14 (B10) goes to A5A1 to offset the CRT deflection during the NI display (see Section 3.8).

3.1.8 Additional outputs and circuitry

The Operational Clock provides a further five outputs, these being derived from the other circuitry on A3A11. The circuitry and outputs are as follows:

1. The Graticule Generator provides pulses to brighten the CRT trace at the appropriate times to 'write' the graticule on the Ionogram. These pulses are derived by gating various outputs from the Operational Dividers. An output from the Graticule Generator also provides pulses for the X-Blank Generator in the CONTROL LOGIC (A3A8).

2. The Transmit Pulse Generator provides 40μS, TTL level pulses for the TRANSMITTER. It also provides an output that controls the operation of the SIGNAL PROCESSING CIRCUITRY.

3. The Y-Blank Generator provides a pulse to the CONTROL LOGIC that allows the CRT trace to be unblanked (brightened) only during the first 5.333mS of the 6mS Y-sweep of the Ionogram holding the trace blanked between sweeps (see Section 3.8).

4. The Camera Drive Generator. The camera motor is a DC motor that normally runs at a speed which is too fast for this application. Its speed is reduced by pulsing the motor drive voltage. This circuit provides a 15.33mS pulse at the end of each 21.33mS period which allows the camera motor to operate at the required speed.

In addition to this function, the same waveform is used as the Y MAIN timebase reset and to generate the X A-SCAN reset in conjunction with the B10 output from the Operational Dividers (see Section 3.8).

3.1.9 The Graticule Generator

The graticule and the time relationships are illustrated in figure 3.1.6.

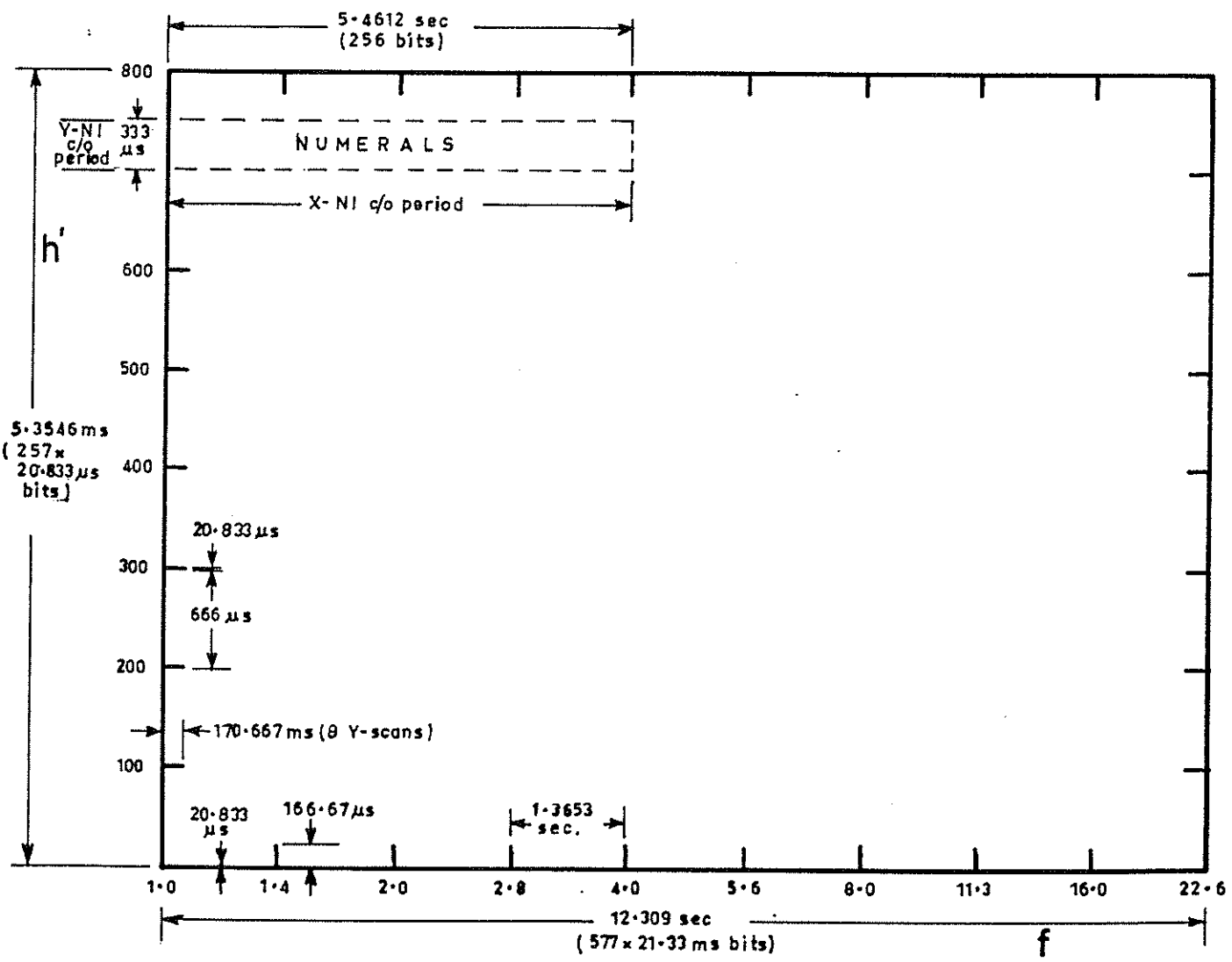


FIG. 3. 1. 6. IONOGRAM GRATICULE.

On drawing CD-225Y1, a series of NAND-gates and AND-gates grouped together in two columns is designated the GRATICULE GENERATOR. To the left of these is a series of AND-gates which gate together outputs of the Operational Dividers to drive twelve inputs to the Graticule Generator gates. IC's 3, 4, 9, 8, 14 and 17 provide gates for this part of the circuit. The Graticule generator input lines are marked 0 to Z. An additional input enters via pin 30 and comes from the Primary Dividers on A3A5. This input is designated N, making a total of 13 inputs to the Graticule Generator.

The left hand row of gates in the Graticule Generator, on dwg CD-225Y1, are two-input AND-gates involving IC's 3, 8, 9, 12, 14 and 18, which produce inputs for the eight, two-input NAND-gates on the right (involving IC7 and IC13) to produce the graticule brightening pulses in parallel form.

The AND-gates drive eleven inputs to the NAND-gates of IC7 and IC13, some gate inputs being paralleled. These eleven inputs are designated A, B, C, D, E, F, G, H, J, K, L. The outputs of IC7 and IC13 are designated 1 to 8 on drawing CD--225Y1. Each of these lines carry pulses which write the parts of the graticule as follows:

Line 1	Frequency markers, bottom line (zero range)
Line 2	Frequency markers, top line (max. range)
Line 3	Bottom border line
Line 4	Top border line
Line 5	Right hand border line
Line 6	Left hand border line
Line 7	Height markers, left hand
Line 8	Height markers, right hand

The individual circuits that derive the waveforms for the Graticule Generator inputs 0 to Z, and each input waveform appear in drawings GC-28Y1, GC-28Y2 and GC-28Y3.

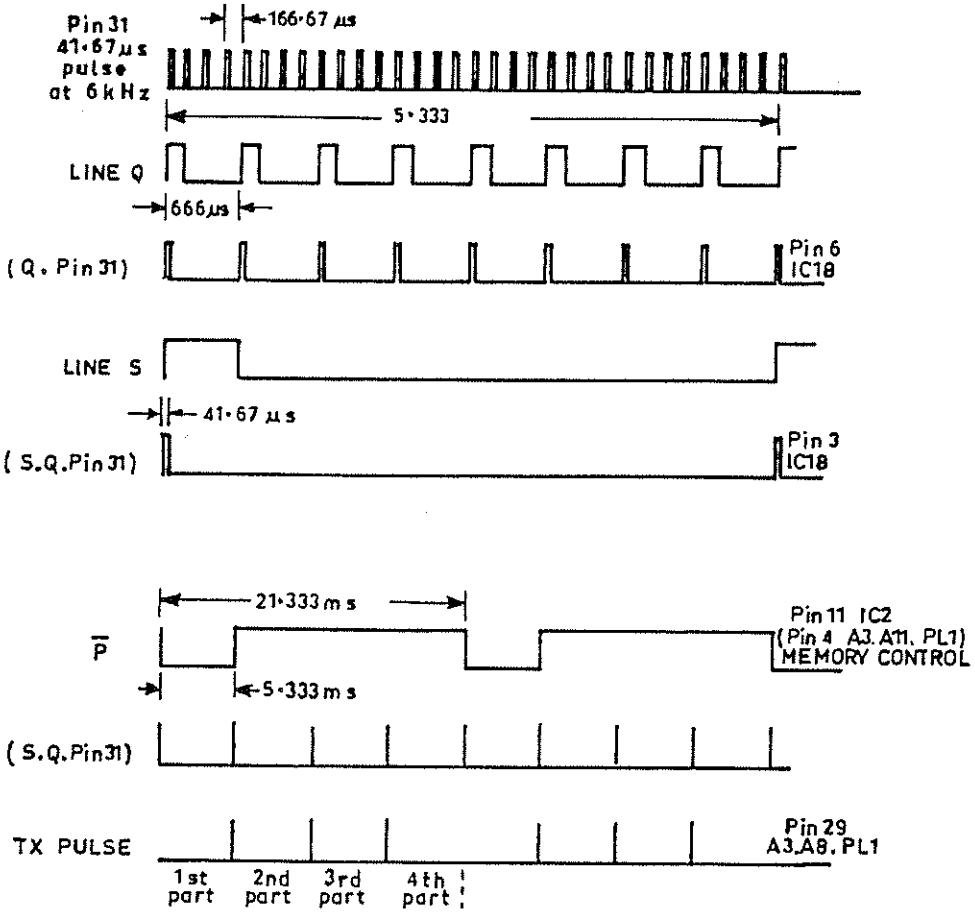
The waveform on input N and the NAND-gate inputs A to L are illustrated in drawing GC-29Y1. The waveforms on the output lines 1 to 8 are also included.

The left hand border line of the graticule is blanked between 700 km and 750 km so that the first numeral in the ident and date/time numeral display on the ionogram is not obscured. The NI-changeover pulse (from pin 6, A3A11/PL1) and the graticule pulses are gated together in a two-input NAND-gate (one gate of IC2) to achieve this.

3.1.10 The Transmit Pulse Generator

This portion of the circuitry on A3A11 involves three AND-gates from IC18 and one NAND-gate from IC2 which functions as an inverter, inverting the waveform on input line P, which becomes P. The 41.66μS pulses generated from the Primary Dividers on A3A5 enter on pin 31 of A3A11/PL1. Three other inputs, Q, S and P, come from the Graticule Generator inputs. The result is a group of three 41.66μS pulses at 5.33mS intervals followed by a gap of 10.66mS. There is no transmit pulse in the '1st part' of the transmit pulse sequence. The waveforms are illustrated in figure 3.1.7. The transmit pulses output on pin 29 of A3A11/PL1.

The inverted wave form of input P (P) becomes the '1st part Control Pulse' for the SIGNAL PROCESSOR on A3A11.



TRANSMIT PULSE GEN. TRUTH TABLE.

PL1 Pin 31	Q	S	IC18 Pin 3	$\bar{P}$	PL1 Pin 29	
1	1	1	1	0	0	Portion of 1st part
0	1	1	0	0	0	
0	1	1	0	0	0	
0	1	1	0	0	0	
1	1	1	1	1	1	TX pulse in 2nd, 3rd or 4th part.
0	1	1	0	1	0	
0	1	1	0	1	0	
0	1	1	0	1	0	
1	0	0	0	1	0	Between pulses.
0	0	0	0	1	0	
0	0	0	0	1	0	
0	0	0	0	1	0	

FIG. 3. 1. 7. Derivation of Transmit Pulse.

3.1.11 The Y-Blank Generator

This is one NAND-gate from IC2. One input is output line 4 of the Graticule Generator, the other input being P. The output goes via pin 3 of A3A11/PL1, to the CONTROL LOGIC (A3A8) portion of the Control System (see Section 3.7). The waveforms are illustrated in figure 3.1.8.

3.1.12 The Camera Drive Generator

This is one AND-gate from IC3. One input is the inverted waveform from input line E ($\overline{E}$) using one NAND-gate from IC2 connected as an inverter. The other input is $\overline{P}$. The output goes via pin 28 of A3A11/PL1 to the Camera motor via the PROGRAM unit, A5A1. The waveforms are illustrated in figure 3.1.9. The Y-MAIN and the X A-SCAN timebases are located on A5A1 and conveniently use this waveform to reset the sweeps (see Section 3.8).

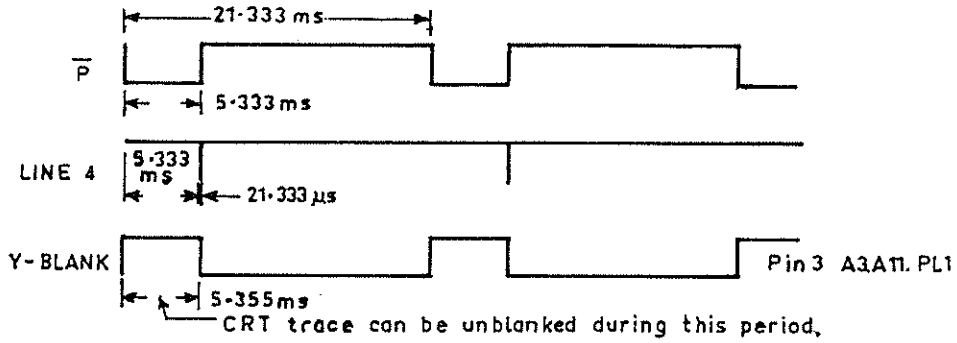


FIG. 3.1.8. Derivation of Y-BLANK

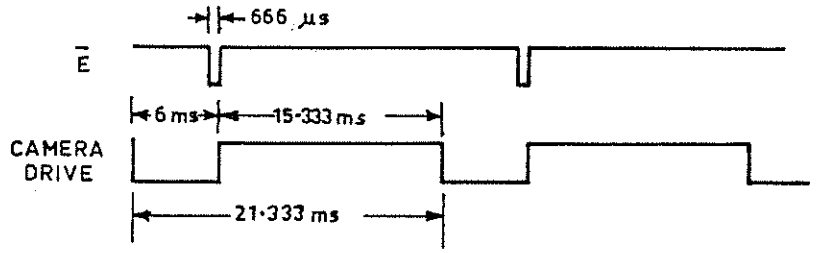


FIG. 3.1.9. Derivation of Camera Drive.

3.1.13 THE CHRONOMETER

(Dwgs: CB-34Y1, CD-224Y1, CD-221Y1, CD-220Y1, CD-218Y1)

The Chronometer circuitry is spread across five of the plug-in printed circuit cards, these being A3A5, A3A7, A3A3, A3A2 and A3A1 (refer CB-34Y1).

The divider chain is driven by the 1pps output of the Secondary Dividers on A3A5.

Each of the Chronometer Dividers produces a group of four-bit BCD numerals representing the date, time, etc., numbers. The numerals of each number are multiplexed in sequence onto four output lines common to each of the Divider assemblies A3A5, A3A7, A3A3, A3A2 and A3A1. These four common lines go to the 'Numeral Input' of the NUMERAL GENERATOR A3A4. The numerals

are then written on the CRT in the required sequence. The 'tens' numeral of each number is written first, followed by the units, except for the Days Divider output where the 'hundreds' numeral precedes them as it is a three figure number.

The Variable Number and Station Number are also multiplexed on to the four common output lines. These appear on the ionogram preceding the date/time numbers. For the 'Numeral Indication ' (NI Display) the Station Number is replaced by the Seconds from the Chronometer. This action, and the multiplexing of the numerals is accomplished by the COMMUTATION GENERATOR located on A3A6 and A3A10. (See Section 3.6)

3.1.14 The Seconds Dividers (Dwg: CD-227Y1)

This is the first stage of the Chronometer Dividers and comprises IC1 and IC2 on A3A5. IC2 is a type 7490 decade counter. The 1pps output from IC3 drives the input of IC2 which produces a 0.1pps output to IC1, a 7492 divide-by-12 counter. Only the $\div 6$ portion of IC1 is used, producing a one-pulse-per-minute output (1ppm). The A, B, C and D outputs of IC2 present a four-bit BCD code representing the 'units' of seconds. This is multiplexed onto the four common output lines, pins 2, 3, 4, 5 of A3A5/PL1, via quad NAND-gates IC9 and IC10. Only the A, B and C outputs of IC1 are required to represent the 'tens' of seconds. This output is multiplexed onto the four common output lines via the quad NAND-gates IC8 and IC10. See Section 3.1.16 for the operation of the output multiplexing circuitry.

To set the Seconds Dividers to a given time the dividers IC3, IC2 and IC1 are all set to zero by operating S1. This causes the 'reset 1' terminal of each divider to go HI resetting each divider to zero. If S1 is held operated, the outputs of each divider remain at zero allowing the Chronometer to be synchronised to a time standard (e.g. VNG, WWV, etc.).

3.1.15 Seconds Dividers Auxiliary Outputs

There are four auxiliary outputs from the Seconds Dividers.

(a) The A output of IC2 is inverted by one gate in IC15, acting as a buffer, and provides one pulse every other second (i.e. one second on, one second off) at pin 9 of A3A5/PL1. This is used to pulse the 'TX FAIL' warning light on the front panel of the PROGRAM unit A5A1, the pulses going via circuitry in the CONTROL LOGIC, A3A8.

(b) The B and C outputs of IC1 go to the two inputs of one NOR-gate in IC17. The output (pin 13, IC17) goes HI for the first 20 seconds of each minute. This output goes to the program decoding circuitry of the Minutes Dividers (refer dwgs: CB-34Y1 and CD-224Y1). This is designated the '1st 20 SECONDS' pulse.

(c) The D output of IC2 and the A output of IC1 go to the two inputs of one gate in IC15 (pins 1 and 2). The output (pin 3, IC15) is inverted by a further gate and goes to pin 24 of A3A5/PL1. This output goes HI from the 18th to the 20th second of each twenty seconds. This pulse is required to control the camera motor drive and shutter at the end of each programmed sounding. It goes to the Program unit, A5A1.

(d) The B, C and D outputs of IC2 and the A output of IC1 go to four inverters made up from gates in IC14. This IC is a type 7401 quad NAND-gate with open-collector outputs. The resultant is a two second long pulse at the commencement of each twenty seconds. It resets the OPERATIONAL DIVIDERS on A3A11, passing via pin 26 of A3A5/PL1.

Each twenty seconds is called the "sounding period" as it is possible for the ionosonde to execute a sounding during these periods. However, if a sounding is initiated, the Transmitter will not be pulsed and the display will not commence until the end of the first two seconds in a twenty second sounding period.

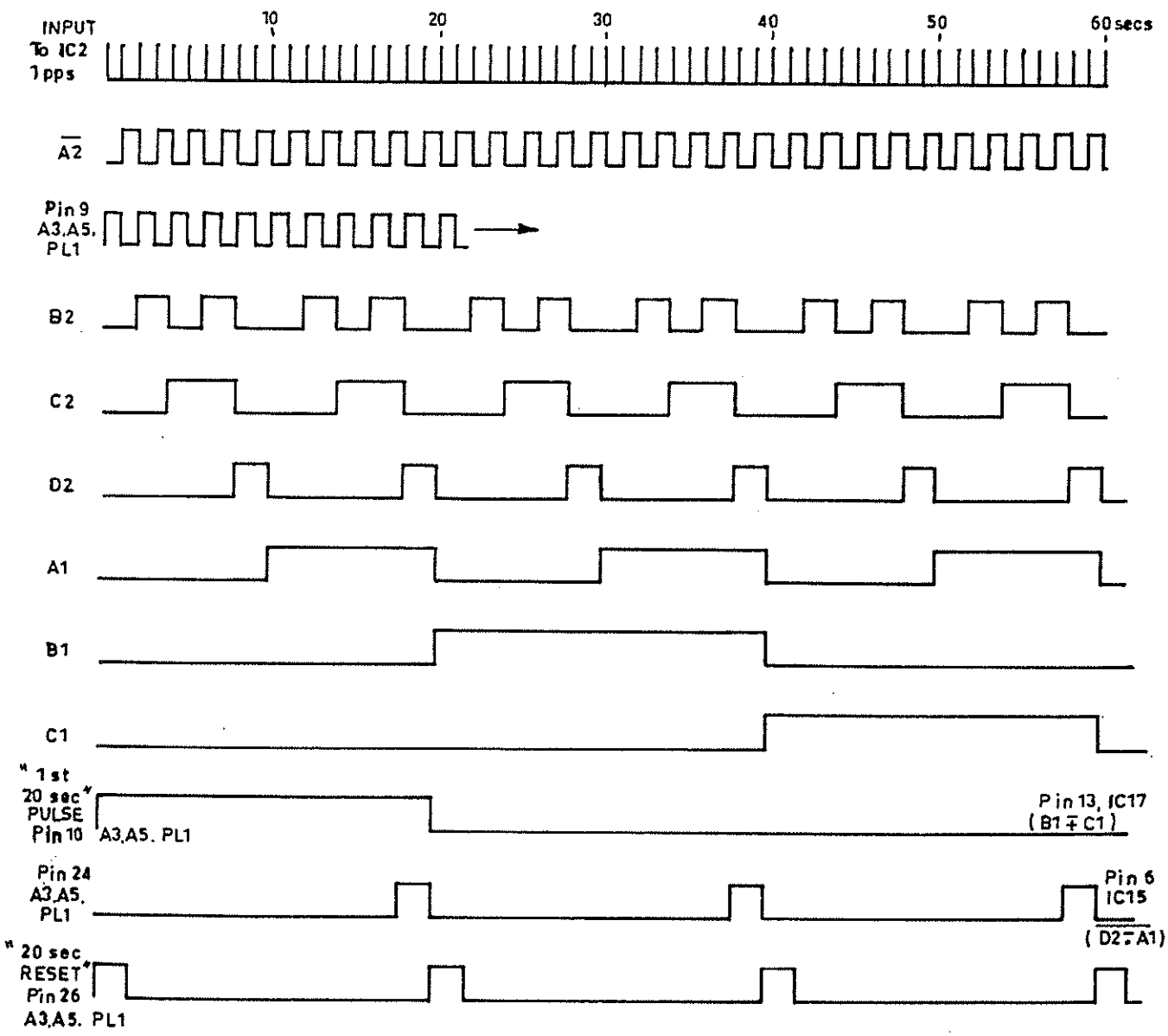


FIG. 3.1.10. Pulse Diagrams Seconds Dividers.

3.1.16 Chronometer Dividers Output Multiplexing

Each stage of the Chronometer has a four-bit BCD output indicating the date, time, etc. (in parallel form) as mentioned previously. These outputs are multiplexed in sequence onto four lines which go to the Numeral Generator input. The circuitry to accomplish this is essentially the same for each stage of the Chronometer. The general form is shown in figure 3.1.11.

A number of quad two-input NAND-gates having open-collector outputs are used. The gates of IC1 drive the four output pins 2, 3, 4, 5. Four inputs of IC1, designated A, B, C, D, are driven by the outputs of IC2 and IC3. The other inputs are commoned and go to the 'enable output' pin which is driven by the Commutation Generator A3A6.

The four-bit BCD output of the TENS divider of the particular stage of the Chronometer goes to the inputs P, Q, R, S of IC2. The other inputs are commoned and go to the 'enable tens' pin which is driven by the Commutation Generator. Similarly, the BCD output of the UNITS divider of the particular Chronometer stage goes to inputs T, U, V, W of IC3, the other four inputs being driven by the Commutation Generator via the 'enable units' pin. -

When a number from the particular stage of the Chronometer is not required, the 'enable output' pin is held LO by the Commutation Generator causing the outputs of each gate in IC1 to go HI, "pulled up" by the resistors R1, R2, R3, R4. With a HI (or 1) on each output line, the Numeral Generator produces a blank, or no output, and nothing is displayed on the CRT for the period that the pins 2, 3, 4, 5 remain HI.

The Commutation Generator selects each number to be displayed by driving the 'enable output' pin HI on each Chronometer stage in sequence. Each gate in IC1 will act as an inverter for the levels on each of the inputs A, B, C, D. The highest value numeral is displayed first so the Commutation Generator next drives the 'enable tens' pin HI. The BCD data on the inputs

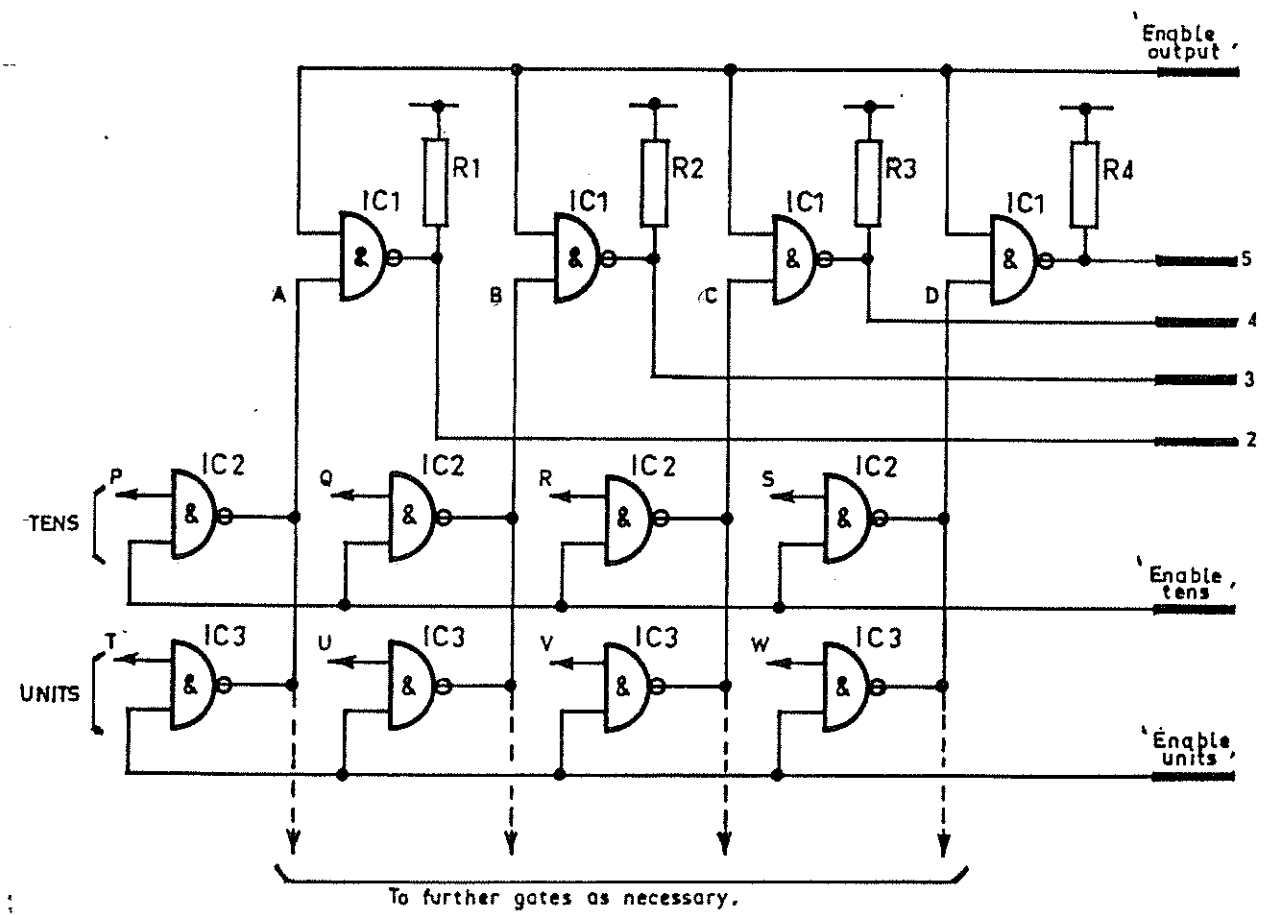


FIG. 3. 1. 11. Chronometer Dividers Output Multiplexing circuitry.

P, Q, R, S of IC2 is then inverted at the outputs of each gate in IC2 which drives the A, B, C, D inputs of IC1 which inverts this again. Thus, the four-bit BCD numeral from the particular Chronometer divider output appears on the output pins 2, 3, 4, 5. The Numeral Generator then causes the particular numeral to be displayed.

Following the display of the tens numeral, the Commutation Generator then drives the 'enable units' pin HI and the 'enable tens' pin LO. The units BCD numeral on T, U, V, W is then passed to the output pins 2, 3, 4, 5 in a similar fashion to the tens numeral.

When the number for the particular Chronometer divider stage has been displayed, the Commutation Generator then drives the 'enable output' pin LO and selects the next stage in the sequence.

Other numerals, and blanks, are added by adding further gates to drive the A, B, C, D inputs of IC1 as indicated in figure 3.1.11.

The overall arrangement and selection of the Chronometer outputs for the numeral display are presented schematically in drawing CB-30Y1.

3.1.17 The Minutes Dividers (A3A7)
(Dwg: CD-224Y1)

The one-pulse-per-minute (1ppm) output of the Seconds Dividers enters the Minutes Units divider IC9, via a circuit which adds an extra pulse to advance the count when the switch S1 is operated. This 'advance count' circuit is used in each subsequent stage of the chronometer dividers to enable the Chronometer to be set to the required time. The operation of this circuit is explained in paragraph 3.1.18 following.

IC9 and IC8 are type 7490 decade counters. Each is reset to zero at the end of sixty minutes. One gate in IC7 nands the B and C outputs of IC8 producing a positive-going pulse which is inverted to reset IC8 and IC9. This action is illustrated in figure 3.1.12. The B and C outputs would normally be as shown by the dotted lines. The reset action reverses their condition with a delay of several nanoseconds producing a very narrow pulse at the end of minute 60, resulting in an output of one-pulse-per-hour from the C output of IC8.

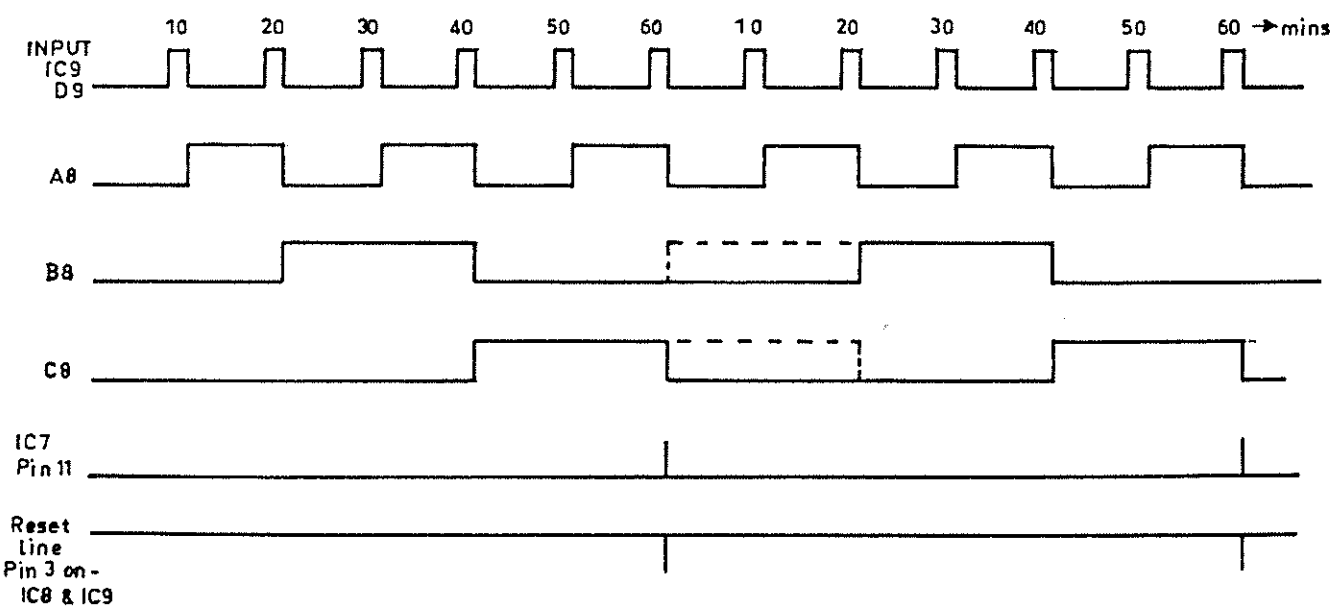


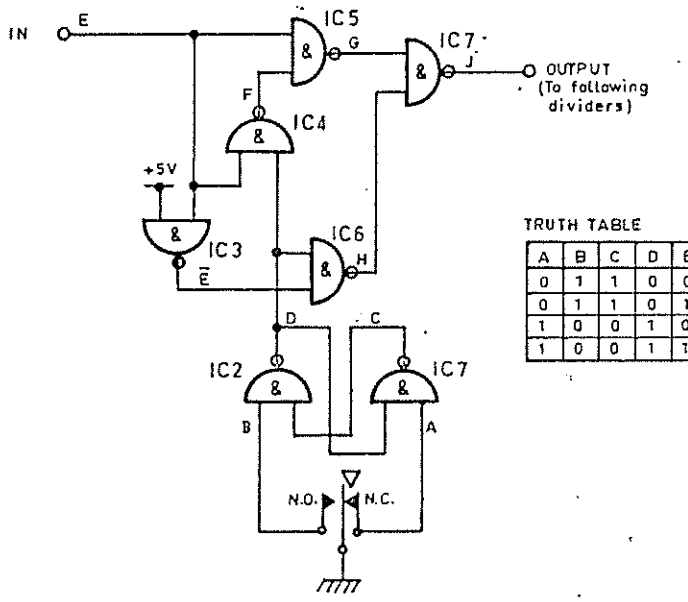
FIG. 3.1.12. Chronometer Minutes Divider reset action.

3.1.18 The 'Advance Count' circuit

The 'advance count' circuit is illustrated in figure 3.1.13. Seven NAND-gates are used, IC1 and IC2 forming a 'SET-RESET', or S-R flip-flop to 'debounce' the pulse from the contacts of S1.

When S1 is not operated, the output of the S-R flip-flop, D, is LO and the incoming pulses are transferred to the output, J, via IC5 and IC7.

If S1 is then operated momentarily while the input (E) is LO, J will go HI momentarily, adding an extra pulse to the incoming pulse train. As a divider is driven via this circuit, it will advance its count by one on the negative-going edge of the extra pulse, i.e. when S1 is released. If S1 is held operated the incoming pulses will be merely inverted at the output, J.



TRUTH TABLE

A	B	C	D	E	Ē	F	G	H	J	
0	1	1	0	0	1	1	1	1	0	When A=0 J=E
0	1	1	0	1	0	1	0	1	1	
1	0	0	1	0	1	1	1	0	1	When A=1 J=Ē
1	0	0	1	1	0	0	1	1	0	

FIG. 3. 1. 13. The 'Advance Count' circuit.

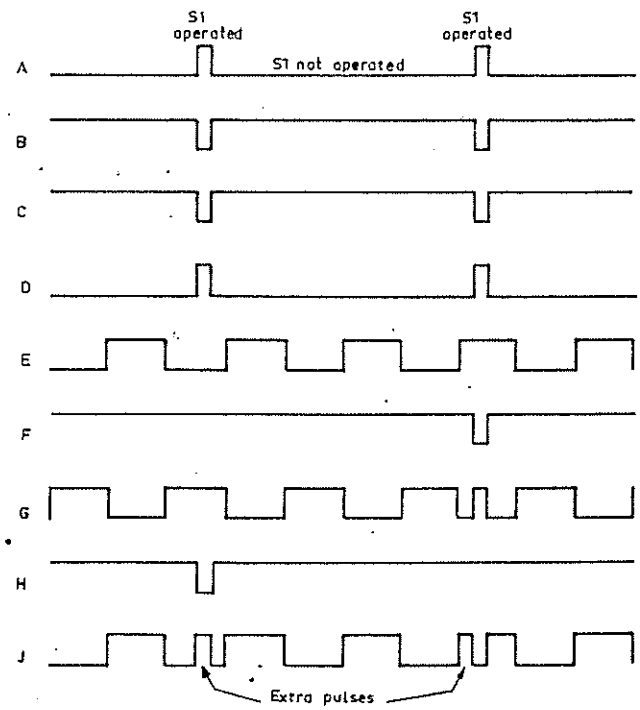


FIG. 3. 1. 14. Pulse diagrams for Advance Count circuit.

If S1 is operated momentarily while E is HI, J will go LO momentarily, the following divider advancing its count by one the moment S1 is operated.

The action of S1 is illustrated in the pulse diagram of figure 3.1.14. The truth table for the advance count circuit is in figure 3.1.13.

3.1.19 Program Decoding Circuitry

Pulses used to program the operation of the ionosonde are derived by circuitry on A3A7 involving IC5, IC10, IC11, IC12, IC13 and IC14. This circuitry produces 20-second long output pulses at intervals of 1 minute, 5 minutes and 15 minutes to three pins on A3A7/PL1.

IC11 and IC12 are type 7442 four-bit BCD-to-decimal decoders. The BCD output of the first decade divider (IC9) is decoded by IC12. The '0' output of IC12 (pin 1) goes LO for the zero minute or commencement of the count. The '5' output (pin 6) goes LO for the fifth minute. Similarly IC11 decodes the BCD output of IC8, the MINUTES TENS divider. The '0' output goes LO from zero to ten minutes, the '1' output goes LO from ten to twenty minutes, the '3' output goes LO from thirty to forty minutes and the '4' output goes LO from forty to fifty minutes.

The 5 MIN output is produced by nanding the 0 and 5 outputs of IC12 in one gate from IC5. This produces pulses of one minute duration every five minutes, i.e. at minutes 0, 5, 10, 15, 20, 25 etc. This output (pin 11, IC5) is then nanded in another gate from IC5 with the 'lst 20 SECS' pulses producing pulses of twenty seconds duration at minutes 0, 5, 10, 15 etc. on pin 15 of A3A7/PL1. This operation is illustrated in figure 3.1.15.

The 1 MIN output (pin 9, A3A7/PL1) is produced by inverting the lst 20 SECS pulses.

The 15 MIN output is produced by nor-ing appropriate outputs from IC11 and IC12 to produce pulses of one minute duration at 0, 15, 30 and 45 minutes on four separate lines from pins 13, 10, 1 and 4 respectively, of IC14. Each of these is then strobed by the lst 20 SECS pulses in four gates (IC13), reducing the duration of each of the pulses to twenty seconds. A four-input NAND-gate, IC10, combines them then in serial form, the output appearing on pin 6 of A3A7/PL1. Refer also the figure 3.1.15 for the pulse diagrams.

In addition, two further outputs are provided for the PRESET PROGRAM unit A3A9 which is an optional unit not normally included in the equipment. Two gates from IC15 derive inputs from appropriate output lines of IC14. The outputs of these two gates are subsequently inverted producing pulses of one minute duration at minutes 15 and 45 (pin 2, A3A7/PL7), and minute 30 (pin 3, A3A7/PL1).

3.1.20 The Hours Dividers (A3A3)
(Dwg: CD-221Y1)

Two type 7490 decade counters are used in this circuit. Both counters are reset to zero at the end of each 24 hours. The 1ppm from the Minutes Dividers enters IC2 via an 'advance count' circuit. The hours units advance by one when S1 is operated. The output of IC2 drives IC1 via another advance count circuit which enables the hours tens to be advanced by operating S2. The C output of IC2 and the B output of IC1 are nanded together and the resulting pulse inverted to produce a negative-going reset pulse at the end of the 24th input pulse. This operation is illustrated in the pulse diagrams of figure 3.1.16 and is similar to the reset action for the Minutes Dividers.

The BCD output code multiplexing differs from that for the other dividers in that the Minutes numerals code is multiplexed onto the output lines (pins 2, 3, 4, 5 of A3A1/PL1) immediately following the Hours numerals via common circuitry spread across the two assemblies A3A7 and A3A3. Commutation for the Minutes output multiplexing is derived via IC10 on the Hours Dividers.

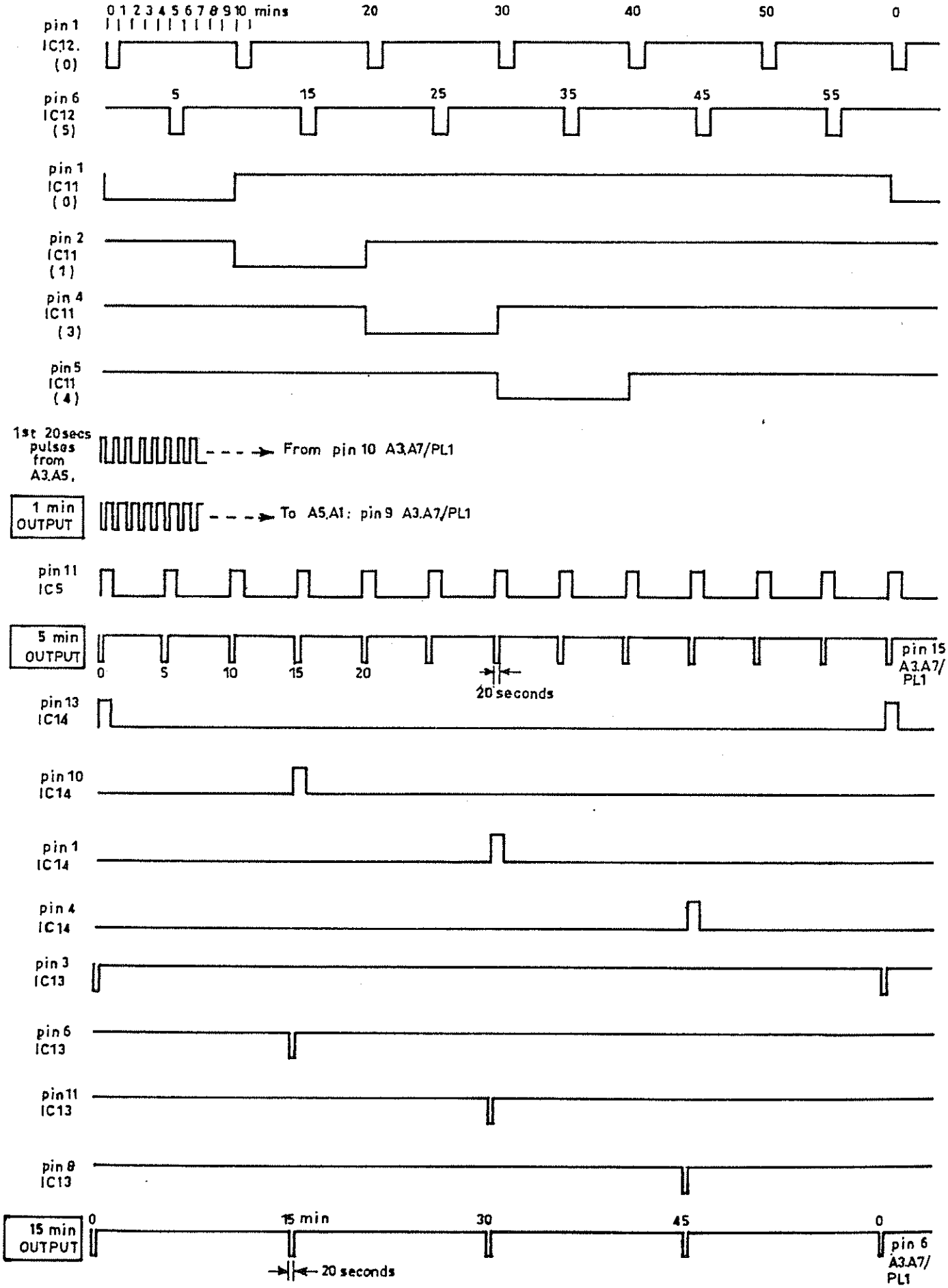


FIG. 3. 1. 15. Derivation of Program Pulses.

In addition, a six-bit BCD output from IC1 and IC2 is provided for the PRESET PROGRAM unit A3A9 (optional) via IC11, a hex-buffer/driver).

The 1-pulse-per-day output is taken from the B output of IC1 and goes to the Days Dividers via pin 25 of A3A3/PL1.

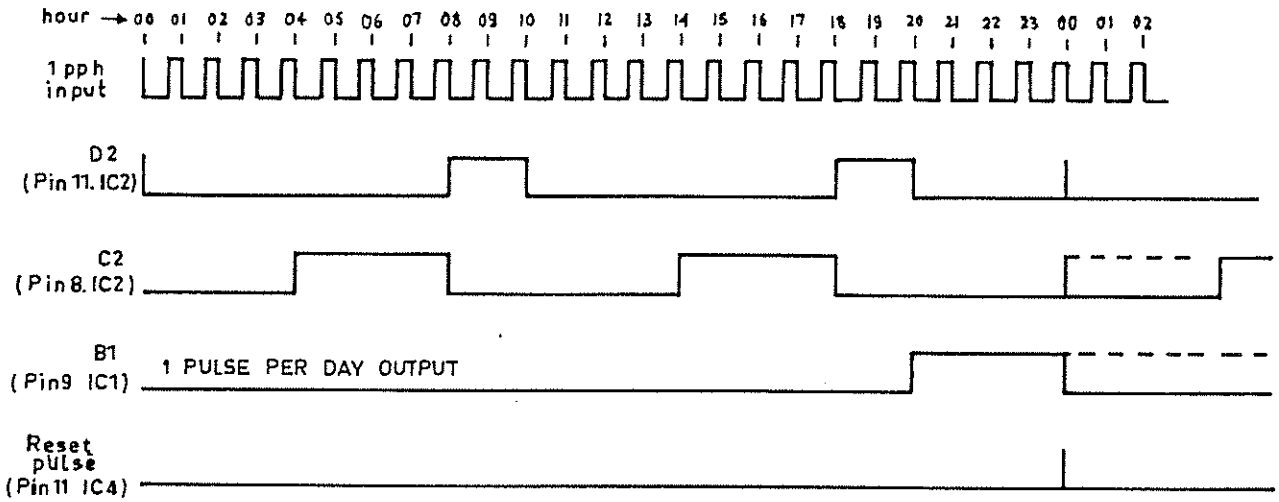


FIG. 3.1.16. Hours Dividers reset action.

3.1.21 The Days Dividers (A3A2)
(Dwg: CD-220Y1)

This consists of three type 7490 decade counters in a chain, IC3, 4 and 5. The input to each counter is preceded by an advance count circuit so that the units, tens and hundreds digits may be set.

This unit provides a three digit number for each day of the year commencing at 001 for January the 1st and ending on 365 for December the 31st, except for leap years which have 366 days.

The divider chain is reset to 000 at the commencement of the 366th input count each year, or the 367th each leap year. The reset pulse is generated by IC6, an eight-input NAND-gate (7430). When all inputs are HI, the output (pin 8, IC6) goes LO, this is then inverted by IC7 providing a positive-going pulse to reset the dividers IC3, 4 and 5. As the divider chain resets within a few nanoseconds of the output of IC6 going LO, the reset pulse is very narrow.

The pulse from the output of IC6 also passes through a series of ten inverters, delaying the pulse about 100nS. This delayed pulse then appears as an extra pulse, following the 366th input pulse, at the input of the first divider IC3, via a NAND-gate (from IC16). Thus, the count advances from 000 to 001 about 100nS following resetting of the divider chain.

The overall operation is illustrated in the pulse diagrams of figure 3.1.17. The reset action for non-leap years is illustrated in figure 3.1.18. During non-leap years, the 'leap year reset input' (pin 28, A3A2/PL1) is held LO from circuitry located on A3A1. This causes pin 11 of IC2 to remain HI during non-leap years, allowing the reset pulse to occur at the beginning of the 366th input pulse as illustrated in figure 3.1.18. During a leap year, the 'leap year reset input' goes HI and the A output pulses from IC3 will appear on pin 6 of IC6. Consequently, all the inputs to IC6 will then only go HI at the beginning of the 367th input pulse allowing for the extra day in a leap year. This is illustrated in figure 3.1.19.

The B output of IC5 provides the 'one pulse per year' (1ppy) output, going high on day 200 and remaining high until the dividers are reset. This output goes to the Years Divider A3A1 via pin 26 of A3A2/PL1.

The BCD output of each divider is multiplexed through to the common output lines as discussed in section 3.1.16 via IC10, 11, 12 and 13. IC13 provides a blank before the first digit of the days number displayed.

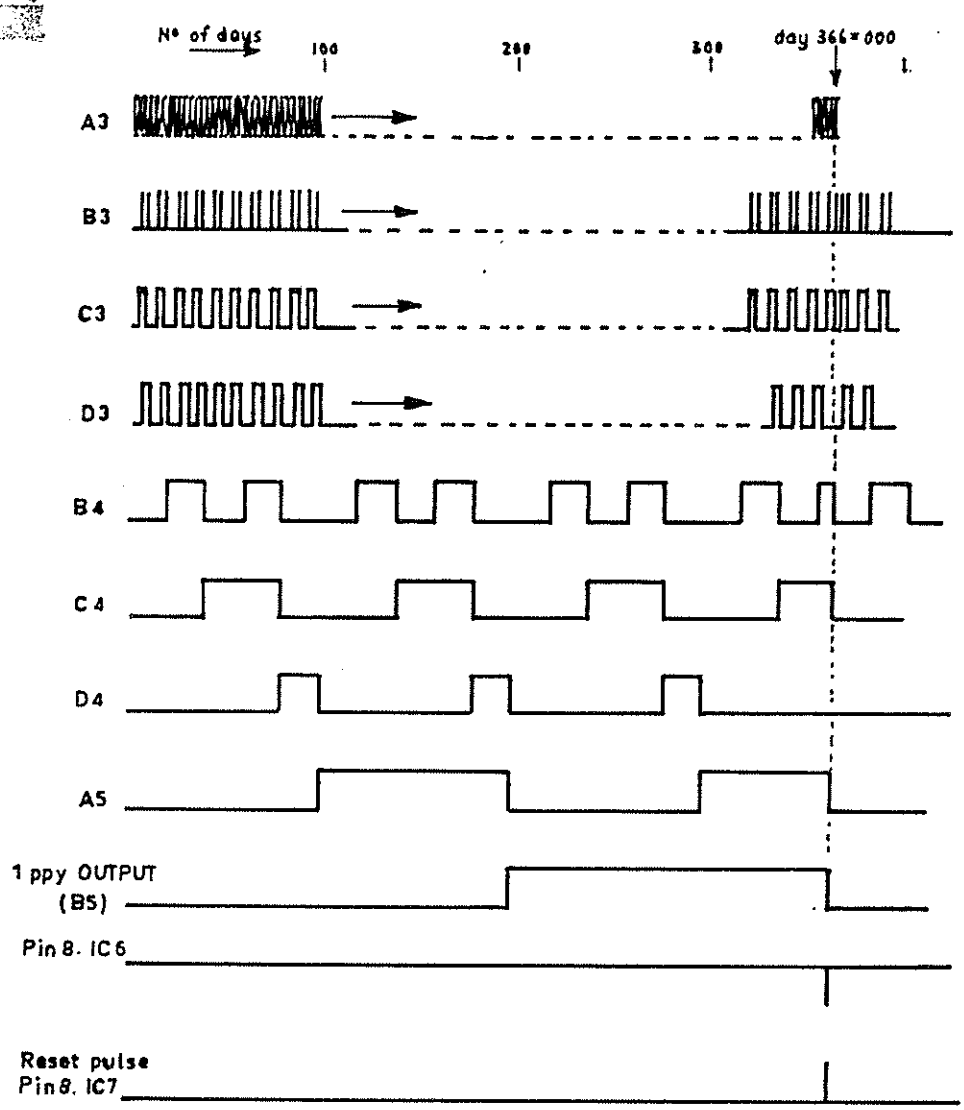


FIG. 3.1.17. Days Dividers pulse diagrams.

3.1.22 The Years Divider (A3A1)
(Dwg: CD-218Y1)

A single 7490 decade counter, IC8, comprises the Years Divider. The 1ppy output of A3A2 enters the input of IC8 via an advance count circuit enabling the 'Years Units' digit to be set. The BCD output of IC8 only provides the units digit of the years number displayed. The BCD code for the tens digit is hard wired on the inputs of IC3 (in the output multiplexing circuitry) to produce a 7 in the numeral display for the 70's decade. This board is replaced at the end of each decade, (i.e. replacement due in 1980).

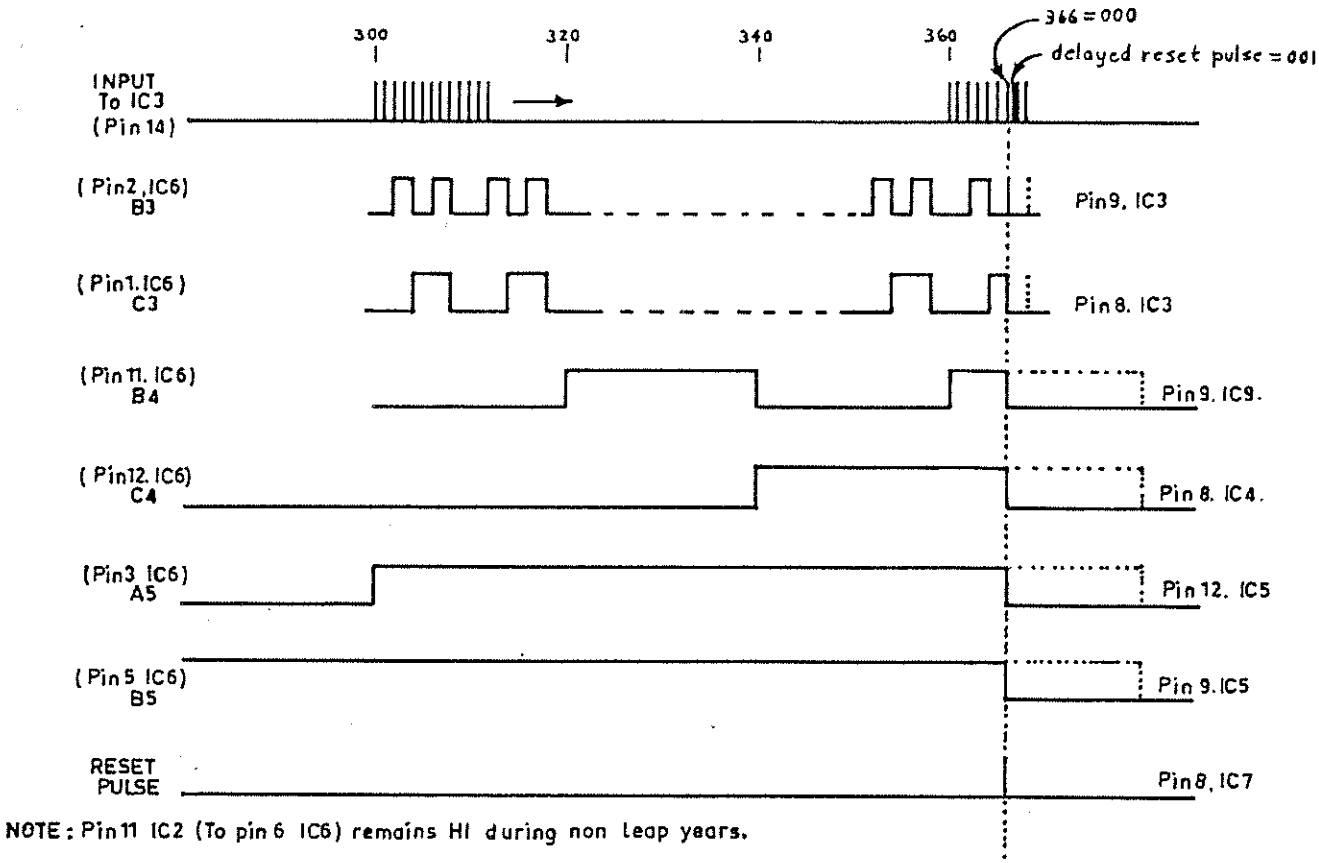


FIG. 3.1.18. Days Dividers reset action in non-leap years.

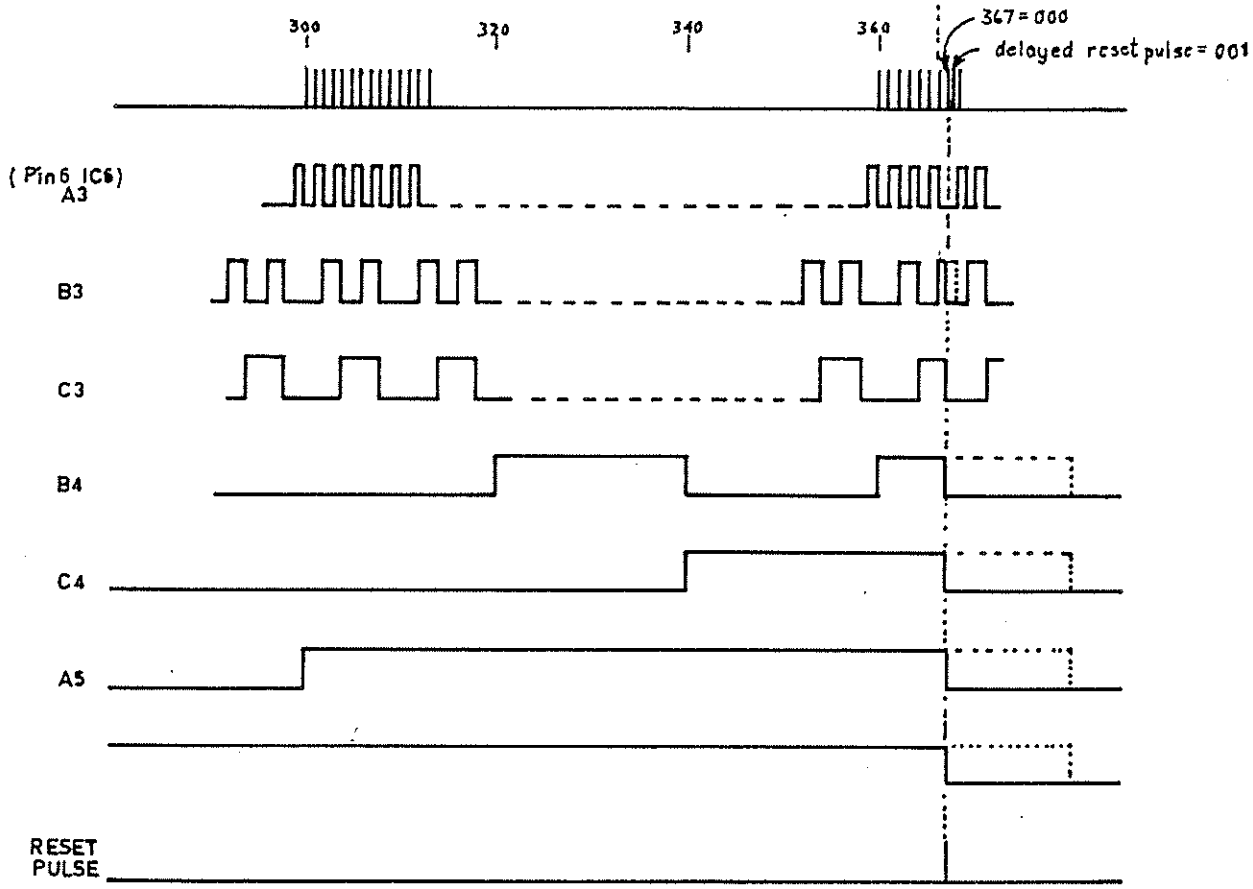


FIG. 3.1.19. Days Dividers reset action during leap years.

Two four-input NAND-gates (IC10) generate the 'Leap-Years-Reset' output. The A, B, C and D outputs from IC8 are nanded so that pin 6 of IC10 goes LO during 1972. The A, B, C and D outputs from IC' are nanded so that pin 8 of IC10 goes LO during 1976. The outputs from pin 6 and pin 8 of IC10 are nanded in one gate from IC9, the output of which (pin 3) goes HI in 1972 and 1976 as required. The 'Leap-Years-Reset' output appears on pin 28 of A3A1/PL1 and goes to the Days Dividers A3A2. The generation of this output is illustrated in figure 3.1.20.

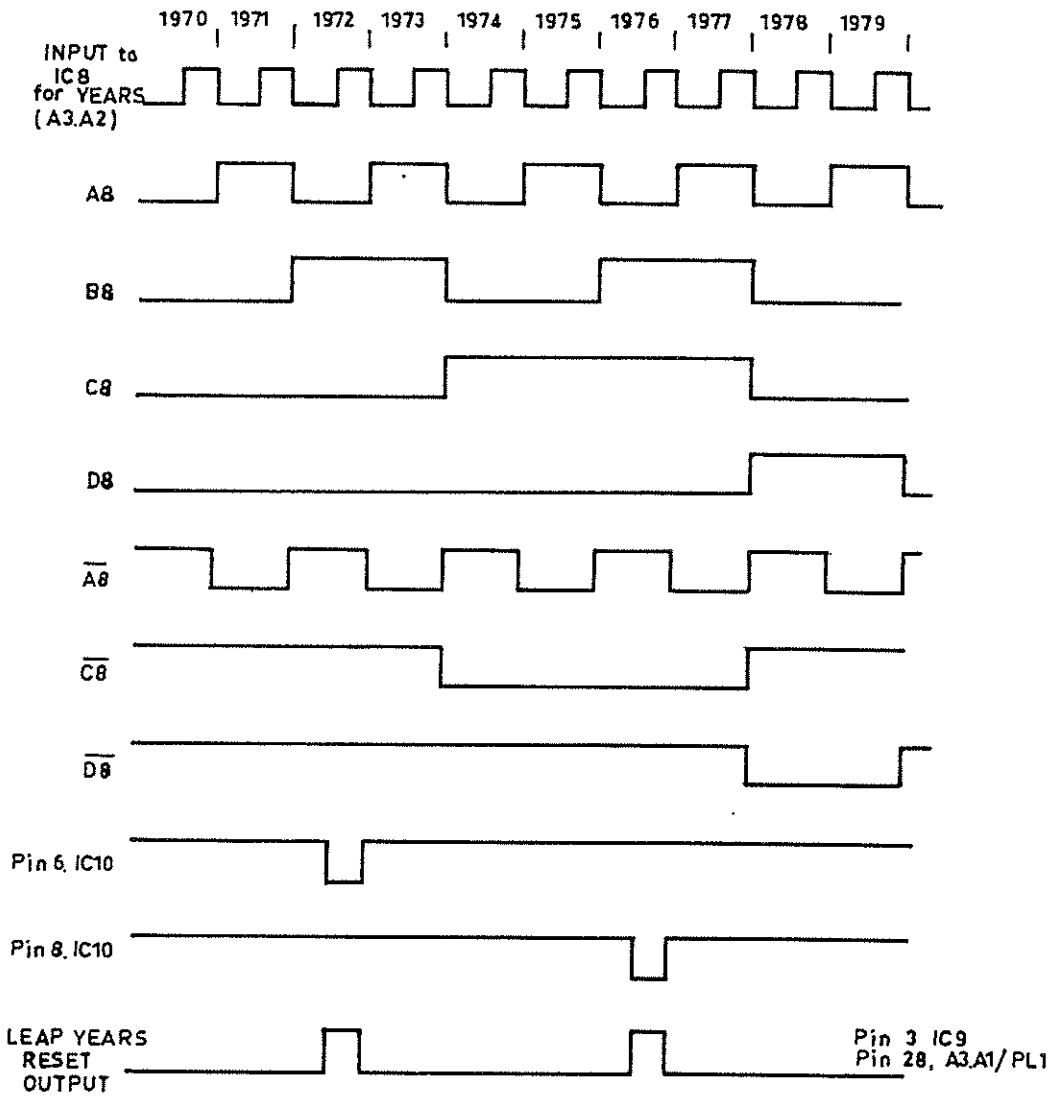


FIG. 3. 1. 20. Derivation of the Leap Years Reset output.

3.2
FREQUENCY SYNTHESIZER

Par. No.	Title	Drawing No.
3.2.1	Introduction	
3.2.2	Brief Description	CB-29Y1
3.2.3	THE DIGITAL SECTION	CD-232Y1 (A4A1)
3.2.4	The Octave Divider	" " "
3.2.5	Programmable Divider A	" " "
3.2.6	Programmable Divider B	" " "
3.2.7	The Digital Comparator	" " "
3.2.8	THE RF SECTION	CD-232X2 (A4A2)
3.2.9	The VFO and Steering Circuitry	" " "
3.2.10	70 MHz Oscillator and Mixer	" " "
3.2.11	The Digital Interface Circuit	" " "
3.2.12	The Pulse Modulator	" " "
3.2.13	The Reference Oscillator	" " "
		(also refer CD-232Y3)

3.2.1 Introduction

The Frequency Synthesizer provides the RECEIVER first conversion and TRANSMITTER drive frequencies which determine the operating frequency of the ionosonde. It generates 576 logarithmically spaced frequencies (or frequency channels) covering the range from 1MHz to 22.6 MHz. The Synthesizer is controlled by a 10-bit binary number derived from the OPERATIONAL DIVIDERS outputs (on A3A11) which causes the Synthesizer to step through the 576 frequency channels during a sounding. As the channels are logarithmically spaced, a logarithmic frequency scale is provided for the ionogram. The relationship between the frequency channels and the channel number is illustrated in figure 3.2.1.

In addition, the synthesizer may be manually set to any of the 576 channels, for single frequency soundings, by setting a group of ten front panel switches.

The unit is located in the top rack assembly of the ionosonde immediately to the right of the PROGRAM unit A5. It is divided into two sections: the Digital section, A4A1 and the RF section A4A2.

A block diagram of the Frequency Synthesizer is given in drawing CB-29Y1.

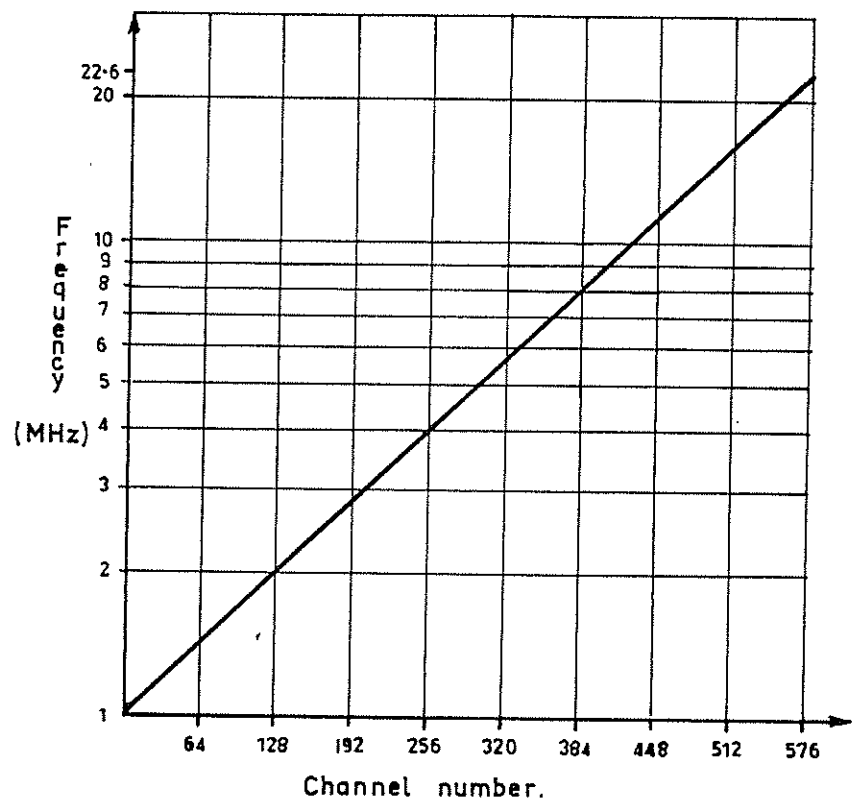


FIG. 3.2.1. Relation between ionosonde operating frequency and channel number.

3.2.2 Brief Description.

The VFO is an oscillator that covers the frequency range of 69 MHz to about 38 MHz. The frequency is controlled by the output of the digital section comparator. The VFO output provides the local oscillator signal to the first mixer of the receiver. As the receiver first IF is 70MHz, the receiver frequency range commences at 1MHz. The VFO output is also applied to a mixer and heterodyned with 70MHz from a crystal oscillator to produce the transmitter frequency range commencing at 1MHz. A filter follows this mixer to prevent unwanted

mixing products from being transmitted or passed to the digital section. The transmitter drive is modulated by the 40uS Transmit Pulse before being passed to the Transmitter input.

The CONTROL SYSTEM (see Section 3.7) terminates a sounding about 12.3 seconds after the commencement of the frequency scan, at which time the frequency has reached about 23 MHz. The operative frequency range of the VFO is thus from 69 MHz to about 47 MHz, although, as explained later, the VFO continues lower in frequency before being returned to 69 MHz at the end of a sounding period.

The filtered output from the mixer is also passed to the digital section via an interface circuit which converts the signal to digital level pulses compatible with the TTL circuitry in the digital section.

The digital section consists of the reference frequency crystal oscillator, several programmable dividers which are preset to divide by ratios according to the frequency channel required, the associated programming circuitry and a comparator circuit which controls the VFO frequency. Briefly, the VFO is set to each frequency channel in the following way:-

The Transmitted frequency (between 1MHz and 23MHz) is first divided or 'prescaled', to a basic octave frequency range of 1 MHz to 2 MHz by the Octave Divider. This divides by ratios of 1,2,4,8 or 16 depending in which octave (i.e. 1-2, 2-4, 4-8, 8-16, 16-23 MHz) the sonde operating frequency is required. Programmable Divider A then divides the Octave Divider output by a number between 309 and 436 according to whichever frequency channel is required. At the same time, Programmable Divider B has also been set to divide the reference frequency by a number between 1744 and 1236 according to the frequency channel required. Each programmable divider has a range of 128 divisors providing 128 channels in each octave.

If the VFO frequency is lower than the required frequency, then the transmitted frequency will be to high and Programmable Divider A will produce an output pulse before Programmable Divider B. This causes the comparator to 'steer' the VFO higher in frequency until the output pulses from the two programmable dividers co-incide.

Conversely, if the VFO is higher than the required frequency, the transmitted frequency will be too low and Programmable Divider B will produce an output pulse before Programmable Divider A. The comparator then steers the VFO lower in frequency until the output pulses from the programmable dividers coincide. If the VFO drifts, the same sequence occurs to correct the output frequency.

The division ratio, or divisor, of each programmable divider is changed to produce each frequency channel. This is effected by a 10-bit binary number that is obtained by setting ten front-panel switches for single-frequency soundings or a group of outputs from the OPERATIONAL DIVIDERS(on A3A11) during a frequency scan for an ionogram. The 'least-significant-bit' of the latter changes each 21.33 mS, incrementing the division ratios each Tx pulse period (i.e. each 21.33 mS) and thus each ionogram y-sweep corresponds to one frequency channel.

Programmable Divider A is an up-counter that is preset to count up from a number between 3660 and 3787, to 4096. This gives 128 divisors from 436 to 309. The programming circuits preset the divider to 3787 to obtain the first channel in each octave, incrementing this number down one, to 3686 and then to 3785-3784 etc., each 21.33 mS to establish the divisors for the succeeding channels. The counter counts up from the preset number giving an output pulse when it reaches 4096,

thus dividing the input pulses (from the Octave Divider output) by the difference between the preset number and 4096. The preset number for the first channel is 3787, providing a divisor of 309, that for the last channel being 3660 which provides a divisor of 436.

Programmable Divider B is a down-counter that counts down to zero from a preset number between 1744 and 1236. Thus the preset number gives the value of the divisor, in this case only 128 divisors are required and the programming circuit is arranged such that it increments the preset number by a factor of 4 for each channel. The divisor for the first channel in each octave is 1744, the succeeding channel being 1740 - 1736 - 1732 etc. to 1236. The divider gives an output pulse when it has reached zero.

The purpose of the gate between the reference oscillator and the input of Programmable Divider B is discussed in section 3.2.7 on the Digital Comparator.

3.2.3 THE DIGITAL SECTION A4A1 (Dwg: CD-232Y1).

This section uses TTL digital ICs throughout. All the components are situated on a double-sided printed circuit board which is located in its own separate compartment on one side of the Synthesizer chassis.

Ten, single-pole, two-position slide switches, S1 to S10, mounted on the front panel, are used to set up the binary number corresponding to a desired channel for a fixed-frequency sounding. Each is connected to switch between +5V (logical 1) when in the up position and ground (logical 0) when down, the pole of each switch going to one input on IC1, IC2 or IC3. The setting of these switches to obtain a desired channel is explained later.

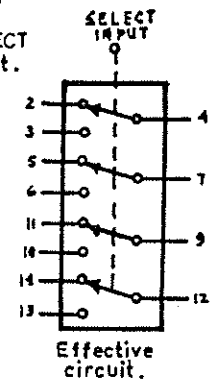
The 10-bit binary number from A3A11, required to control the synthesizer during a frequency scan, enters via pins 15 to 25 of A4A1/PL1 (with the exception of pin 17 which carries the +5V supply). Each 'bit' of the input goes to an input on IC1, IC2 or IC3.

IC1, IC2 and IC3 are type 9322 quad, two-input multiplexers. Here, the three of them are connected as a 10-pole, two-position digital switch. The truth table illustrating the operation of each IC is given in TABLE 1. In this configuration, the ENABLE input is grounded and thus the outputs are always operative. The logic level on the SELECT inputs (pin 1 of IC1, IC2 and IC3) is controlled by S11, and selects which inputs are to be routed to the output pins. When the select input of the 9322 is high (1) the inputs on pins 3,6,10 and 13 are switched to the output pins 4,7,9 and 12 respectively. When it is low, the inputs on pins 2,5,11 and 14 are switched through to pins 4,7,9 and 12 respectively. Note that pins 5,6, and 7 are not used on IC2 and IC3.

TABLE 1

	INPUTS								OUTPUTS			
	Pin 2	Pin 5	Pin 11	Pin 14	Pin 3	Pin 6	Pin 10	Pin 13	Pin 4	Pin 7	Pin 9	Pin 12
	S=1 / S=0											
IC1	S1	S2	S3	S4	$\overline{C10}$	$\overline{D10}$	$\overline{A15}$	$\overline{B15}$	$\overline{C10}$ / S1	$\overline{D10}$ / S2	$\overline{A15}$ / S3	$\overline{B15}$ / S4
IC2	S5	Not used	S7	S6	$\overline{C15}$	Not used	$\overline{A19}$	$\overline{D15}$	$\overline{C15}$ / S5	Not used	$\overline{A19}$ / S7	$\overline{D19}$ / S6
IC3	S8	Not used	S10	S9	$\overline{B19}$	Not Used	$\overline{D19}$	$\overline{C19}$	$\overline{B19}$ / S8	Not used	$\overline{D19}$ / S10	$\overline{C19}$ / S9

S is Pin 1 the SELECT input.



TRUTH TABLE for the 9322 digital switches in the Frequency Synthesizer, Digital Section (A4.A1.)

Switch S11 is a slide switch mounted on the front panel of the synthesizer. The up position is designated 'SF' for single frequency. When set to this position, the slide switches, S1 to S10 are operative and may be set so that the ionosonde then operates on whichever frequency channel is required. The down position of S11 is designated 'N' for normal operations; that is, so that a frequency scan occurs during a sounding. The circuitry controlling the selection of the two operating modes operates as follows:

Two NAND-gates from IC4 are involved. One is connected as an inverter, its inputs being tied to the pole of S11. When this is in the N position, the pole of S11 is connected to +5V and pin 11 of IC4 will drive pin 10, one input of the other NAND-gate, low. This forces the output (pin 8) of this gate high, and as this drives the select inputs of IC1, IC2 and IC3, the 10-bit binary input from A3A11 is selected to control the operation of the synthesizer.

When S11 is in the SF position, the pole is connected to pin 13 of A4A1/PL1. This is connected to contact 2 on S2D of the MONITOR function switch, which is designated 'A-Scan' in position 2. (See section 3.7 THE CONTROL SYSTEM, particularly 3.7.1 and 3.7.7). The Synthesizer can only be operated in the single frequency mode when the A-Scan function is selected.

When the monitor function switch is set to A-Scan, and S11 is switched to SF, pin 11 of IC4 will drive pin 10 high. Between programmed soundings the MAIN DISPLAY CONTROL LINE is high, and this is connected to the other input (pin 9) of the NAND-gate, pin 8 of IC4 will go low. Thus, the select inputs of IC1, IC2 and IC3 are driven low and the 10-bit binary number set up on switches S1 to S10 selects the operating frequency.

When a programmed sounding is initiated (see section 3.7.3) the Main Display Control Line goes low. This forces pin 8 of IC4 high and the synthesizer is automatically returned to normal operation to allow a frequency scan during the sounding.

IC1 and IC2 switch the first seven bits of the 10-bit binary input to IC5, IC6, IC7 and IC8. These are four-bit adders which provide the preset numbers to each programmable divider.

IC3 switches the last three bits of the 10-bit binary input to IC12. This is a type 8211 eight channel digital switch, part of the Octave Divider circuitry, also output on pin 4 of A4A1/PL1. This goes to the CONTROL LOGIC A3A8, to turn the transmitter on for a single frequency A-scan.

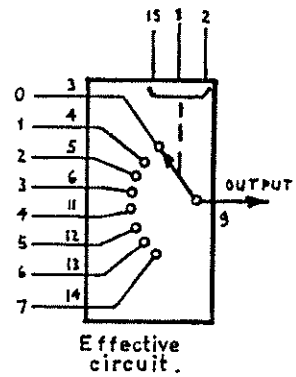
3.2.4 The Octave Divider

The transmitted frequency output from the Digital Interface circuit in the RF Section (A4A2) enters the Digital Section via terminal A. It is passed to the input of IC16 via R6 and an inverter from IC24, acting as a buffer. The Octave Divider is IC16. This is a type 74193 binary up/down counter, here used as in the down-counter mode. The output of IC24 (pin 8) drives the 'count-down' input of IC16 (pin 5). There are four outputs from IC16, these are $\div 2$, $\div 4$, $\div 8$, $\div 16$.

IC12 operates as a single-pole, eight position digital switch. It selects sequentially the input (i.e. $\div 1$), and the four outputs of IC16, controlled by the last three bits of the 10-bit control number. During a frequency scan IC12 will select the input and the four outputs of IC16 in the sequence shown in TABLE 2 as the three-bit input

SELECTION INPUTS			DATA INPUTS								OUTPUT Pin 9
15	1	2	0 Pin 3	1 Pin 4	2 Pin 5	3 Pin 6	4 Pin 11	5 Pin 12	6 Pin 13	7 Pin 14	
1	1	1	X	X	X	X	X	X	X	✓	fin
0	1	1	X	X	X	X	X	X	✓	X	fin ÷ 2
1	0	1	X	X	X	X	X	✓	X	X	fin ÷ 4
0	0	1	X	X	X	X	✓	X	X	X	fin ÷ 8
1	1	0	X	X	X	✓	X	X	X	X	fin ÷ 16
0	1	0	X	X	✓	X	X	X	X	X	fin ÷ 4
1	0	0	X	✓	X	X	X	X	X	X	fin ÷ 2
0	0	0	✓	X	X	X	X	X	X	X	fin ÷ 1
B19/S8	C19/S9	D19/S10	fin	fin/2	fin/4	fin/16	fin/8	fin/4	fin/2	fin	
From IC3			Inputs from IC16								

✓ = active input.



Effective circuit.

TABLE 2. TRUTH TABLE for IC12, an 8211, operating as a single pole, 8-position switch selecting the divisor of the octave divider.

cycles through its sequence. For the first octave it selects the input (the actual transmitted frequency) and the two programmable dividers each step through their 128 divisors until the next octave is reached. The three-bit input number then changes from 111 to 011 as shown in Table 2 and IC12 selects the ÷2 output of IC16. The two programmable dividers each take 2.7306 seconds to step through their 128 divisors, the eight-channel switch, IC12, changing at this interval.

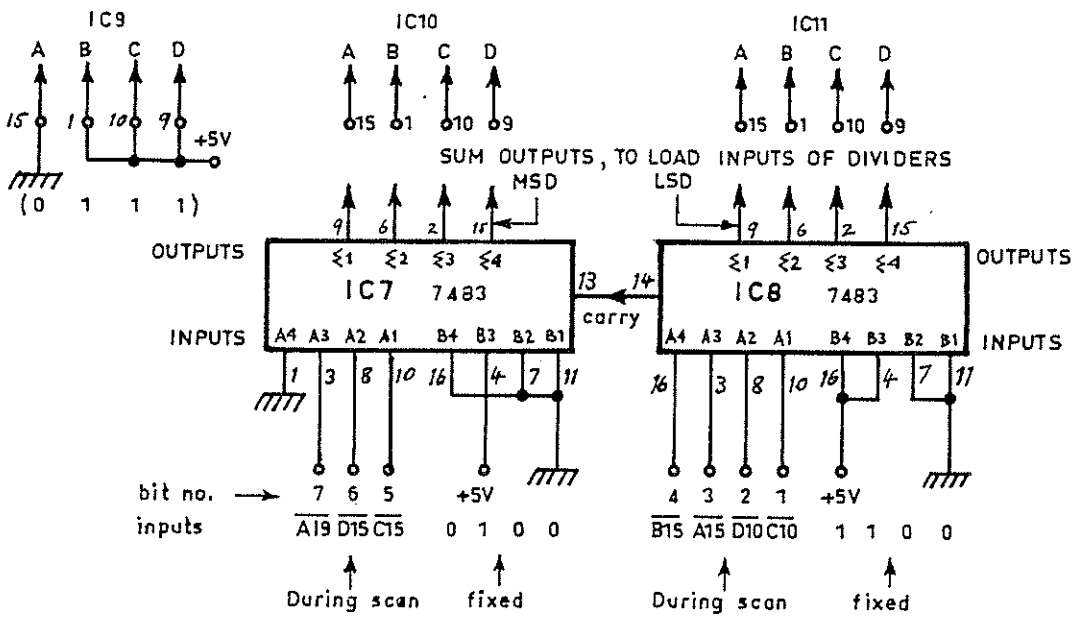
The sounding is terminated when the synthesizer if half-way through the final octave as frequencies above 23 MHz are not required for vertical-incidence ionograms. However, the synthesizer continues to step through the final octave. Upon reaching the end, the eight channel switch, IC12, selects the outputs of IC16 in decreasing order, as shown in Table 2, so that the VFO is stepped in the reverse direction and returned to a frequency near 69 MHz in readiness for the next scan.

The output from IC12, pin 9, goes to the 'count-up' input of the first IC in Programmable Divider A, pin 5 of IC11.

3.2.5 Programmable Divider A

Programmable Divider A consists of IC9, IC10 and IC11. Each is a type 74193 up/down binary counter which is capable of being preset to any number from 0 through 15, that is, a range of sixteen divisors. As there are three connected in a chain, the overall maximum division ratio is 4096. Each is arranged to count up, the count-up input of IC10 being driven by the 'carry' output of IC11. Similarly, the count-up input of IC9 is driven by the carry output of IC10. The 'load' inputs of each are parallelled and connected to the carry output of IC9. Thus, the whole divider chain is reset once it has reached a count of 4096.

The preset inputs of IC10 and IC11 are driven by the sum outputs of the two four-bit adders, IC7 and IC8, connected as an eight-bit full adder. The first seven bits of the 10-bit control number go to the 'A' inputs of IC7 and IC8. The A4 input of IC7 is wired to logical 0. The 'B' inputs of IC7 and IC8 are connected so that the binary equivalent of the number 76 is added to whatever binary number is presented at the A inputs. Figure 3.2.2 illustrates the operation of IC7 and IC8 in presetting Programmable Divider A.



Decimal weight of each bit →	1	2	4	8	16	32	64	128	256	512	1024	2048	Decimal equivalent	Comments
	IC8				IC7									
	1	2	3	4	1	2	3	4						
A INPUTS	1	1	1	1	1	1	1	0					127	First channel in octave
B INPUTS	0	0	1	1	0	0	1	0					76	Fixed
SUM OUTPUTS	1	1	0	1	0	0	1	1					203	
	IC11				IC10				IC9					
	A	B	C	D	A	B	C	D	A	B	C	D		
LOAD INPUTS	1	1	0	1	0	0	1	1	0	1	1	1	3787	First channel preset input Divisor = 4096 - 3787 = 309
	IC8				IC7									
	1	2	3	4	1	2	3	4						
A INPUTS	0	0	0	0	0	0	0	0					0	Last channel in octave
B INPUTS	0	0	1	1	0	0	1	0					76	Fixed
SUM OUTPUTS	0	0	1	1	0	0	1	0					76	
	IC11				IC10				IC9					
	A	B	C	D	A	B	C	D	A	B	C	D		
LOAD INPUTS	0	0	1	1	0	0	1	0	0	1	1	1	3660	Last channel preset input. Divisor = 4096 - 3660 = 436

FIG. 3.2.2 Illustrating the operation of the 4-bit adders IC7, IC8 in presetting Programmable Divider A, and how the divisors are obtained.

For the first channel in each octave, the first seven bits of the 10-bit control number will be high. This represents the binary equivalent to 127 at the A inputs of IC7/IC8. The number at the B inputs, 76, is added to this and the binary equivalent of 203 is preset at the sum outputs of IC7/IC8. Thus, the first two counters in Programmable Divider A are preset to 203. The preset inputs of IC9, the last divider in the chain are connected so that the divider chain is, in effect, permanently preset to 3584. Thus, the divider is preset to 3787 for the first channel in each octave.

When the first seven bits of the 10-bit control number reach the end of their cycle, they will all be low, the binary equivalent of zero will be present at the A inputs of IC7/IC8 and thus 76 will appear at the sum outputs. The divider is thus preset to 3660 for the last channel in an octave.

As the seven bits of the binary control number cycle through their sequence, the preset input number, and thus the divisor, of Programmable Divider A is incremented by one each time the least significant digit changes. There are 128 steps between 127 and 0 for the seven bits of the control number and thus 128 channels per octave.

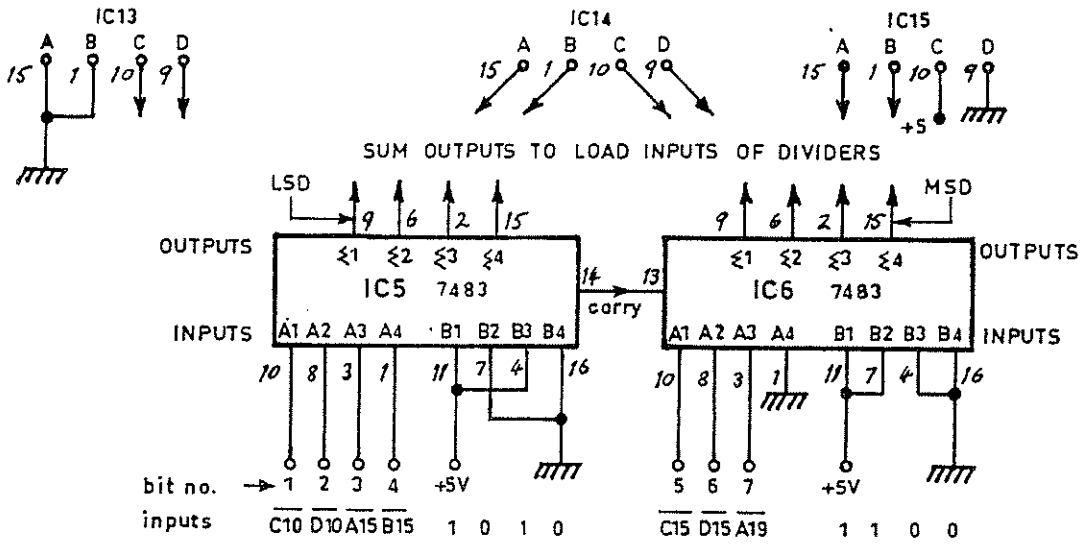
3.2.6 Programmable Divider B

Programmable Divider B consits of IC13, IC14 and IC15. As for Programmable Divider A, each is a type 74193 up/down binary counter which can be preset to any number from 0 through 15. The three ICs are connected in a chain as a down counter, the borrow output of IC13 drives the count down input of IC14. IC15 is driven by IC14 in the same way. This divider chain commences at the number presented to the preset inputs and counts down to zero, as explained previously.

The appropriate preset inputs of IC13, IC14 and IC15 are driven by the sum outputs of IC5/IC6, which are four-bit adders connected as an eight-bit full adder. The seven-bit control number driving the A inputs of IC7/IC8 also drives the A inputs of IC5/IC6. The B inputs of IC5/IC6 are connected so that the binary equivalent of 53 is added to whatever binary number is presented at the A inputs. The operation of IC5/IC6 is illustrated in figure 3.2.3 showing how Programmable Divider B is preset and how the divisors are obtained.

As mentioned previously, for the first channel in each octave, the first seven bits of the 10-bit control number will be high. This is the binary equivalent to 127, and 53 is added to this by IC5/IC6. Thus the binary equivalent to 180 appears at the sum outputs of IC5/IC6.

Now, the eight bits of the sum outputs of IC5/IC6 do not drive the first eight preset inputs of Programmable Divider B. Instead the A and B preset inputs of IC13 are grounded (logical 0) and the sum outputs of IC5/IC6 then drive the succeeding eight preset inputs of the divider chain. The least significant digit (LSD) of the sum outputs drives the C preset input of IC14, which has a decimal weight of four. The other sum outputs drive the succeeding preset inputs of the rest of the dividers. This effectively multiplies by four the number presented to the preset inputs. Thus, for the first channel in an octave, 180 at the sum outputs of IC5/IC6 appears as 720 to the preset inputs of Programmable Divider B. The final two preset inputs, pins 9 and 14 of IC15, are connected so that the divider chain is always preset to 1024. Thus, for the first channel of each octave, the divisor is 1744. (i.e. 720 + 1024).



Decimal weight of each bit.	1	2	4	8		16	32	64	128	Decimal equivalent	Comments
	IC5					IC6					
	1	2	3	4		1	2	3	4		
A INPUTS	1	1	1	1		1	1	1	0	127	First channel in octave
B INPUTS	1	0	1	0		1	1	0	0	53	Fixed
SUM OUTPUTS	0	0	1	0		1	1	0	1	180	

	IC13				IC14			IC15						
	A	B	C	D	A	B		C	D	A	B	C	D	
LOAD INPUTS	0	0	0	0	1	0		1	1	0	1	1	0	1744

First divisor { Load inputs A&B of IC13 and C&D of IC15 are fixed.

	IC5					IC6					
	1	2	3	4		1	2	3	4		
A INPUTS	0	0	0	0		0	0	0	0	0	Last channel in octave.
B INPUTS	1	0	1	0		1	1	0	0	53	Fixed
SUM OUTPUTS	1	0	1	0		1	1	0	0	53	

	IC13				IC14			IC15						
	A	B	C	D	A	B		C	D	A	B	C	D	
LOAD INPUTS	0	0	1	0	1	0		1	1	0	0	1	0	1236

Last divisor.

Decimal weight of load bits.	1	2	4	8	16	32	64	128	256	512	1024	2048

FIG. 3.2.3. Illustrating the operation of the 4-bit adders IC5, IC6 in presetting Programmable Divider B, and how the divisors are obtained.

When the seven-bit control number reaches the end of its cycle all the A inputs of IC5/IC6 go low and thus 53 is present at the sum outputs. This appears as 212 to the preset inputs of the divider and thus the last divisor in an octave is 1236.

The least significant digit (LSD) of the sum outputs of IC5/IC6 increments the divisor by four each time the LSD increments because the LSD sum output drives the C preset input of IC13, which has a decimal weight of four as mentioned previously.

3.2.7 The Digital Comparator

This portion of the circuitry involves IC's 17 to 24 inclusive and has three main functions. It provides steering pulses to the VFO circuitry according to the relationship between the outputs of the two programmable dividers. It also provides a load pulse to the programmable Divider B and gates the reference frequency input to this divider, as explained previously in section 3.2.2.

The VFO steering circuitry (see section 3.2.9) has two inputs. One is the GO DOWN input which moves the VFO such that the transmitted frequency is reduced when pulses are received at this input. The other is the GO UP input which moves the VFO in the opposite direction such that the transmitted frequency is increased when pulses are received at this input.

A block diagram of the Digital Comparator is shown in figure 3.2.4.

The CARRY pulses from Programmable Divider A are halved by a binary counter (BC), the output of which (BCO) drives two monostables, M1 and

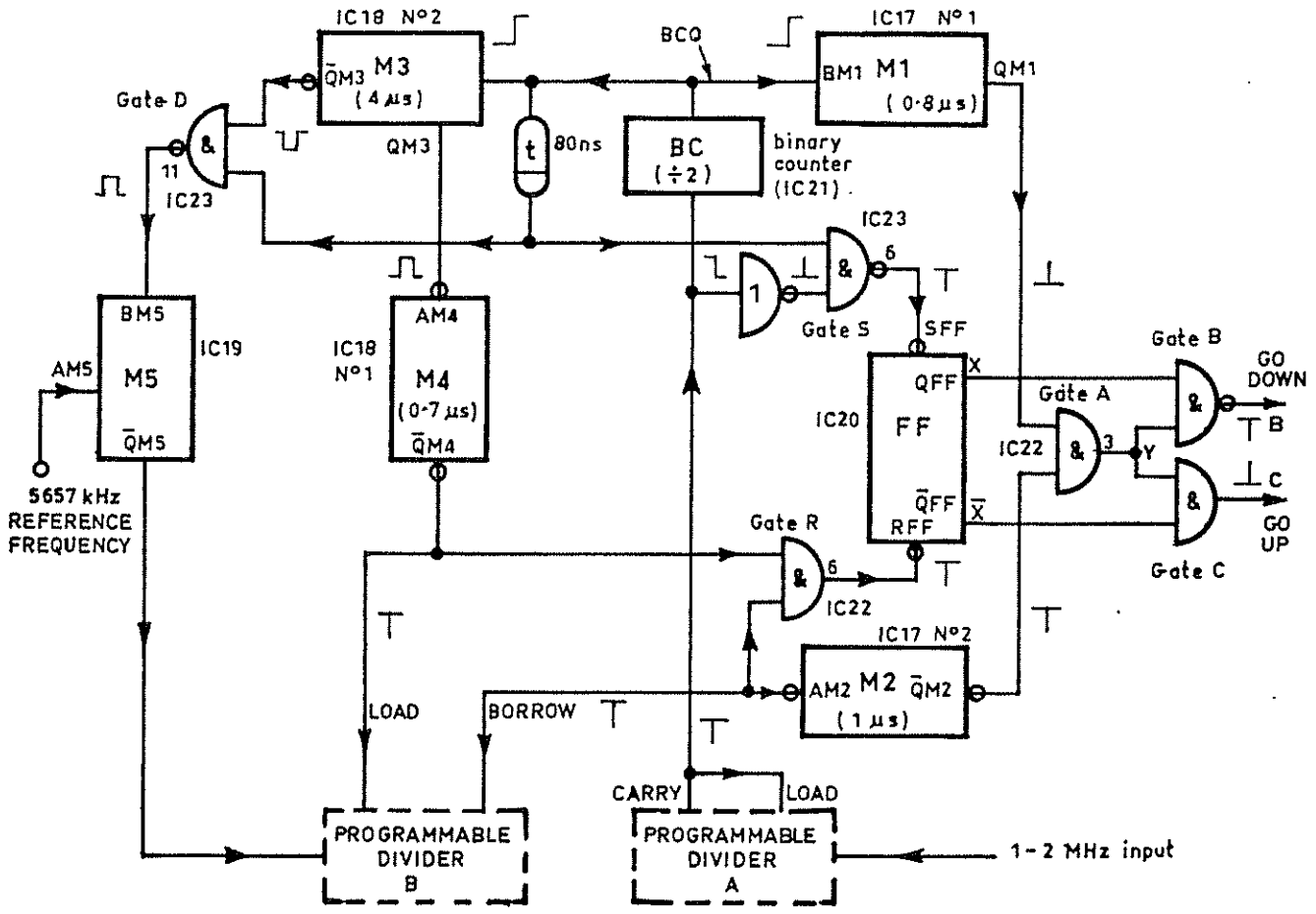


FIG. 3.2.4. Block Diagram of the Digital Comparator.

M3. A pulse, 0.8 us wide, is generated by M1 when BCO goes high. A 4 us wide pulse is generated by M3 when BCO goes high. The pulses from BCO are delayed about 80 us (using four inverters in cascade) and gated with the CARRY pulses in Gate S. For the CARRY pulse that causes BCO to change from high to low, a set pulse for FF is provided at the output of Gate S. The delay is introduced so that the negative -going edge of the delayed BCO pulse is later than the CARRY pulse which causes BCO to change state, allowing the two inputs of Gate S to be high each alternate CARRY pulse.

Thus, one CARRY pulse will trigger M1, resulting in a 0.8 us pulse at QM1. The next CARRY pulse will set FF, causing X to go high, $\overline{X}$ low.

The delayed BCO pulses are also gated with the 4 us pulse from $\overline{QM3}$ in Gate D. The output of this gate holds AM5 high for 4 us following the CARRY pulse which triggers M3. The input to Programmable Divider B is then gated off. A load pulse, 0.7us wide, is generated by M4 at the end of this 4us period so that Programmable Divider B will commence counting afresh when M5 is gated on again.

The pulses from $\overline{QM4}$ and the BORROW pulses from Programmable Divider B go to the two inputs of Gate R. When a BORROW or a LOAD pulse occurs, the output of Gate R delivers a reset pulse to FF and X goes low, $\overline{X}$ high.

Each BORROW pulse also triggers the monostable M2 which delivers a lus wide, negative-going pulse at $\overline{QM2}$.

The output of M1 (QM1) is gated with the output of M2 ($\overline{QM2}$) in the AND-gate, Gate A.

If the BORROW and CARRY pulses are not coincident, M1 and M2 will be triggered at different times and the pulses from QM1 and $\overline{QM2}$ will not coincide. For this condition, the positive-going 0.8us pulse from QM1 will appear at Y. If X is high at this time, the pulse from QM1 will be gated through to the GO DOWN output by Gate B, appearing as a negative -going pulse on terminal B. If $\overline{X}$ is high at this time, the 0.8us pulse at Y will be gated through to the GO UP output by Gate C, appearing as a positive-going pulse on terminal C. If the BORROW and CARRY pulses are not quite coincident, but overlap, then the pulse at Y will be narrowed (from 0.8us) by the amount that the lus pulse from $\overline{QM2}$ overlaps the pulse from QM1. Thus, the pulses gated to the steering outputs (B and C) will be narrowed as the BORROW and CARRY pulses approach coincidence. This slows the rate at which the VFO changes frequency. When they coincide, the pulse from $\overline{QM2}$ will completely overlap the pulse from QM1 and there will be no pulses gated through to the steering outputs.

If the Synthesizer output is higher than the required frequency, CARRY pulses will occur before the BORROW pulses. At the first CARRY pulse, BCO will go high triggering M1 and M3. If X is high at this time (assuming it has been previously set) a 0.8us pulse will appear at the GO DOWN output.

When $\overline{QM3}$ goes high at the end of the 4us period, BM5 will be driven low as the other input to Gate D will be high because BCO is high. Thus M5 will gate off the input to Programmable Divider B. It receives a LOAD pulse at the end of the 4us which ensures that it will commence counting afresh when the input is again gated on. The LOAD pulse resets FF (via Gate R) and X goes low, $\overline{X}$ high.

When the next CARRY pulse occurs BCO goes low and FF recieves a set pulse, X goes high and $\overline{X}$ low. The input to Programmable Divider B is gated on again following this CARRY pulse as the delayed BCO output on the input to Gate D will be low until the next succeeding CARRY pulse. Thus BM5 will be high for this period, and the output from M5 will be gated on. Both programmable dividers thus commence counting together.

The next CARRY pulse to occur will again drive BCO high, triggering M1 and M3, resulting in a pulse at the GO DOWN output and the whole sequence is repeated until the BORROW and CARRY pulses are almost coincident. When this occurs, the pulses at the GO DOWN output will be narrowed as described before, the steering pulses disappearing when the BORROW and CARRY pulses coincide. The synthesizer output will then be on the desired frequency.

If the Synthesizer output is lower than the desired frequency, the BORROW pulses will occur before the CARRY pulses. At the first BORROW pulse, FF will be reset and $\overline{X}$ will go high. The first CARRY pulse will cause BCO to go high, triggering M1 and M3. The 0.8us pulse from QM1 will be gated through to the GO UP output by Gate C, as X is high. Programmable Divider B receives a LOAD pulse and its input is gated off 4us after the CARRY pulse.

When the next CARRY pulse occurs, FF receives a set pulse, X going high, $\overline{X}$ low. BCO goes low causing BM5 to go high, M5 gating through the input to Programmable Divider B and the process is repeated until the BORROW and CARRY pulses coincide, no pulses appear at the steering output and the Synthesizer output is on the desired frequency.

3.2.8 THE RF SECTION A4A2
(Dwg: CD-232X2)

This section is largely constructed on three printed circuit boards located in separate shielded compartments on the opposite side of the chassis to the Digital Section. The Reference Oscillator, Digital Interface, Pulse Modulator and VFO steering circuits are located on the largest board in the upper section of the chassis. The 70 MHz oscillator and Mixer is located on a small printed circuit board in a separate, fully-shielded compartment situated in the lower section of the chassis, towards the front panel. The VFO and buffer are located on a small board at the rear of the chassis, adjacent to the Receiver output socket. The amplifier following this is located between the VFO and the 70 MHz osc. and mixer shielded compartment. Two shields across the chassis isolate the input and output circuitry of each stage of the amplifier which is constructed using standoffs and feed-through capacitors to support the components.

3.2.9 The VFO and Steering Circuitry

The VFO employs an MC1648L IC which contains an oscillator having a high spectral purity output. This reduces spurious responses in the receiver as the VFO output is the local oscillator signal for the first mixer in the receiver.

An external tuned circuit determines the frequency, the tuned circuit being comprised of L4 and D1, a variable capactance diode.

The capacitance, and thus the VFO frequency, is varied by varying the DC voltage across the diode. This is effected by the steering circuit. When the potential between anode and cathode of D1 is increased, the capacitance decreases, increasing the VFO frequency. The capacitance of D1 increases when the potential across it decreases, decreasing the VFO frequency. L4 is a slug-tuned coil. It is set during the initial aligment of the ionosonde and should not require further adjustment.

Capacitors C12 and C13 are DC blocking capacitors isolating the DC control voltage on D1 from the terminals of IC1. Resistors R10 and R11 provide RF decoupling from the tuned circuit for the DC control to D1 while providing a DC connection to it.

An emitter-follower buffer, TR4, isolates the output terminal of IC1 from the external circuitry to preserve the spectral purity of the VFO signal. The VFO output to the Receiver is taken from the emitter of TR4 via R15 and a BNC socket mounted on the lower section of the back panel of the chassis. This is accessible through the card-file sockets at the rear of the top rack assembly.

Capacitors C14, 17, 18 and 19 are RF bypass components. L5 decouples the + 10V supply line. Resistors R15 and R17 drop the ten volt supply to five volts, required by IC1.

Steering of the VFO is accomplished by TR1 and TR2, the GO DOWN and GO UP pulses from the digital comparator turning each transistor on as neccessary, effecting a change in the VFO frequency in the following way:-

Assume the VFO has been set to a particular frequency. Capacitors C8 and C11 are charged and D1 will be reverse biased, the potential between anode and cathode establishing the capacitance required to tune the VFO to the channel.

When the Digital Section is set to move the Synthesizer to a higher channel, the digital comparator will present a series of pulses to the GO UP input, terminal C. These pulses are applied to the base of TR2 (via R2/C2) turning it on for the duration of each pulse. Each pulse of collector current conducts some of the charge from C8 via R6, R7 and the -10V supply as this is the lowest impedance discharge path, The series of pulses causing a reduction in the potential across C8 in a series of small steps. The VFO frequency then decreases in a series of small steps. This results in an increase in the transmitted (or operating) frequency, as the VFO is heterodyned with 70 MHz, the difference providing the operating frequency.

As the VFO approaches the required frequency the GO UP pulses become narrower, slowing the rate of change in the VFO frequency. When the Synthesizer is on the required frequency, no steering pulses are received.

When the Synthesizer is to be moved to a lower frequency channel, the GO DOWN pulses cause TR1 to conduct and C8 charges via R5 and C11 as this is the lowest impedance charging path. The voltage across C8 is reduced in a series of small steps in a similar manner to that explained above, resulting in an increase in the VFO frequency, reducing the operating frequency. As the VFO approaches the required frequency the GO DOWN pulses become narrower slowing the rate of change in the VFO frequency in the same manner as before. There is a small amount of

frequency 'jitter', but this is unimportant as it is less than the bandwidth of the receiver. If the VFO drifts, the digital comparator will correct it in a similar manner.

A two-stage amplifier follows the VFO buffer output. Its purpose is to increase the level of the VFO signal to the Mixer and to provide isolation between the VFO output to the Receiver and the various products generated by the mixer, as well as the 70 MHz oscillator.

The amplifier involves TR5 and TR7, two type 40673 dual-gate FETs, and employs R-C coupling. It has only a small amount of gain. The two 10V supply rails are decoupled by L6, 7,8,9 and 11 and a number of feedthrough capacitors which also serve as tie points. The components are readily identified from drawing CD-232Y3. Gate two of each FET is biased to about 6.5-7V with respect to chassis.

3.2.10 70 MHz Oscillator and Mixer

The 70 MHz oscillator is an overtone crystal oscillator involving TR6, a BF200, and XL2 which operates on the fifth overtone. Feedback is controlled principally by C23 and C24. L10 resonates at 70 MHz with the combined capacities of C22, C23 and C24, and circuit strays. It is slug-tuned and is set during the initial alignment of the ionosonde and should not require further adjustment unless components are replaced due to a malfunction of this circuit. Adjustment of the slug alters both the output and the frequency and for this reason should not be touched.

Output from the oscillator is via C26 which goes to gate 1 of TR8, the mixer.

The collector supply of TR6 is decoupled by R29, bias being provided by R27 and R30 from the -10V supply rail.

The Mixer, TR8, involves a dual-gate FET type 40673. The amplified output from the VFO is applied to gate 1. Output, in the 1 to 23 MHz range, is taken from the drain to the digital interface and pulse modulator circuits via a four-section low-pass filter consisting of L13, 14,15,16 and C27,28,29,31 and C33. The drain voltage for TR8 is supplied from the +10V rail via a 1.5mH RF choke, L12. All the inductors in the filter are encapsulated microchokes. L13, 14 and C27,28 are mounted on the 70MHz oscillator and mixer printed circuit board. The rest of the filter components are mounted on the large P.C. board in the top section of the synthesizer chassis adjacent to TR10 in the digital interface circuit (see Dwg: CD-232Y3).

3.2.11 The Digital Interface Circuit

This consists of a two-stage amplifier involving TR10 which is a wideband, common-emitter amplifier and TR13/TR14 connected as an emitter-coupled amplifier, TR14 being driven between saturation and cutoff. It is located on the large printed circuit board, towards the end nearest the front panel. (see Dwg: CD-232Y3).

The 1 to 23 MHz output from the filter is coupled to the base of TR10 via C34. Low value resistors, R47 and R44, in the collector and emitter of TR10 provide wide bandwidth, but the stage has only low gain. The emitter resistor R44 is unbypassed providing some AC negative feedback to improve the bandwidth. Output from the collector of TR10 via C37 and R47 is coupled to the base of TR13. Bias for TR10 is provided

by R41 and R45 from the - 10V supply. The collector supply for TR10 is via R42 from the + 10V rail. Capacitors C35 and C36 are bypass components.

During the positive half-cycles of the RF signal from TR10 the base of TR13 is forward biased. This causes the emitter potential of TR13, and thus TR14, to rise towards the + 5V supply, cutting off TR14. During negative half-cycles of the RF from TR10 the base of TR13 is reverse biased. TR14 will conduct as the base-emitter junction is forward biased from the - 10V supply by R54.

As the collector supply for TR13/TR14 is from the + 5V rail, the output is square wave, the low and high levels being compatible with the following TTL circuitry in the Digital section.

3.2.12 The Pulse Modulator

This consists of a wideband amplifier stage, a diode switch and a switch driver. The amplifier stage involves TR9; the 1 - 23 MHz output from the filter is coupled to the base which is connected in parallel with the base of TR10. The emitter resistor, R37, is unbypassed providing some AC negative feedback to improve the bandwidth. The primary of T1 is in the collector of TR9 so that the 1 - 23 MHz RF is coupled to the diode switch. Bias for TR9 is obtained from the - 10V rail via R38, the base current being returned to ground via R41, which is also the base bias return for TR10. R36 ensures a constant, low impedance load on the primary of T1 so that the amplifier has constant gain across the frequency range.

The diode switch involves two wideband transformers, T1 and T2, and four, silicon, high-speed switching diodes, D2 to D5. These are biased hard on and hard off appropriately by the switch driver, involving TR11 and TR12.

The positive-going 40us Tx pulse forward biases TR12 which conducts. This forward biases TR11 which also conducts. Part of the collector current of TR11 will flow via R39, forward biasing D2 and D5, which conduct, the current return passing via the grounded secondary centre-tap of T1. D3 and D4 will be reverse biased by this. The secondary of T1 is thus connected to the primary of T2, via D2 and D5, and the RF output of the Synthesizer is coupled to the Transmitter, via the secondary of T2, for the duration of the 40us Tx pulse.

During the period between Tx pulses, TR12 is unbiased and no collector current flows, hence TR11 is cut off. D3 and D4 will then conduct as they will be forward-biased, via R39 and R40 from the - 10V supply, and via the grounded secondary centre-tap of T1. Thus, the secondary of T1 is virtually short-circuited by D3 and D4, and, as D2/D5 are also now reverse biased, the RF is cut off and there is no output.

The two wideband transformers, T1 and T2, are wound on dual-hole ferrite 'balun' transformer cores so that the windings are almost totally enclosed, providing effective shielding.

The pulse modulator circuitry is located on the large printed circuit board, TR9 being near the centre line of the board, the rest of the circuitry being located towards the rear end of the Synthesizer chassis. T1 and T2 should be easily located (see Dwg: CD-232Y3).

3.2.13 The Reference Oscillator

This is a crystal controlled Colpitts oscillator, involving XL1 and TR3, operating on 5657kHz. It is located on the large printed circuit board, toward the end nearest the front panel. Feedback is controlled by capacitors C15/C16 and output is taken from the collector of TR3 to pin D on the end of the board. (see Dwg: CD-232Y3). The collector supply is derived from the + 5V rail so that the output levels are compatible with the TTL circuitry it drives in the Digital section. A lead passes from pin D on the board in the RF section, through the chassis,to pin D on the Digital section p.c. board (see Dwg: CD-232Y3).

3.3
TRANSMITTER

Par. No.	Title	Drawing No.
3.3.1	Brief Summary	CB-27Y1
3.3.2	The Power Supply	CD-255Y1 (A6A1)
3.3.3	The Pulser	" " "
3.3.4	The Driver	CD-254Y1 (A6A2)
3.3.5	The Power Amplifier (P.A.)	CD-256Y1 (A6A3)
3.3.6	The Transmitter Fail Detector	CD-256Y1 (A6A4)

3.3.1 Brief Summary

There are five sections in the transmitter assembly, A6. A block diagram is given in drawing CB-27Y1. The five sections and their functions are as follows:

(a) The POWER SUPPLY (part of A6A1). This provides high tension, bias and EHT voltages derived from 24 V DC via an inverter.

(b) The PULSER (part of A6A1). This provides 500 V, 40 μs pulses for the P.A. tube screen grids from the transmit pulse produced by the OPERATIONAL CLOCK (on A3A11).

(c) The DRIVER (A6A2). This amplifies the low level, pulsed RF output of the FREQUENCY SYNTHESIZER to drive the Power Amplifier.

(d) The POWER AMPLIFIER (P.A.) (A6A3). This amplifies the output from the Driver to about 5kW peak pulse output using four vacuum tubes.

(e) The TRANSMITTER FAIL DETECTOR (A6A4). This indicates if the transmitter is not producing RF output during a sounding and gates on a warning light on the front panel of the PROGRAM unit, A5, which flashes once every two seconds.

The P.A. output is designed to match 50 ohm coaxial cable, used for the antenna transmission line, and a standard SO-239 connector is mounted on the back panel of the transmitter chassis. The Pulser and Power supply are located on the one printed circuit board, A6A1. This assembly, the Driver (A6A2) and the P.A. (A6A3) are all located in separate shielded compartments in the transmitter chassis.

The Transmitter Fail Detector (A6A4) is on a small printed circuit board located in the P.A. shielded compartment.

The transmit pulses, from the Operational Clock (A3A11), simultaneously pulse the Frequency Synthesizer RF output, the Transmitter Driver and the P.A. screens via the Pulser (A6A1).

3.3.2 The Power Supply (A6A1) (Dwg CD-255Y1)

This is a push-pull, driven switching inverter. It consists of two transformer coupled stages, driver and power output, and three rectifier circuits providing +1.5kV EHT, +250 V. HT and -100 V. bias.

The driver stage, TR1 and TR2, is driven by a 6kHz square wave derived from the PRIMARY DIVIDERS of the CLOCK (on A3A5). This is converted to complementary-phase pulses for the push-pull input by circuitry in the CONTROL LOGIC (A3A8) which also gates the 6kHz drive on and off at the beginning and end of each sounding. Alternate cycles of the 6kHz input drive TR1 and TR2 alternately into saturation or cutoff. Transformer T1 then drives the bases of the power output transistors TR4 and TR5.

The power output transistors are alternately saturated or cutoff, the collector-to-collector voltage swing being nominally 48 V. The full secondary of T3 provides about 250 V. output. A voltage multiplier rectifier, consisting of three voltage doublers with their outputs in series, produces +1.5kV EHT for the P.A. tube anodes. When the P.A. screens are pulsed, a high current DC anode pulse is provided by the energy stored in capacitors C13, C11 and C7.

High tension of +250 V. for the output stage of the Driver (A6A2) is provided by a half-wave rectifier (D4, R23, R25, C14) from the full secondary of T3.

Bias for the P.A. tube grids is derived from a tap on the secondary of T3. A half-wave rectifier (D2, R19, R24, C8) provides about -100 V.

A pi-network filter consisting of C1, L1 and C2 prevents pulse transients and 6kHz hash from being superimposed on the power supply line.

The Power Supply is located on a printed circuit mounted in the front compartment of the Transmitter chassis.

3.3.3. The Pulser
(Dwg. CD-255Y1)

This is located on the same printed circuit board as the transmitter Power Supply.

The transmit pulse sequence is only applied during a sounding, being gated on and off by the Control Logic, A3A8. Each 40 μs transmit pulse forward biases the base of TR3, which conducts. The negative-going pulse at the collector is capacitively coupled to the base of TR6 which saturates, providing a 40 μs high current pulse in the primary of T2.

The pulser transistor, TR7, is normally off and C9 charges to about +500 V. via R21. TR7 acts as a high voltage, high current switch. When the 40 μs pulse appears at the primary of T2, the secondary provides a high current pulse to the base of TR7 which saturates. The energy stored in C9 then provides a 500 V. high current pulse to the screens of the P.A. tubes.

The diode, D1, and the resistor, R15, absorb the back e.m.f. generated in the primary of T2, reducing any ringing and preventing reverse voltage breakdown of TR6. Decoupling from the 24 V. supply is effected by R16 and C5.

3.3.4 The Driver (A6A2)
(Dwg. CD-254Y1)

This is a five stage, direct-coupled, wideband amplifier. It has a single-ended input stage to accept the low-level, unbalanced, low impedance output of the Frequency Synthesizer and a push-pull power output stage to drive the grids of the P.A. tubes.

The bias, and thus the operating point, for each stage is set by the quiescent collector current of the preceding stage. The DC return for the emitters of the input stage, TR2-TR3, is via the collector of TR1, which functions as a switch. When TR1 is not conducting, TR2 and TR3 cannot conduct and the whole amplifier is effectively turned off. The 40 μs transmit pulses from the Operational Clock (on A3A11), via the Control Logic (A3A8), forward bias the base of TR1 which conducts, causing TR2 and TR3 to conduct. As all five stages are direct-coupled, the switching action of TR1 pulses the complete amplifier.

The input stage transistors, TR2-TR3, are connected in the 'long-tailed pair) configuration, having a single ended input to TR3 and a push-pull output from the collectors. TR3 operates as a common-emitter amplifier and TR2 as a common-base amplifier. The emitter of TR3 is coupled to the emitter of TR2 via C5 and R12. The succeeding stages of the amplified all operate in push-pull.

The second stage, consisting of two PNP transistors, TR4 and TR5, drives the fourth stage via emitter followers TR6 and TR7, the third stage.

The output stage employs a grounded-base push-pull amplifier with five transistors in parallel in each side. The collectors of the fourth stage, TR8-TR9, drive the emitters of the output stage transistors. R23 in parallel with C12, coupling the emitters of TR8 and TR9, increases the gain and improves the frequency response.

The collectors of the five transistors in each side of the output stage are paralleled with a brass strip to provide a low inductance connection. The bases of the ten output transistors are all paralleled and grounded for RF via a series of 0.001 µF capacitors. The Driver output stage uses high voltage power transistors and a collector H.T. of 250. V. to provide a drive voltage swing of about 150. V. peak to the P.A. tube grids.

The earth return for the first two stages is separated from the earth return for the third, fourth and fifth stages. This is to avoid common-earth RF feedback problems as high RF current pulses flow into the earth return path for the output stage and cause instability if coupled into the input stages. The earth connection to chassis for the first two stages is via the braid of the input coax, while the earth connection for the output stages is to the common-point earth for the P.A. tube cathodes, via a heavy braid. If either is lifted, the amplifier is disabled as they also serve as DC-returns.

The +24. V. supply to the two sections is also separated, each line being separately decoupled, the input section by R16, C7, C8, and C9, the output section by R38, C14, C15 and C16.

3.3.5 The Power Amplifier (P.A.) (A6A3) (Dwg. CD-256Y1)

This is a push-pull, pulsed power amplifier employing two tubes in parallel per side. A wideband output transformer, T1, matches the anode-to-anode impedance of the output tubes to 50 ohms for the antenna transmission line.

The P.A. operates in class C. The tube control grids are biassed somewhat beyond anode cutoff, and some grid current flows at the peak of the RF pulse from the driver. The grid input impedance is swamped by resistors R1, R3, R7 and R9 to achieve wide bandwidth. The P.A. tube screens receive a 500. V., 40µs pulse from the pulser located on A6A1. The anodes conduct during the screen pulse as grid drive is simultaneously present, producing a high power RF pulse output.

Parasitic suppression is effected by passing each anode lead of the parallel tube pairs through the two holes of a small ferrite balun core, before making the parallel connection, inductively loading the anode leads. Screen grid parasitics are suppressed by series resistors (R5, R6, R11 and R12).

The peak pulse power output developed by the P.A. is about 5kW up to about 8 MHz. It decreases to about 2kW at 12MHz, falling to about 500. W. above 16 MHz.

3.3.6 The Transmitter Fail Detector (A6A4) (Dwg. CD-256Y1)

A peak detector, consisting of D1 and D2, rectifies the RF from a single-turn winding on T1, charging a large value capacitor, C15. The voltage on C15 forward biases TR1, the collector conducts and 'pulls down' one input of a NAND gate in the 'Tx Fail Warning Logic' in the Control Logic A3A8. (See section 3.7 for the circuit operation.)

If no RF appears at the output of the transmitter, TR1 will not conduct. This 'enables' the Tx Fail Warning Logic, gating through pulses from A3A5 to the TX FAIL warning light, on the front panel of the PROGRAM unit (A5), which flashes once every two seconds.

3.3.7 Transmitter Pulse Delay Circuit

The circuit is comprised of C2, R3, R6, R7, D1 and TR1, and is incorporated to ensure that the E.H.T. is applied to the anodes of the output valves before the screen voltage pulse and R.F. drive.

A manual switch, S1, is located on the Harness, A13 A1, and may be used to prevent the Tx pulse from being applied to the transmitter unit. In this case, the delay circuit would, of course, be inoperative.

The delay circuit is capacitively coupled through C2 to the +24V main supply rail located on A6 PL1/pins 1 and 2. When power is applied, the negative side of C2 is at +24V and current flows into TR1 base through R6, turning it on and thereby short circuiting the Tx pulse input (A6PL1/pin 15) to ground. (D1 is reverse biased during the charging of C2). When C2 has charged sufficiently, through R6 and the base-emitter junction of TR1, TR1 turns off and allows the Tx pulse to feed the transmitter driver and the SCREEN PULSER sections. The delay time is approximately the charge time constant of R6, C2.

DELAY TIME = 100K x 10uF

OF Tx PULSE

= 1 second

When the power is turned off the 24 volt rail falls to zero and the negative side of C2 falls to -24V. C2 then rapidly discharges through R3 and D1,

3.4
RECEIVER

Par. No.	Title.	Drawing No.
3.4.1	Brief Description	CB-24Y1
3.4.2	The Front End	CD-253Y1 (A7A1)
		CD-253Y2 (A7A2)
3.4.3	The First IF and Second Mixer	CD-253Y3 (A7A3/4)
		CD-253Y4 (A7A5)
3.4.4	The Second IF and Third Mixer	CD-253Y5 (A7A6)
3.4.5	The Third IF and Detector	CD-253Y6 (A7A7)
3.4.6	The Video Output and AGC circuitry	CD-253Y7 (A7A8)

3.4.1 Brief Description

The receiver is a triple conversion design employing intermediate frequencies (IF's) of 70 MHz, 10.7 MHz and 1.6 MHz. The block diagram appears in drawing CB-24Y1.

Double-balanced diode mixers are used for the three mixers to reduce spurious responses and for their ability to cope with strong signals. The first mixer conversion frequency is derived from the FREQUENCY SYNTHESIZER, the second and third mixers have associated crystal oscillators on 59.3 MHz and 9.7 MHz respectively. Selectivity is provided by the third IF amplifier which employs L-C interstage filters to provide a bandwidth of 40 kHz. The first and second IF amplifiers are gain controlled by a sample-and-hold AGC circuit. The detector output is passed to the Signal Processor and Display via circuitry which interfaces the received pulses to TTL logic levels.

The receiver can be divided into five basic sections according to their functions, as follows:

(a) The FRONT END. This comprises the serial input filter (A7A1) and the first mixer (A7A2). The input signal is converted to the first IF of 70 MHz.

(b) The FIRST IF and SECOND MIXER. This is located on A7A5. Included in this section is the 70 MHz filter (A7A3/A7A4) interposed between the first mixer and first IF amplifier. The second mixer follows this stage providing a conversion from 70 MHz to 10.7 MHz.

(c) The SECOND IF and THIRD MIXER. Located on A7A6, this section of the receiver provides IF amplification at 10.7 MHz followed by conversion to 1.6 MHz by the third mixer.

(d) The THIRD IF and DETECTOR. This is located on A7A7 and is the section providing the bulk of the receiver selectivity. A full-wave detector drives the AGC and interface circuitry following.

(e) The VIDEO OUTPUT and AGC CIRCUITRY. This is located on A7A8. The output circuitry interfaces the receiver video output to TTL logic levels. The automatic gain control (AGC) circuitry samples the amplitude of noise and signals between echo pulses and varies the gain of the first and second IF amplifiers accordingly.

There are eight printed circuit boards in the receiver mounted in a half-rack chassis located in the cabinet next to the Ionosonde POWER SUPPLY, A12A1. The boards are mounted in separate, shielded compartments to reduce spurious responses and instability. The power supply interconnections to each board are decoupled via feedthrough capacitors, the interconnection wiring and other decoupling components being on the opposite side of the chassis to the circuit boards. The antenna input and Frequency Synthesizer input enter through BNC sockets mounted on the back of the Receiver chassis. A schematic of the board interconnections, signal inputs and outputs is given in drawing CD-259Y1.

The overall gain of the receiver is in the order of 80 to 90dB. The aerial filter and 70 MHz filter each have a loss of several dB. The three mixers each exhibit a loss of about 6dB. The first and second IF amplifiers have a gain of 20dB or more each while the third IF amplifier has a gain of over 70dB. The sum of the IF amplifier gains is about 110dB, while the losses total about 20dB resulting in an overall gain of about 90dB.

Positive and negative DC supplies of 10V are provided for the receiver circuitry. These are derived from the IC POWER SUPPLY REGULATORS (A12A2).

3.4.2 The Front End (A7A1 and A7A2)
(Dwgs: CD-253Y1 and CD-253Y2)

Signals received by the antenna are first passed through a bandpass filter consisting of a high-pass filter and a low-pass filter in cascade. The high-pass filter has a cutoff that may be set somewhere between 800 kHz and 1.6 MHz. This reduces cross modulation interference that could be introduced by strong local MF broadcast stations, by attenuating signals below the cutoff frequency. The lowpass cutoff is usually set to 1.6 MHz, although it may be set to another frequency, prior to installation of the Ionosonde, according to the local circumstances. The low-pass filter has a cutoff frequency of 23 MHz, just above the upper frequency channel of the synthesizer. This filter attenuates signals in the low VHF range that may crossmodulate wanted signals below 23 MHz and prevents 70 MHz "break-through" to the first IF.

The bandpass filter components are located on A7A1. This is a long, narrow board with the input and output at opposite ends and mounted in a shielded compartment to maintain high stop-band attenuation.

The bandpass filter output goes directly to the input of the first mixer. This is a double-balanced diode mixer employing four IN914 high speed switching diodes (D1 to D4). The conversion frequency is obtained from the VFO output of the Frequency Synthesizer. This is amplified in an LM733 wideband op-amp followed by a single transistor amplifier stage (TR1) to drive the mixer diodes. The output of TR1 drives the mixer via T1 which provides an impedance match and an unbalanced-to-balanced transformation. The incoming signal enters the mixer via the centre-tap of T2, the IF output appears on the secondary. Both T1 and T2 are wideband balun transformers.

The double-balanced mixer configuration suppresses the conversion frequency and the input frequency and their even harmonic, greatly reducing the level of spurious responses in the output. The output consists primarily of the sum and difference frequency components of the conversion and signal frequencies. The sum of the input frequencies is chosen as the IF, and thus, as the Frequency Synthesizer VCO output varies from 69 MHz to 47 MHz, signals between 1 MHz and 23 MHz, respectively, will be converted to 70 MHz the first IF.

L1 and L2 are RF chokes forming part of the supply decoupling circuitry. Capacitors C2, C4, C5, C8 and C9 and resistors R5 and R8 are all supply bypass and decoupling components.

3.4.3 The First IF and Second Mixer (A7A3/4 and A7A5)
(Dwg: CD-253Y3 and CD-253Y4)

A filter precedes the first IF input, following the first mixer output. Its purpose is to reject spurious responses caused by signals from the antenna mixing with spurious products from the Frequency Synthesizer in the first mixer.

The filter consists of two, short, capacitively tuned strip transmission lines, A7A3 and A7A4, resonating at 70 MHz. They are capacitively coupled between terminals at the high impedance end of each line. (Between Tml 2 of each line as shown on drawing CD-253Y3). A small capacitance is formed by a short length of insulated wire, soldered to one terminal and wrapped around the other terminal without a connection. The construction forms two capacitively loaded, top-coupled, quarter-wave transmission line resonators. This results in a high-Q bandpass filter with consequent narrow bandwidth, steep sides and high attenuation outside the bandpass.

A7A3 and A7A4 each consist of a narrow strip of printed circuit board with an etched conductor running almost its full length. One end is grounded via a brass mounting pillar. On the other end is mounted a 60pF trimmer for tuning the line. Each board is mounted in a trough running the full width of the receiver chassis which completes the configuration of an unbalanced transmission line.

Input and output coupling is via tapping points at the low impedance end of each line. (Shown as Tml 1 on drawing CD-253Y3).

A type 40673 dual-gate FET, TR1, is the first IF amplifier. The output of the 70 MHz filter goes to gate 1 of TR1. A tuned circuit in the drain of TR1, L2/C5, is mutually coupled to T1 the input transformer of the second mixer. Source bias for TR1 is derived from the negative supply line via R2. The AGC voltage is applied to gate 2. R1 decouples the AGC line, C1, C2 and C3 are for RF bypassing. The quiescent AGC voltage, with no signals present is somewhat over 4V for maximum gain and decreases with increasing signal amplitude.

The primary of T1 is tuned to 70 MHz. Both L2 and T1 are slug-tuned coils. A low impedance, centre-tapped secondary provides an impedance match to the input of the double-balanced mixer diodes D1 to D4. The IF output at 10.7 MHz is taken from the centre-tap of this winding.

A type BSV78 junction FET, TR2, is used in an overtone crystal oscillator on 59.3 MHz providing the conversion frequency for the second mixer. The crystal, XL1, is a third overtone type oscillating in the series resonant mode. The ratio of C8 to C9 determines the level of oscillator feedback.

The oscillator drives the four IN914 mixer diodes via a low impedance, centre-tapped secondary on T2. The primary is slug-tuned and resonates with the combined capacitance of C8, C9 and the drain-source capacitance of TR2. The gate of TR2 is grounded for RF by C13, R4 is the DC return to the negative supply. Source bias is provided by R3.

Both tuned transformers, T1 and T2, provide an impedance match and an unbalanced-to-balanced transformation to the double-balanced mixer.

RF chokes L1, L3, L4, L5, L6, L7 and capacitors C4, C6, C11 and C12 provide decoupling and bypassing for the DC supplies to TR1 and TR2.

3.4.4 The Second IF and Third Mixer (A7A6)
(Dwg: CD-253Y5)

The output of the second mixer enters the second IF amplifier via a double-tuned circuit, L1/C2, L2/C5, employing common capacitive coupling via C3. This provides a measure of selectivity at 10.7 MHz, further improving attenuation of spurious products outside the passband. The capacitive divider formed by C2/C1 provides an impedance match between the second mixer output and the input tuned circuit.

A 40673 dual-gate FET, TR1, is the second IF amplifier. Resistor R1 provides a DC return for gate 1. The AGC voltage is applied to gate 2 via R2, which decouples the AGC line. C4 and C7 are RF bypasses. Source bias from the negative supply line is provided by R3.

The output tuned circuit for TR1 is a pi-network formed by C6/L4/C8. Supply voltage for the drain of TR1 is provided via an RF choke, L3. The capacitive divider C9/C8 forms an impedance match to the primary of T7 which is tuned to 10.7 MHz and drives the third mixer. The secondary of T1 provides a low impedance match to the four IN914 mixer diodes and a balanced-to-unbalanced transformation. The 1.6 MHz IF output of the third mixer is taken from the centre-tap of the T1 secondary via L5.

The 9.1 MHz conversion frequency for the third mixer is derived from a Colpitts oscillator using a BSV78 junction FET (TR2). The crystal (XL1) oscillates in the parallel resonant mode at its fundamental frequency. The ratio of C14 to C15 determines the level of feedback.

The crystal oscillator drives the four IN914 mixer diodes via a low impedance, centre-tapped secondary on T2. This provides an impedance match and a balanced-to-unbalanced transformation. The primary of T2 is tuned to 9.1 MHz, resonating with the combined capacitance of C11 in series with the parallel combination of C13/C16. This combination forms a capacitive divider impedance match to the drain of TR2.

The DC supply to the drain of TR2 is via R5. Source bias from the negative supply is provided by R4; R6 is a DC return for the gate.

The positive and negative supplies to TR1 and TR2 are decoupled by L3, L7 and L6, bypassing is provided by C10 and C12.

3.4.5 The Third IF and Detector (A7A7)
(Dwg: CD-253Y6)

This consists of four grounded-base amplifier stages followed by a full-wave diode detector. The input and interstage coupling consists of four, high-Q, double-tuned circuits, common-capacity coupled, providing a steep-sided selectivity response and a bandwidth of 40 kHz. Type BF200 bipolar transistors are employed in each stage of the amplifier.

A capacitive divider, C1/C2, provides matching between the low impedance output of the third mixer and the input double-tuned circuit.

The low impedance input to the emitter of each BF200 is matched with a capacitive divider to each double tuned circuit (i.e. C4/C5 for TR1).

The Q of the collector tuned circuit of each stage is dampened by parallel resistors (R3, R7, R11, R14) to improve stability and the symmetry of the bandwidth response.

The output transformer, T1, has a tuned primary and a low-impedance, centre-tapped secondary. Two OA95 germanium diodes are employed in a full-wave detector. The video output to A7A8 is on terminal 4 of A7A7, following RF filtering by R15, R16 and C28.

Bias for each stage is provided by a resistor from each emitter to the negative rail (R1, R4, R8, R12), each stage being individually decoupled (R2, R6, R10; C6, C10, C16, C24). The DC collector supply to each stage is provided via 1mH RF chokes L4, L7, L10 and L12. The positive DC supply is also decoupled between individual stages (R5, R9, R13; C9, C15, C21, C27).

3.4.6 The Video Output and AGC Circuitry (A7A8) (Dwg: CD-253Y7)

The detector output from A7A7 is direct coupled to a buffer consisting of two emitter followers in cascade, TR1 and TR2, which present a high impedance load to the detector output. TR1 is a PNP transistor, the emitter of which drives the base of an NPN transistor TR3. Bias for TR1 is provided by R2, its emitter load, from the +10 V rail. Bias for TR3 is provided by its emitter resistor, R7, from the -10 V rail as well as via R2.

The received signals appearing on the emitter of TR3 are AC-coupled to the video amplifier (TR4 - TR5) via C1. The A-scan Y-deflection signal is also taken from the emitter of TR3 and goes to the MONITOR display (A10) via pin 1 A7PL1, and the Monitor Function Control switch (S2B) on the PROGRAM unit A5A1.

The video amplifier consists of TR4 and TR5. TR6 interfaces the video to TTL logic levels for the Signal Processing circuitry that follows (Section 3.5). The first stage, TR4, is an emitter follower. An OA95 germanium diode, D1, provides a DC path for forward base bias by TR4. R11/L1 provides a DC return path to ground for the positive-going video signals and compensates for "droop" in the received pulses due to the AC-coupled input (C1).

The emitter of TR4 is at a DC potential of about -1 V (with respect to ground) with no video signals present. It is direct coupled to the base of TR5 via R14. The emitter of TR5 is also maintained at a potential of about -1 V by D2. Thus, TR5 is cut off in the absence of video signals. The collector of TR5 is direct coupled to the base of TR6 via the resistive divider R18/R19. Thus, as TR5 is cut off, the collector potential will be near the +10 V supply, causing TR6 to conduct. The collector of TR6 "holds down" (logic level 0) one input of a gate in the Signal Processor located on A3A12 (pin 2, IC6/A3A12) in the absence of video signals.

Video signals will cause the TR4 emitter voltage to rise, and as they pass a certain amplitude, will forward bias TR5 causing it to conduct. It will rapidly saturate, the collector voltage dropping to near ground potential, thus causing TR6 to cease conducting. This will allow pin 2 of IC6 on A3A12 to go HI for the duration of the received signal. Generally, the AGC circuitry maintains the receiver gain so that only echo pulses will cause TR5 to conduct. As TR5 and TR6 are operated as saturated switches, heavy clipping of the video occurs, removing amplitude information from the echo pulses presented on the ionogram.

The AGC circuitry consists of TR2, a BSV78 JFET which operates as a switch, and an LM308 op-amp (IC1) which functions as a DC amplifier and integrator. The AGC voltage is determined by the level of noise and other signals appearing at the detector output. As the amplitude of these signals increases, the AGC voltage, and thus receiver gain decreases.

The gate of TR2 is coupled to the collector of TR5. The negative-going echo pulses on the collector of TR5 reverse bias the gate of TR2, turning it off, and the drain-source virtually becomes an open circuit isolating the detector output from the input of IC1. The DC output of the detector is proportional to the amplitude of noise and any signals in the bandpass of the receiver. Between echo pulses, the drain-source resistance of TR2 is very low as there is zero gate bias, allowing current to flow into the input of IC1. The output (pin 6 of IC1), and thus the AGC voltage, will fall to a value proportional to the DC output of the

detector, thus decreasing the receiver gain. If the echo pulses do not exceed the noise and interference level, then they will not cause TR5 to conduct and no echo will be present on the ionogram. Thus, in the presence of interference of sufficient strength, gaps appear in the ionogram echo trace.

ICI functions as an integrator owing to the action of C2 placed in negative feedback path between the output and the inverting input, and the series input resistance of R1 and R8. This averages short-term variations of the detector output to allow smooth control of the receiver gain in response to the average value of noise and signals detected by the receiver.

During echo pulses, the AGC voltage is maintained at its value immediately prior to the echo by the charge stored in C2. The input impedance of I01 is very high, and thus C2 will take considerably longer than the echo pulse duration to discharge.

The AGC voltage is derived from the resistive divider R13/R16 forming the output load of IC1. The quiescent value of the AGC voltage is set by the potentiometer R9, part of a resistive divider R9/R10 from the +10 V rail, providing a small positive voltage (about +1.7 V maximum) to the non-inverting input of IC1. The potentiometer, R9, is a trimpot mounted on A7A9 and accessible through the right hand hole on the front panel of the receiver. The AGC voltage can be measured at the right hand test point. The quiescent AGC voltage is set to about 4V for maximum receiver gain and may be subsequently adjusted according to conditions at the station.

3.4.7 AGC Display (A7A9)
(Dwg: CD-323YI)

At the commencement of each Y sweep the LM301 output begins a negative ramp.

At the end of each Y sweep the Y reset line going low causes the output of the LM301 to be short circuited to its input (=VR1) and it remains so until the next Y sweep commencement.

The ramp voltage is compared to the AGC voltage in IC3 and to the limit voltage in IC2. As the ramp voltage passes the AGC voltage IC3 comparator output goes high. This positive transition is gated and triggers the 74123 timer, which produces a 20us pulse. This pulse goes to A3A8 where it is gated into the video. The delay prior to this transition is therefore proportional to how negative the AGC is. If the AGC goes more negative than the limit voltage (approx.0 volts) then comparator IC2 output goes high which is similarly gated to obtain a video pulse.

The 20us pulse is gated into the video where the delay becomes the virtual height of the AGC on the display screen.

To set up the AGC display on the ionogram, vary the AGC preset so AGC is biased at +4 volts for no signal, measured on the right hand test point on the RX front panel.

R6 changes the offset of the AGC line from the bottom of the screen. This is varied by the left hand trim-pot measured on the left hand test point. Set VR1 to approx. + 3 Volts. The maximum height of the AGC line on the display corresponds to the AGC being 0 volts or less (i.e. very strong signals).

3.5
SIGNAL PROCESSING

Par. No.	Title		Drawing No.
3.5.1	Introduction		
3.5.2	Blanking the first 50 km		CD-229Y1 (A3A12)
		also refer	CD-225Y1 (A3A11)
3.5.3	Noise Interference Suppression		CD-229Y1 (A3A12)

3.5.1 Introduction

To present a clear, uncluttered ionogram, the detected echoes and any other signals are processed to remove the ground pulse and any noise interference prior to being displayed on the CRT.

There are three stages to the signal processing, carried out in the following sequence.

(a) The receiver detector output is interfaced to TTL logic levels, the signal being clipped in the process. The AGC system prevents strong, interfering narrowband signals from appearing at the receiver output. These processes are covered in Section 3.4 on the RECEIVER.

(b) The first 333 μS of each part of the transmit pulse sequence is blanked, thus removing the ground pulse and blanking the first 50 km of the ionogram range.

(c) Noise interference is suppressed.

In addition, following the last process, the video being passed to the CRT is blanked between 700 and 750 km during the date/time segment of the ionogram to avoid echoes obscuring the numbers.

A block diagram of the signal processing is given in fig. 3.5.1. The signal processing circuitry is located on A3A12.

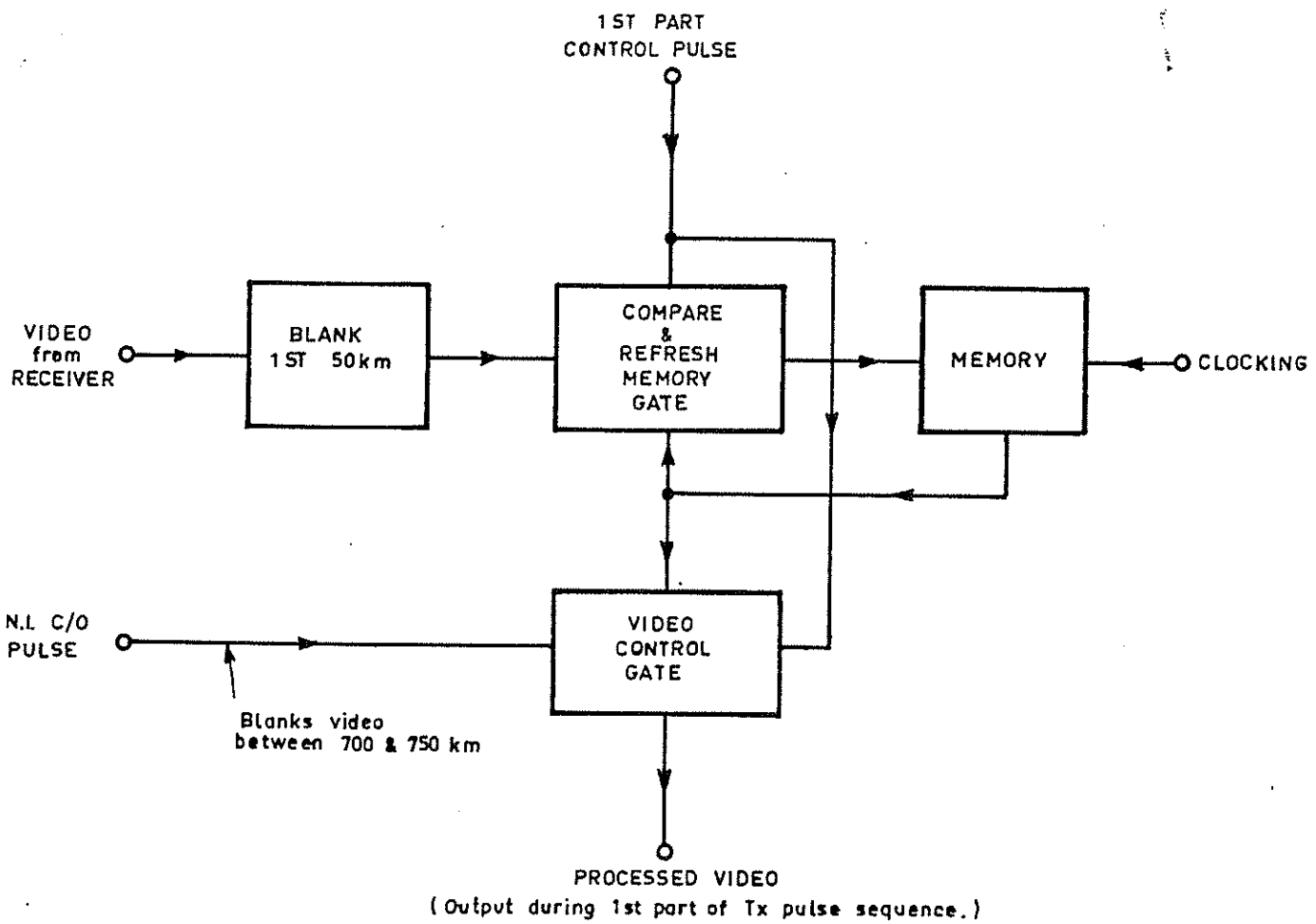


FIG. 3.5.1. Block diagram of signal processing.

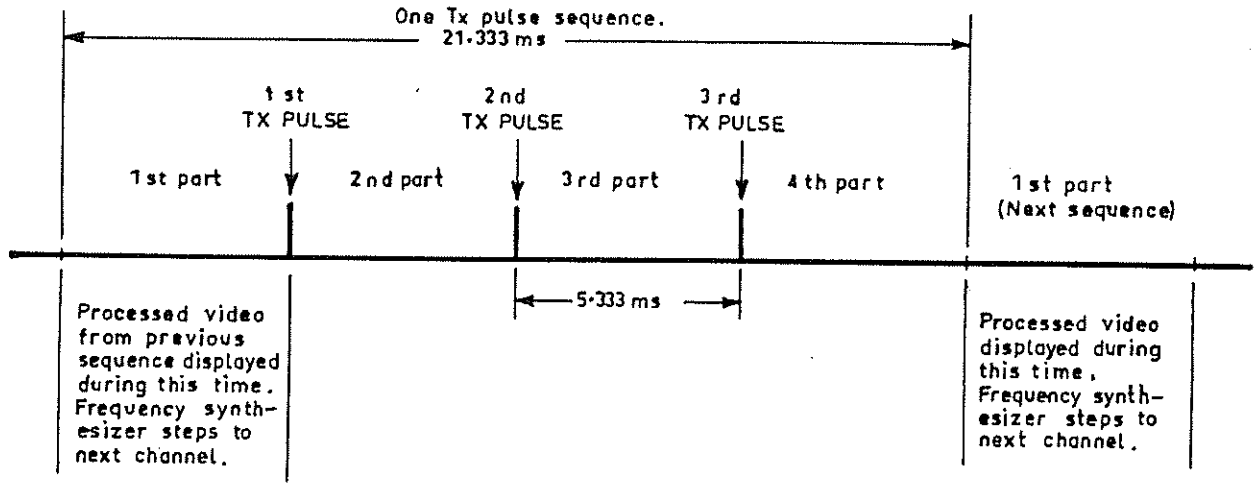


FIG. 3. 5. 2. Transmit pulse sequence.

3.5.2 Blanking the first 50 km

The portions of the circuit for blanking the first 50 km are shown in fig. 3.5.3. The four inputs to IC15 are derived from the A,B,C,D outputs of the first divider in the OPERATIONAL DIVIDERS (IC5) on A3A11. The output of IC15 goes low for the first 333 μS of each 5.33 mS period.

The video input from the receiver is on pin. 28 of A3A12. A transistor (TR6) on A7A8 of the RECEIVER 'holds down' pin. 2 of IC6 (on A3A12) one input of a two-input NAND gate. Echoes or signals turn off TR6 on A7A8 which allows pin. 2 of IC6 to go high. When pin. 1, the other input of IC6 is high, the video from the receiver appears as negative-going pulses at the output, pin. 3. When pin. 1 goes low, for the first 333 μS of each 5.33 mS period, the video is prevented from appearing at the output of IC6, thus blanking the video for the first 50 km of the ionogram range.

3.5.3 Noise interference suppression

Atmospheric static is essentially random in nature and ignition noise, while repetitive, does not exhibit a stable interval between pulses. Use is made of these characteristics to remove noise interference from the video to be displayed by selecting only those video signals which are repetitive over the three parts of the transmit pulse sequence following each transmit pulse.

The first transmit pulse occurs at the commencement of the 2nd-part of the transmit pulse sequence (see fig 3.5.2). Echoes and noise occurring during the second part are stored for 5.33 mS in a static shift register. The shift register acts simply as a delay, the period of the delay being equal to the period between transmit pulses; one 'part' of the transmit pulse sequence i.e. 5.33 mS. Echoes and noise during the 3rd-part, following the second transmit pulse, are then compared by a NAND-gate with the delayed video from the 2nd-part. Only video pulses which are coincident will appear at the output of the NAND-gate. These then become new video data and are recirculated back into the shift register. This data is then compared, 5.33 mS later, with the echoes and noise in the 4th-part. By this time, virtually the only remaining video data will be echoes as they will be coincident from one part of the transmit pulse sequence to the next.

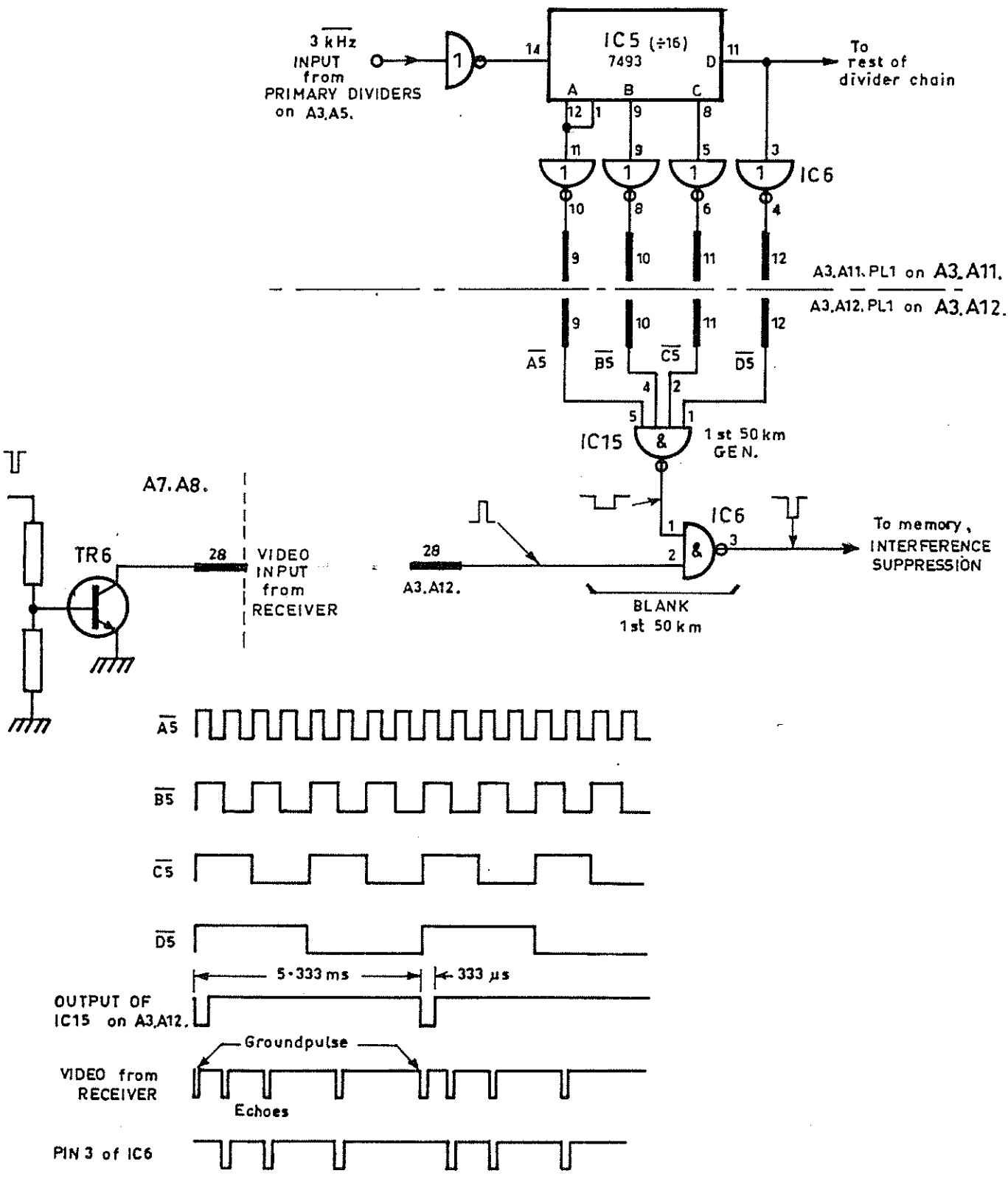
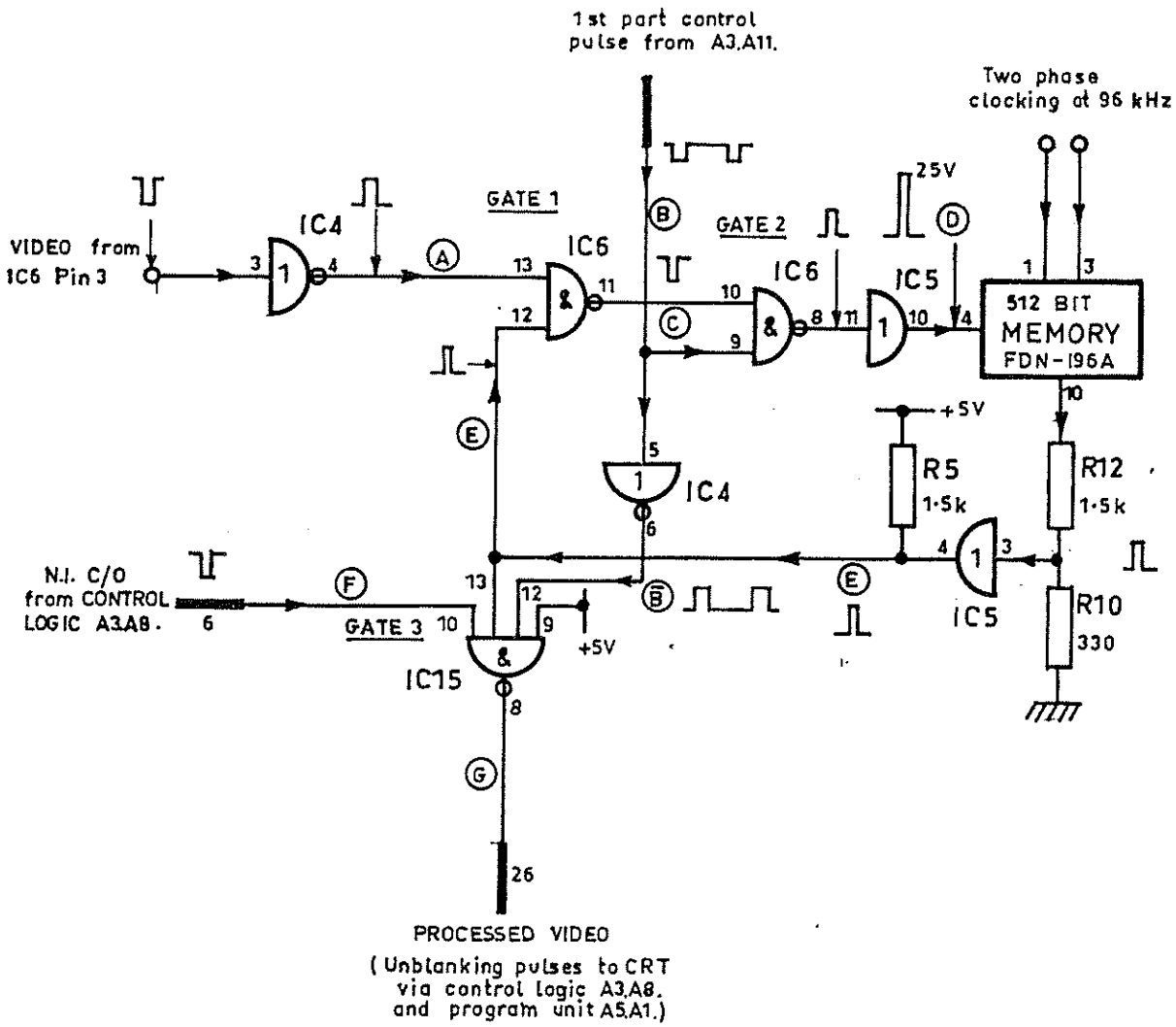


FIG. 3.5.3 Circuitry to blank first 50 km of ionogram



TRUTH TABLE

	A	E	C	B	D	F	$\bar{B}$	G	
	0	1	1	1	0	X	0	1	2nd part
	1	1	0	1	1	X	0	1	
	0	0	1	1	0	X	0	1	3rd & 4th parts
Non-coincidence	1	0	1	1	0	X	0	1	
coincidence	1	1	0	1	1	X	0	1	
	X	0	X	0	1	1	1	1	1st part
	X	1	X	0	1	1	1	0	
700 - 750 km	X	1	X	0	1	0	1	1	

FIG. 3. 5. 4. Circuitry for noise interference suppression (on A3.A12.)

The portion of the circuit performing noise interference suppression is shown in fig 3.5.4. Each line on the circuit, of importance to this discussion is labelled, A to G. Three NAND-gates control the operation of the circuit. Gate 1 passes video to the shift register via gate 2 which loads the video data into the shift register or inhibits it. Gate 3 is the output gate. The video to be displayed consists of negative-going pulses on line G. If any input to gate 3 is a 0 then the output remains at a 1.

Initially, for the 5.33 mS of the first part of the transmit pulse sequence, line B is 0 which forces a 1 on the output of gate 2 (pin 12, IC6) during the second part of the transmit pulse sequence. The video pulses, following blanking of the first 50 km, are inverted to provide positive-going pulses at A, the other input of gate 1 (pin 13, IC6). The video then appears at C as negative-going pulses. Line B is now a 1 and remains so for the 2nd, 3rd and 4th parts of the transmit pulse sequence. This is inverted in IC4, holding the output of gate 3 to a 1. The video pulses from the 2nd part, on line C, are inverted to positive going pulses by gate 2, and passed to the shift register. They appear 5.33 mS later on line E at pin 12 of IC6, one input of gate 1. At the same time, video pulses from the 3rd part, following the second transmit pulse, are appearing on pin 13 of IC6, the other input of gate 1. As this is a NAND-gate, only input pulses which coincide (1-1) will activate the output, pin 11 (line C). This new video data is then inverted by gate 2 and passed to the shift register. This then appears, 5.33 mS later, on line E and the comparison repeated for video from the 4th part, in gate 1. The resultant video, consisting only of coincident pulses, is again passed to the shift register.

At the end of the fourth part, line B goes to a 0, forcing a 1 on the output of gate 2 again and inhibiting any further video pulses from being passed to the shift register. At the same time, it enables gate 3, allowing video pulses on line E to be passed to the output, line G (pin 26 A3A12/PL1).

Line F is normally high (1), going low for 333 μS, or 50 km of range, 4.66 mS after the start of each part of the transmit pulse sequence, i.e. between 700 and 750 km of range. This forces a 1 on the output of gate 3, for this part of the range, preventing video pulses from appearing between 700 and 750 km on the ionogram where the numerals are displayed. The 'N I c/o Pulse' is the signal on line F (from pin 6, A3A12/PL1) and it is only present for the first 5.46 seconds of a sounding.

The pulse diagrams illustrating the processes occurring during the transmit pulse sequence are illustrated in fig. 3.5.5.

The shift register is clocked at a repetition rate of 96 kHz. This is derived from the divider in the Master Oscillator/Divider also located on A3A12. In each 5.33 mS of the transmit pulse sequence, there are 512 'bits' of 10.4166 uS duration, about 1.6 km of range.

The shift register is a MOS device requiring a negative supply voltage of 10 V. in addition to the normal 5 V logic supply.

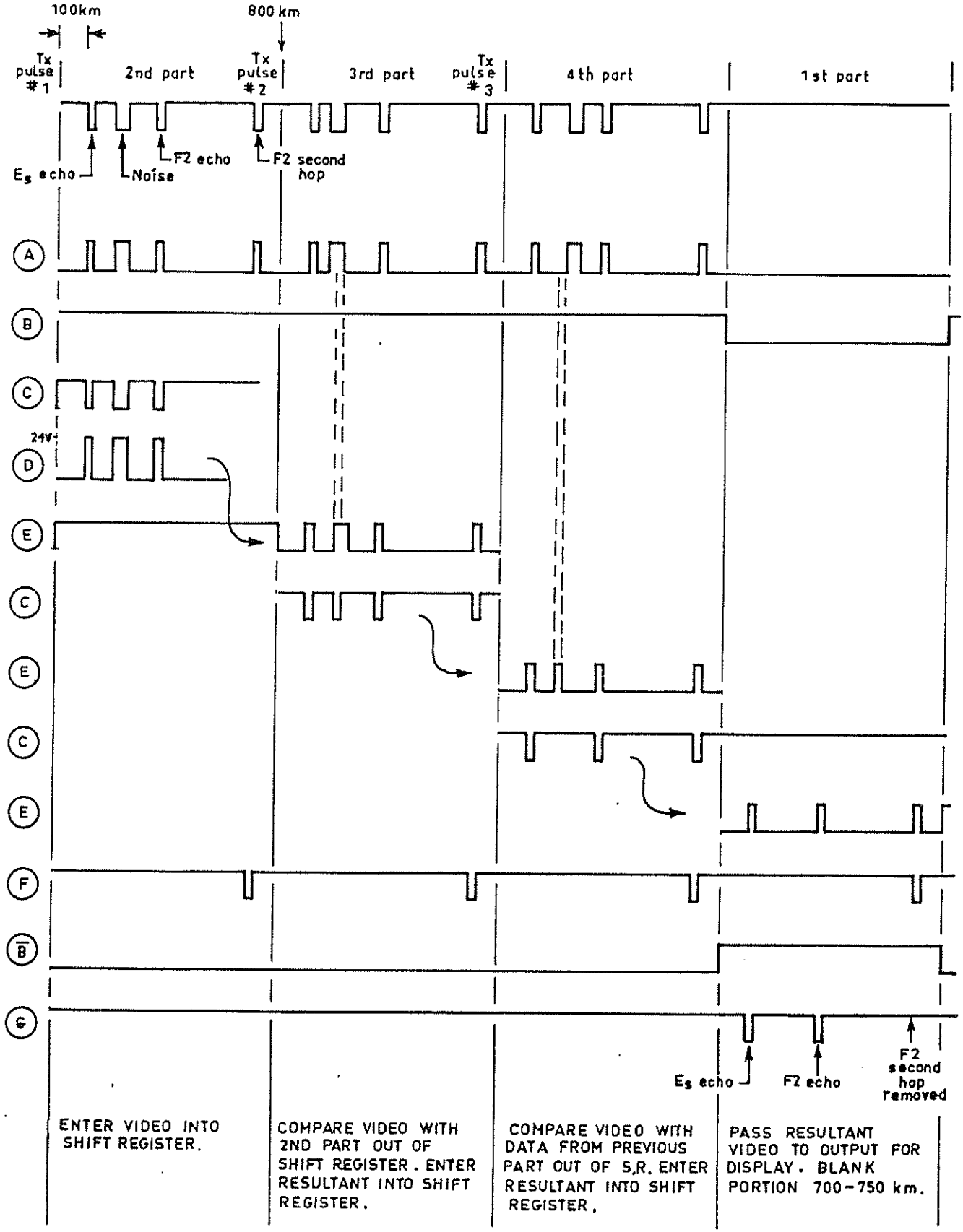


FIG. 3.5.5. Operation of Noise Suppression Circuit.

3.6
NUMERAL GENERATION

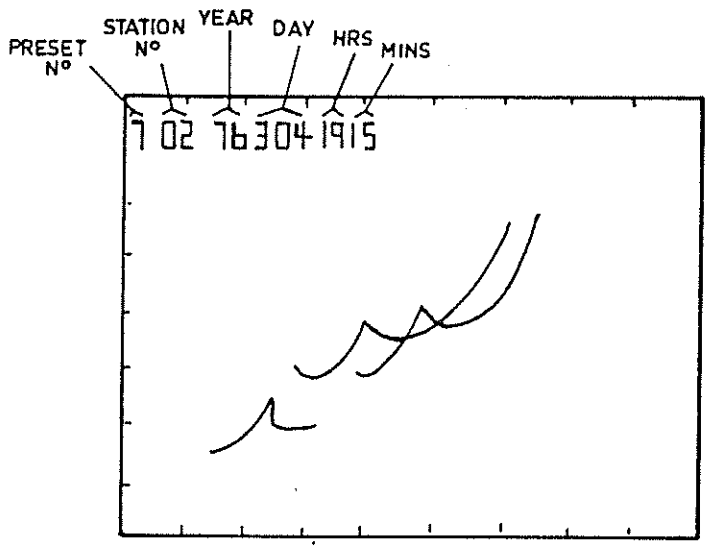


FIG. 3.6.1. Numbers displayed on the ionogram.

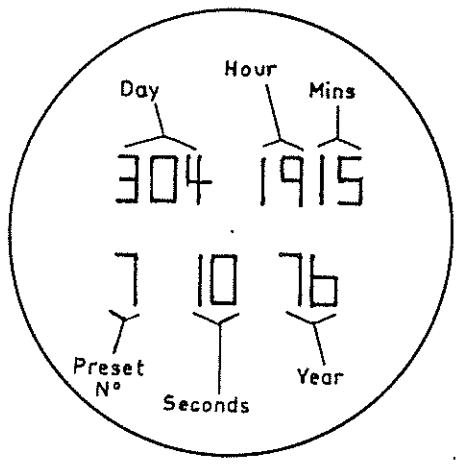


FIG. 3. 6. 2 Numbers displayed on the N.I. Display (On monitor)

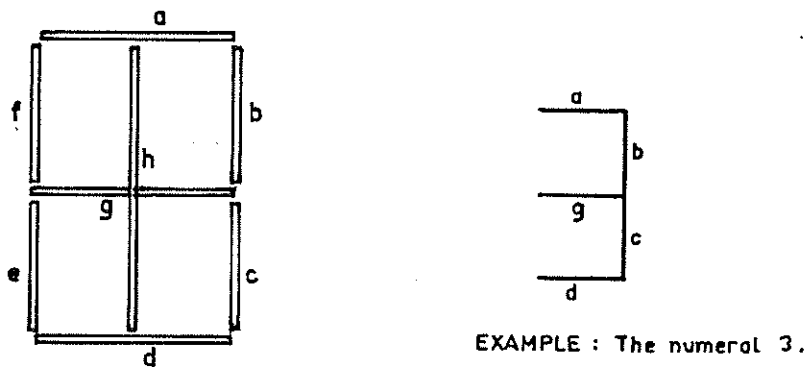


FIG. 3. 6. 3. Illustrating the way the eight segment numerals are made up.

NUMERAL SELECTION, GENERATION AND DISPLAY

3.6.1 Introduction

The numbers displayed on the ionogram and the N.I. Display are illustrated in figure 3.6.1 and 3.6.2. The date/time numbers are derived from the output of dividers in the Chronometer section of the clock. These outputs are a four-bit BCD code. The code for each numeral of the date/time numbers is converted to CRT brightening pulses by the NUMERAL GENERATOR A3A4.

In addition to the Chronometer outputs, two other numbers are displayed. These are the 'Preset Number' and the 'Station Number'. The Preset Number was originally included to indicate the Frequency Synthesizer operating modes but is not now used. It is 'hard-wired' and is produced by portion of the commutation circuitry. The Station Number is also a hard-wired portion of the commutation circuitry but is different for each station. A particular number is obtained by bridging terminal pins on the printed circuit board of the MASTER COMMUTATION unit A3A6. (See also Section 3.6.7).

The unit that generates the brightening and blanking pulses for the numerals is designated the NUMERAL GENERATOR, A3A4, and is located in the card file of the top rack assembly of the ionosonde. The BCD outputs from the chronometer section of the clock are selected for the Numeral Generator input by the MASTER COMMUTATION circuit, A3A6 which selects each numeral in the required sequence for the N.I. Display and the ionogram. This is driven by the COMMUTATION GENERATOR, A3A10 which also provides two inputs to the Numeral Generator for generating the horizontal and vertical segment brightening and blanking pulses. These two units are also located in the card file of the top rack assembly of the ionosonde. Digital TTL integrated circuits are used throughout the Numeral Generator and commutation circuitry.

The numerals are selected and displayed in sequence, from left to right on both displays, commencing with the Preset Number. On the N.I. Display, the Preset Number, Seconds and Year are displayed first, on the lower line. The Days number and Time (hours-minutes) follow on the upper line. The Station Number is not displayed on the N.I. Display, being replaced by the Seconds.

A numeral is made up from the required number of segments of an eight segment pattern as shown in figure 3.6.3. Each segment is designated a b c d e f g h in clockwise order. Thus, for example, the numeral 3 comprises segments a b c d and g.

Each numeral is generated in a period of sixteen y-sweeps (called the 'numeral generation period'). The 1st, 15th and 16th sweeps are always blanked. The trace is brightened for particular portions of the 2nd to 14th sweeps to 'write' the various segments. This is illustrated in figure 3.6.4. The vertical deflection is divided into sixteen 'time blocks'. The trace is always blanked during the 1st, 15th and 16th time blocks of each y-sweep. Horizontal segments are produced by brightening the trace during the 2nd, 8th or 14th time block of each y-sweep. For example, the 'a' segment is produced by brightening each y-sweep during the 14th vertical time block. Vertical segments are produced by brightening the trace during the 2nd, 8th or 14th y-sweep. For example the segment 'e' is produced by brightening the trace during the first half of the 2nd y-sweep.

For the N.I. Display, the y-sweep (Y-NI) is initiated each 83.33 uS and the blanking and brightening pulses required to write each numeral are generated in 1.33 mS, the period of sixteen y-sweeps. The vertical deflection time blocks are each 5.2 uS long. The display is completed in 256 y-sweeps, a period of 21.33 mS. The X and Y deflection sequences are explained in section 3.8.14 and illustrated by figure 3.8.6.

On an ionogram, the numerals are written between the 700 km and 750 km height markers extending from the left hand edge of the graticule to the fourth frequency marker, as illustrated in figure 3.6.1. Thus, the numerals occupy only a 333 uS period of each ionogram y-sweep, 4.66 mS from the commencement of each sweep. The ionogram y-sweeps are only 6 mS long and are initiated at 21.33 mS intervals. Each numeral on the ionogram, as it requires sixteen y-sweeps, will be generated in a period of 341.33 mS, the whole series of numbers takes 256 y-sweeps, a period of 5.4163 seconds. The 700-750 km portion of the y-sweep is divided into sixteen time blocks of 20.83 uS for the horizontal segments of the numerals (see figure 3.6.4).

3.6.2 The Numeral Generator A3A4.
(Dwg: CD-222Y1)

There are three basic inputs to the Numeral Generator, as follows:

(a) A four-bit BCD code, representing the numeral to be displayed originating from the chronometer dividers as explained previously. This enters IC4, a type 7442 BCD to decimal decoder, via pins 2,3,4,5 of A3A4/PL1.

(b) A four-bit binary code that is used to generate the vertical segments brightening and blanking pulses. This enters IC8, also a 7442 BCD to decimal decoder, via pins 28, 29, 30, 31 of A3A4/PL1. This input originates in the OPERATIONAL DIVIDERS on A3A11 and comes via the COMMUTATION GENERATOR, A2A10.

(c) Another four-bit binary code used to generate the horizontal segments brightening and blanking pulses. This enters IC12, another 7442 BCD to decimal decoder, via pins 18, 19, 20, 22 of A3A4/PL1. This input originates in the PRIMARY DIVIDERS of the clock on A3A5 and comes via part of the commutation circuitry on that board.

In addition, there are two other inputs. These are designated the 'Upper segments (b,f) Control Line' and the 'Lower Segments (c,e) Control Line'. These carry complementary-phase pulses that control the blanking or brightening of the vertical segments b,c,e, and f. They enter via pins 21 and 22 respectively, of A3A4/PL1. Note that pin 22 is also one input line of the four-bit binary input to IC12.

As the ionogram and N.I. Display are generated at different sweep rates, the inputs to IC8 and IC12 are altered, the cycling rate of the binary inputs being changed, so that the numeral segments blanking and brightening pulses are the required widths and are generated at the required rates for the two displays. The input to IC4 is also changed simultaneously, along with the rate and sequence of numeral selection, so that the numerals are presented to the Numeral Generator at the appropriate time and in the required sequence, the STATION NUMBER displayed on the ionogram being replaced by the seconds on the N.I. Display as well. The changeover of the inputs is carried out by the commutation circuitry under the action of the 'N.I. c/o Pulse' which is generated by portion of the CONTROL LOGIC circuitry on A3A8. (See Sections 3.7.8 and 3.7.10).

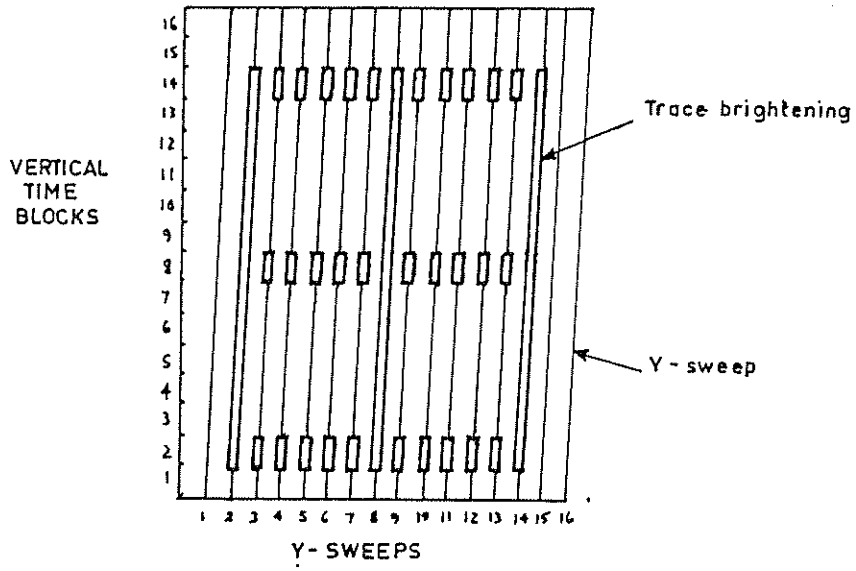


FIG. 3.6.4. Illustrating how the CRT trace is brightened to produce the numeral segments.

An ionogram may be initiated and displayed each sounding period, that is, each 20 seconds. (See section 3.1.15). The ionogram display sequence commences at second number two of each sounding period and has a duration of 12.309 seconds - as explained in Section 3.8. The N.I. Display may be displayed on the Monitor CRT all the time, simultaneously with an ionogram being displayed on the Main CRT. The inputs to the Numeral Generators are therefore changed during the first 5.4163 seconds of an ionogram for a period of 333 uS each 21.33 mS, 4.66 mS after the commencement of each ionogram y-sweep. The timing and period of the change corresponds with the position of the numerals on the ionogram and thus the Numeral Generator produces the required numeral segment brightening pulses. The complete N.I. Display is generated in 21.33 mS as explained in Section 3.6.1.

The input changeover action causes part of the SECONDS units numeral to be blanked while an ionogram is being written on the Main CRT when an N.I. Display is appearing on the Monitor. The blanking occurs during the 333 uS changeover period which is 4.66 mS from the commencement of the N.I. Display. This corresponds to the period of four Y-N1 sweeps at the middle of the seconds units numeral and occurs during the first 5.4 seconds of an ionogram. As the N.I. Display is provided for the operator's convenience, this is of little consequence.

The truth table indicating the basic operation of a 7442 IC is given in Table 1. Each output pin is normally high. As the BCD code equivalent to each decimal number from 0 to 9 is presented to the input, the output pin with the corresponding designation will go low. For example, if the BCD code equivalent to decimal 3 appears on the input of the 7442, pin 4 will go low. All the output pins will remain high if the BCD input beyond decimal 9 equivalent is presented to the input.

The operation of IC4 is essentially as indicated in Table 1. The output pins 1,3,4,6,7 and 11 control the writing of those numerals having greater than four segments, with the exception of the numeral 8, viz: 0,2,3,5,6 and 9. Pin 10 is unconnected as the circuitry is arranged to generate the segment brightening pulses for an '8' continuously. Appropriate segment brightening pulses are gated off to produce the other 'greater than 4-segment' numerals. The output pins 2,5 and 9 of IC4, control the writing of those numerals having less than four segments, viz: 1,4 and 7.

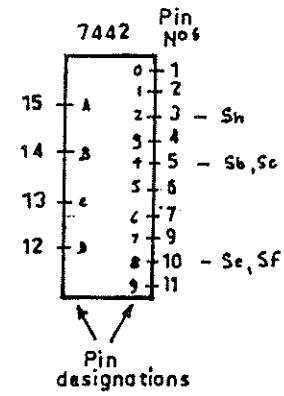
DECIMAL	INPUT A	B	C	D	OUTPUTS 0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	1	0	0	0	1	0	1	1	1	1	1	1	1	1
2	0	1	0	0	1	1	0	1	1	1	1	1	1	1
3	1	1	0	0	1	1	1	0	1	1	1	1	1	1
4	0	0	1	0	1	1	1	1	0	1	1	1	1	1
5	1	0	1	0	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	1	1	1	1	1	0	1	1	1
7	1	1	1	0	1	1	1	1	1	1	1	0	1	1
8	0	0	0	1	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	1	1	1	1	1	1	1	0
10	0	1	0	1	1	1	1	1	1	1	1	1	1	1
11	1	1	0	1	1	1	1	1	1	1	1	1	1	1
12	0	0	1	1	1	1	1	1	1	1	1	1	1	1
13	1	0	1	1	1	1	1	1	1	1	1	1	1	1
14	0	1	1	1	1	1	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Pin Nos →	15	14	13	12	1	2	3	4	5	6	7	9	10	11

Truth Table for 7442 BCD-to-Decimal decoder.

TABLE 1

	BINARY INPUT A	B	C	D	DECIMAL EQUIV	Y SWEEP No	7442 OUTPUTS	FUNCTION
One numeral generation period.	1	0	0	1	9	1	Pin 11 : 0	Blank 1st Y-sweep.
	0	0	0	1	8	2	Pin 10 : 0	Brighten e-f.
	1	1	0	1	11	3		
	0	1	0	1	10	4		
	1	0	0	0	1	5		
	0	0	0	0	0	6		
	1	1	0	0	3	7		
	0	1	0	0	2	8	Pin 3 : 0	Brighten h
	1	0	1	1	13	9		
	0	0	1	1	12	10		
	1	1	1	1	15	11		
	0	1	1	1	14	12		
	1	0	1	0	5	13		
	0	0	1	0	4	14	Pin 5 : 0	Brighten b-c
	1	1	1	0	7	15	Pin 9 : 0	Blank 15th sweep
	0	1	1	0	6	16	Pin 7 : 0	Blank 16th sweep

TABLE 2 Operation of IC8.



IC8 generates brightening pulses for the vertical segments b-c, e-f and h. It also generates blanking pulses for the 1st, 15th and 16th Y-sweeps for each numeral. This process is illustrated in Table 2 and the relationship between the input. output and y-sweep waveforms is apparent from figure 3.6.5.

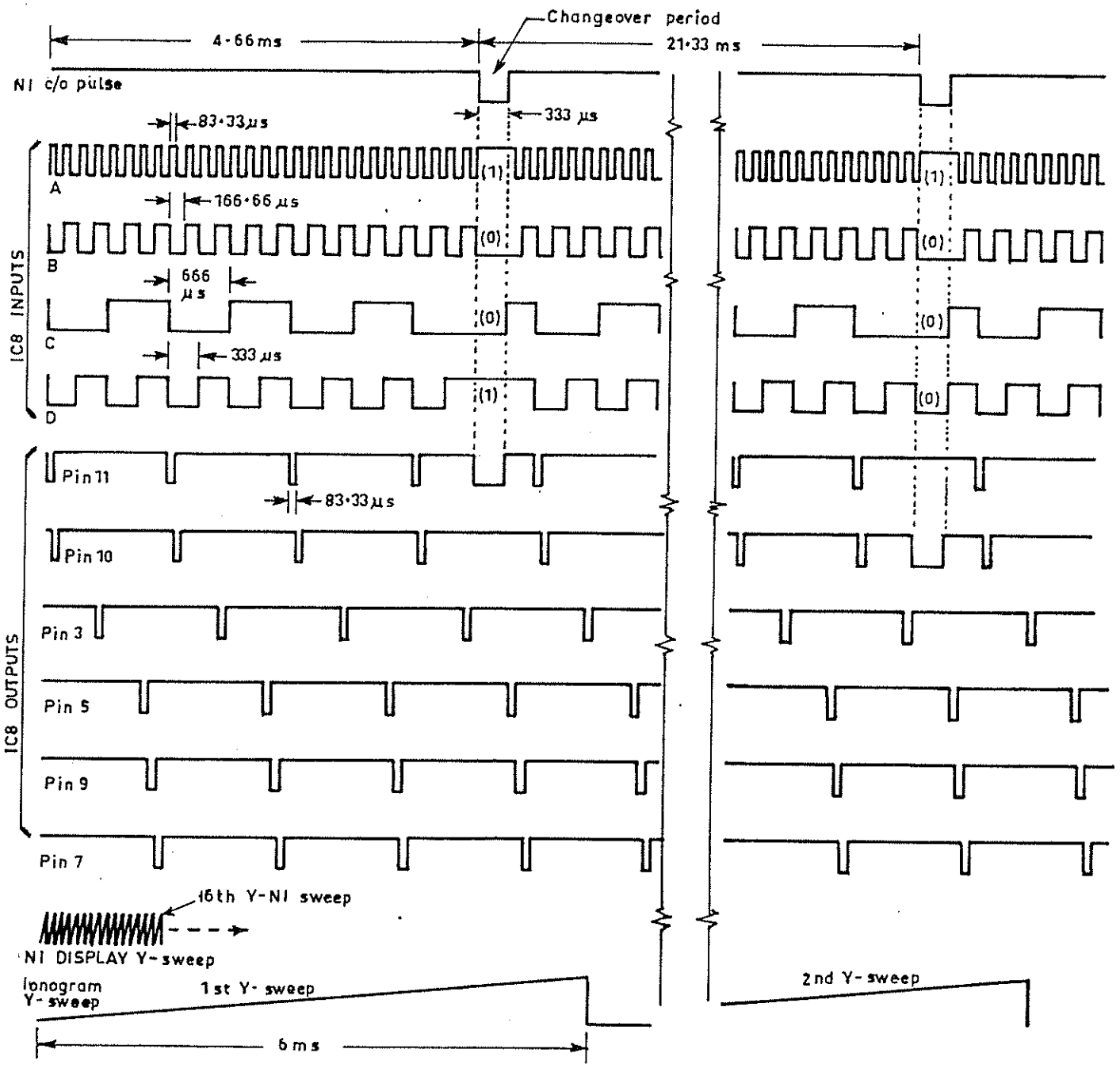


FIG. 3.6.5. Generation of the vertical segment brightening pulses by IC8 showing the relationship between its input, outputs and the Display Y-sweep waveforms.

	BINARY INPUT				DECIMAL EQUIV.	VERTICAL TIMEBLOCK No	7442 OUTPUTS	FUNCTION
	A	B	C	D				
One Y-sweep period	1	0	0	1	9	1	Pin 11 : 0	Blank 1st timeblock
	0	0	0	1	8	2	Pin 10 : 0	Brighten d
	1	1	0	1	11	3		
	0	1	0	1	10	4		
	1	0	0	0	1	5		
	0	0	0	0	0	6		
	1	1	0	0	3	7		
	0	1	0	0	2	8	Pin 3 : 0	Brighten g
	1	0	1	1	13	9		
	0	0	1	1	12	10		
	1	1	1	1	15	11		
	0	1	1	1	14	12		
	1	0	1	0	5	13		
	0	0	1	0	4	14	Pin 5 : 0	Brighten a
	1	1	1	0	7	15	Pin 9 : 0	Blank 15th timeblock
	0	1	1	0	6	16	Pin 7 : 0	Blank 16th time block

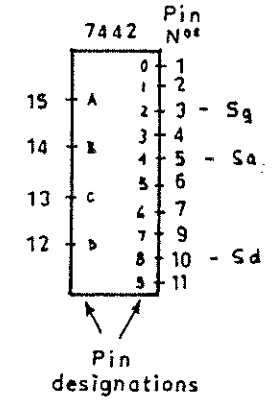


TABLE 3

Operation of IC12.

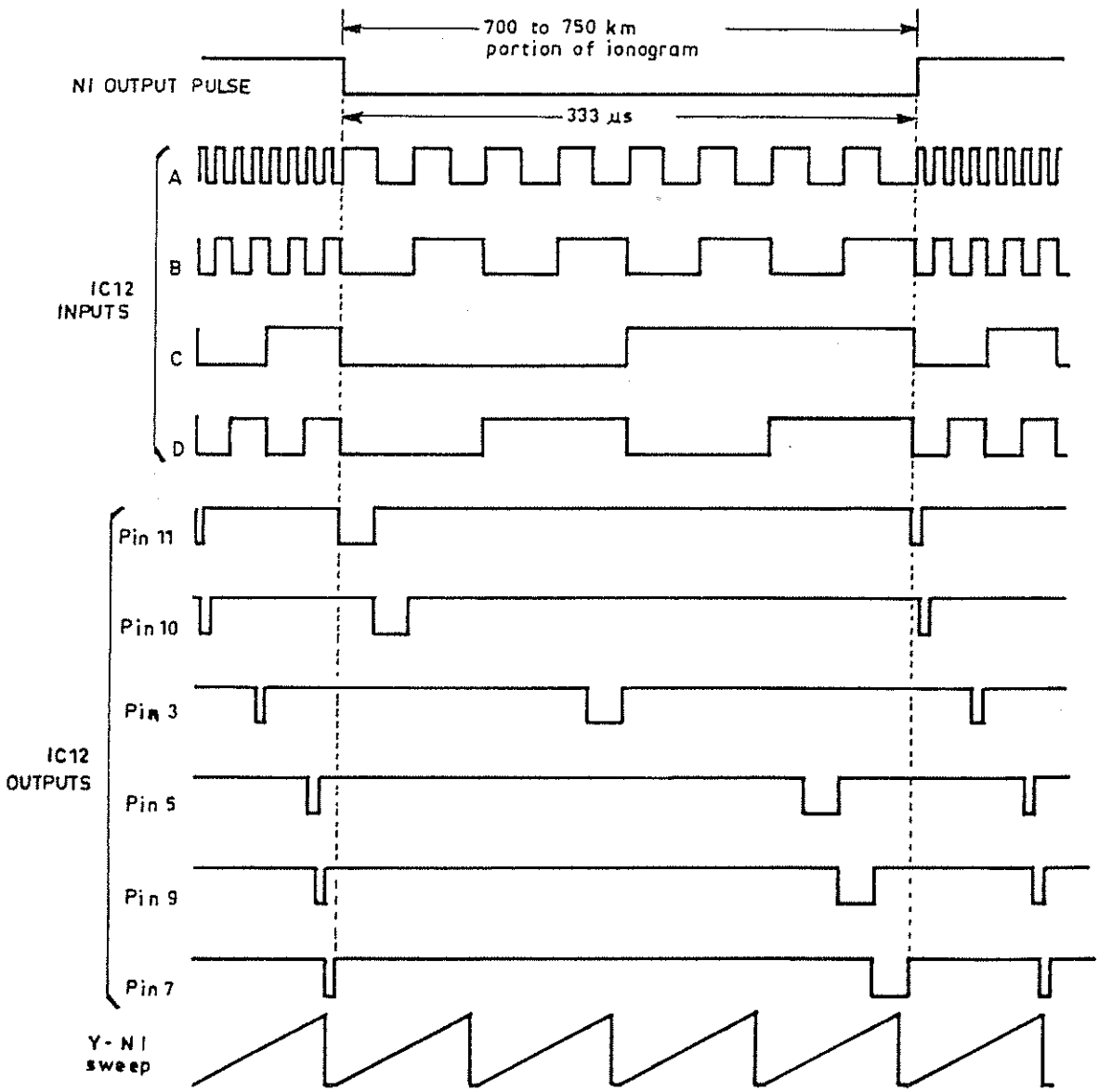


FIG. 3. 6. 6. Generation of the horizontal segment brightening pulses by IC12 showing the relationship between its input, outputs and the Display Y-sweep waveforms.

The horizontal segments brightening pulses are generated by IC12. It also generates blanking pulses for the 1st, 15th and 16th time blocks for each numeral. The process is illustrated in Table 3 and the relationship between the input, output and y-sweep waveforms is apparent from figure 3.6.6.

Before proceeding to a description of the rest of the circuitry, the operation of the output gate IC11, should be described. This is a type 7430, eight-input NAND-gate. Its output, pin 8, provides the numeral blanking and brightening pulses to the video section of the CONTROL LOGIC on A3A8, via pin 15 of A3A4/PL1 (see section 3.7.9). To blank the CRT trace, the output of IC11 goes high, while to brighten the trace, it goes low.

Positive-going numeral segment brightening pulses (from pin 6 of IC6) produced by the rest of the circuitry, drive one input (pin5) of IC11. Thus, negative-going segment brightening pulses appear at the output of the Numeral Generator.

The output pulses from pins 7,9 and 11 of IC8 each drive one input of IC11. These outputs go low during the 1st, 15th and 16th y-sweeps, respectively, of a numeral generating period, driving the output of IC11 high, and thus blanking the CRT trace for these sweeps.

Similarly, the output pulses from pins 7, 9 and 11 of IC12 blank the CRT trace during the 1st, 15th and 16th time blocks during each y-sweep.

In order to separate the different numbers from each other, the CRT trace is blanked for a period of sixteen y-sweeps between the last numeral of a number and the first numeral of the succeeding number. This occurs in the following way.

The Commutation Generator causes all the numeral input lines (pins 2,3,4,5 of A3A4/PL1) to be driven high for the period between each number. A two-input NAND gate (pins 1,2,3 from IC6) senses the condition of pins 4 and 5 of A3A4/PL1. The output of this gate (pin 3) drives one input of IC11 (pin 4). This is normally high as pins 4 and 5 of A3A4/PL1 are never simultaneously high when a numeral (which is always between 0 and 9) is to be displayed (See Table 1). When the numeral input lines go high, pin 3 of IC6 will go low, forcing the output of IC11 high, blanking the CRT trace for the sixteen y-sweeps between numbers.

The process of generating the numerals can be separated into two parts: generating the 'Greater than 4-segment numerals' 0,2,3,5, 6,8 and 9; and generating the 'Less than 4-segment numerals' 1,4 and 7. The description and circuit operation of these two processes follow.

3.6.3 Generating the 'Greater Than Four-Segment Numerals' (Dwg: CD-222Y1)

The circuitry to generate these numerals first involves a group of NOR-gates from IC7 designated the 'Vertical Segment Control Gates'. These divide the 'Sb, Sc' and 'Se, Sf' outputs of IC8 into separate segment brightening pulses for segments b and c, and e and f respectively, by gating these outputs with the upper segments control line and the lower segments control line as illustrated in figure 3.6.7.

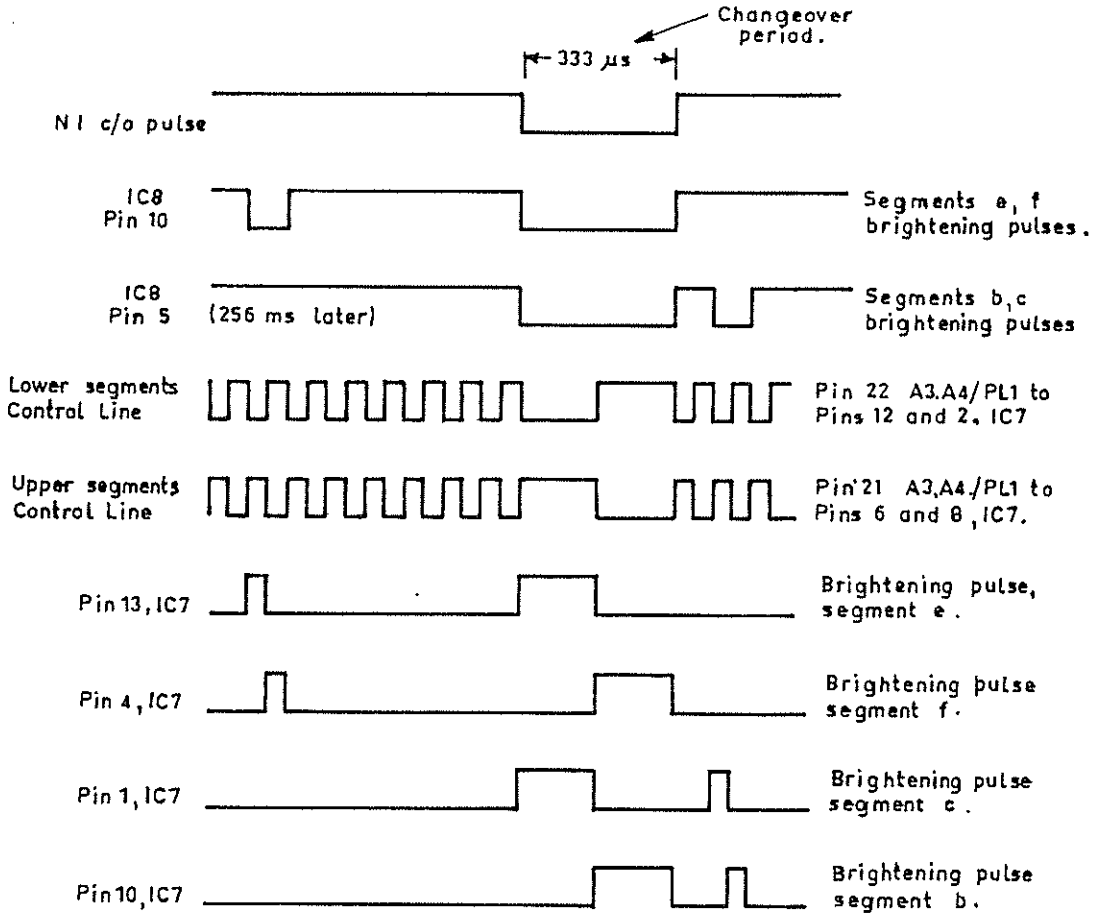


FIG. 3. 6. 7. Operation of the 'Vertical Segment Control Gates."

Next, a group of seven NAND-gates, designated the 'Greater than 4-segment Numerals Control Gates', provide the appropriate segment brightening pulses required for a numeral, in parallel form. Each gate has one input driven by segment brightening pulses. The other input, or inputs, of each gate being connected to one or more of the numeral outputs from IC4. The output of each gate has a designation (Sa etc, to Sg) indicating which segment brightening pulses appears on that particular output.

When one of the greater than 4-segment numerals is to be displayed, except for the 8, the appropriate output pin of IC4 goes low. This forces the output of appropriate control gates high, gating off those segment brightening pulses not required to write the particular numeral.

As the numeral 8 is comprised of all segments a to g, pin 10 of IC8 (decimal 8 output) is unconnected and none of the segment brightening pulses will be gated off.

The seven control gate outputs, Sa to Sg, each drive one input to IC9, a type 7430 eight-input NAND-gate. This gate converts the segment brightening pulses presented in parallel at its inputs to a group of pulses in serial at the output (pin 8, IC9). The output consists of positive-going pulses, these going to one input of a four-input NAND-gate from IC3 (pin 5), a 7420. The other three inputs of this gate are driven by the decimal 1,4, and 7 outputs of IC4. These are normally high, and the segment brightening pulses for the less than 4-segment numerals are passed to pin 5 of IC6, one input of a two-input NAND-gate. The other input (pin 4) will be high, pulled-up by R1, at this time and the negative-going pulses from the output of IC3 will be inverted at the output of the two-input NAND-gate, pin 6 of IC6. This drives one input, pin 5, of IC6 and the segment brightening pulses are gated to the output of the Numeral Generator as described in the previous section, via IC11.

When one of the less than 4-segment numerals is to be displayed, one of the decimal 1,4, or 7 outputs of IC4 (pins 2,5,9 respectively) will go low. Thus, one of the inputs pins 1,2, or 4, or IC3 will go low forcing the output of this gate, pin 6, high and gating off the segment brightening pulses from IC9.

3.6.4 Generating the 'Less Than Four-Segment Numerals' (Dwg: CD-222Y1)

The circuitry to generate these numerals involves a group of three two-input NAND-gates from IC1 having open-collector outputs, each connected in parallel. These are designated the 'Less than 4-segment Control Gates'. Each one only gates through the segment brightening pulses for a particular numeral. The gates are thus labelled 'write 1', 'write 4' and 'write 7'.

The Write 1 gate has one input (pin 3, IC1) driven by the decimal 1 output of IC4 (pin 2) via an inverter from IC2. The other input is driven by the h-segment brightening pulse from pin 3 of IC8 via another inverter from IC2. When the numeral 1 is to be displayed, pin 4 of IC4 goes low and pin 3 of IC1 goes high. At the same time, pin 2 of IC3 goes low. This inhibits the brightening pulses from the output of IC9 from appearing on pin 6 of IC3 as this will be forced high, driving pin 5 of IC6 high. When the segment h brightening pulse is generated by IC8, IC1 gates it (as a negative-going pulse) through to pin 4 of IC6. As pin 5 of IC6 is high, the brightening pulse appears on pin 6 of IC6, now a positive-going pulse. As this drives pin 5 of IC11, all the other inputs of which are high at this time, the segment h brightening pulse is gated through to the output of the Numeral Generator and the Numeral 1 is written on the CRT.

The Write 7 gate works in a similar manner. One input (pin 8 of IC1) is driven by the decimal 7 output of IC4 (pin 9) via an inverter from IC2. The other input (pin 9) is driven by the output of a two-input NAN-gate from IC1 (pin 4). This gate adds in serial the segment 'a' brightening pulses and the segments b-c brightening pulse from IC8. When pin 9 of IC4 goes low, pin 6 of IC3 and pin 5 of IC6 go high, the segment brightening pulses are then gated through to the output of the Numeral Generator as explained above and the numeral 7 is written on the CRT.

The Write 4 gate works in the same way. The decimal 4 output of IC4 (pin 5) drives pin 12 of IC1 via an inverter from IC2. The other input (pin 11) is driven by the output of a three-input NAND-gate from IC10 which generally adds the f, g and h segment brightening pulses. The numeral 4 is written on the CRT, when pin 5 of IC4 goes low.

3.6.5 The Commutation Circuitry (Dwgs: CB-30Y1, CD-249Y1, CD-227Y1, CD-223Y1)

The Commutation Circuitry is basically divided into two parts:- The COMMUTATION GENERATOR (A3A10) and the MASTER COMMUTATION (A3A6). Both of these units are located in the card file of the top rack assembly of the Ionosonde.

The Commutation Generator consists of a series of six digital switches, four of which are located on A3A10, the other two being located on the SECONDS board A3A5, of the Chronometer section of the Sonde Clock. These switches select BCD outputs from the Operational Dividers and the Secondary Dividers of the sonde Clock to drive the Master Commutation Circuitry input, and the Numeral Generator vertical segments and horizontal segments inputs.

As explained in the previous sections, the rate of numeral generation and selection is different for the ionogram and N.I. Displays. Under the action of the NI c/o pulse from the CONTROL LOGIC on A3A8, the digital switches select a different set of BCD outputs from the Clock for the 700-750 km portion of each of the first 256 ionograms y-sweeps.

The Master Commutation Circuitry is functionally divided into four parts:-

(a) The Primary Commutation Generator which generates pulses that 'enables' the output circuits of the SECONDS, YEARS, DAYS and HOURS/MINS Chronometer dividers in sequence, and the STATION Number also.

(b) The Secondary Commutation Generator which generates pulses that gate each numeral output from the Chronometer dividers output circuits in sequence onto the Numeral Generator input lines.

(c) Primary Commutation for the 'Station Number, Replacement of Seconds' which 'enables' either the Chronometer SECONDS divider output circuit for the N.I. Display, or the STATION Number output circuit for the Ionogram.

(d) Secondary Commutation for the 'Station Number, Replacement of Seconds' which gates in sequence each numeral output from the Seconds dividers output circuitry or the Station Number circuitry.

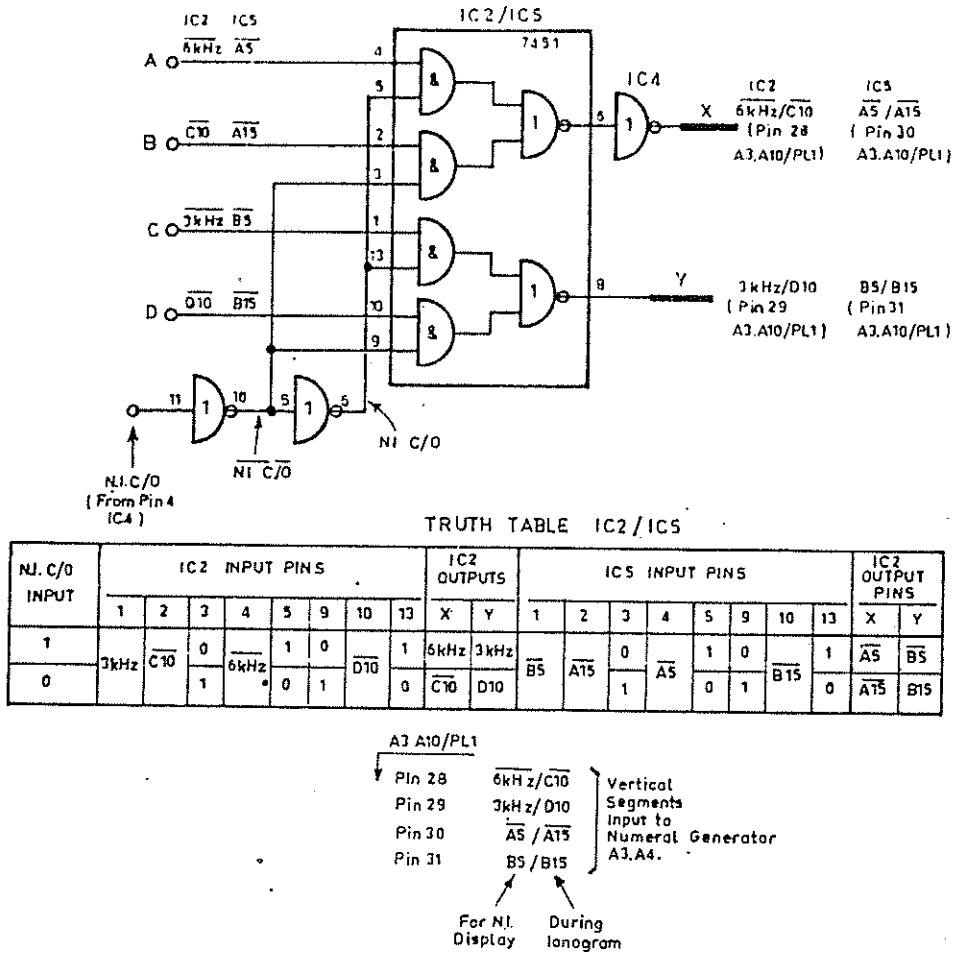
As mentioned previously, the Station Number is derived from a 'hard-wired' portion of the circuitry which is located on the Master Commutation board A3A10.

3.6.6 The Commutation Generator
(Dwgs: CD-249Y1 and CD-227Y1)

Four, type 7451, AND-OR-INVERT gates located on A3A10, and a further two located on A3A5, perform the function of digital switches. On A3A10, IC9 drives the Primary Commutation input of the MASTER COMMUTATION circuit (A3A6) and IC7 drives the Secondary Commutation input. The operation of each is apparent from figure 3.6.8. During the period in which the numerals are written on the ionogram, the NI c/- line goes low for 333 ms each 21.33 ms, 4.66 ms after the commencement of each ionogram y-sweep as explained previously. This causes the 7451 switches to gate through the different inputs. These are two-bit binary codes from the outputs of the OPERATIONAL DIVIDERS on A3A11.

The other two digital switches on A3A10, IC2 and IC5, switch the four-bit binary input to the vertical segments input of the Numeral Generator A3A4. One output of each is inverted by an inverter from IC4 to present the required binary code. Their operation is apparent from figure 3.6.9. The output wave forms, including the switching action, are illustrated in the top portion of figure 3.6.5.

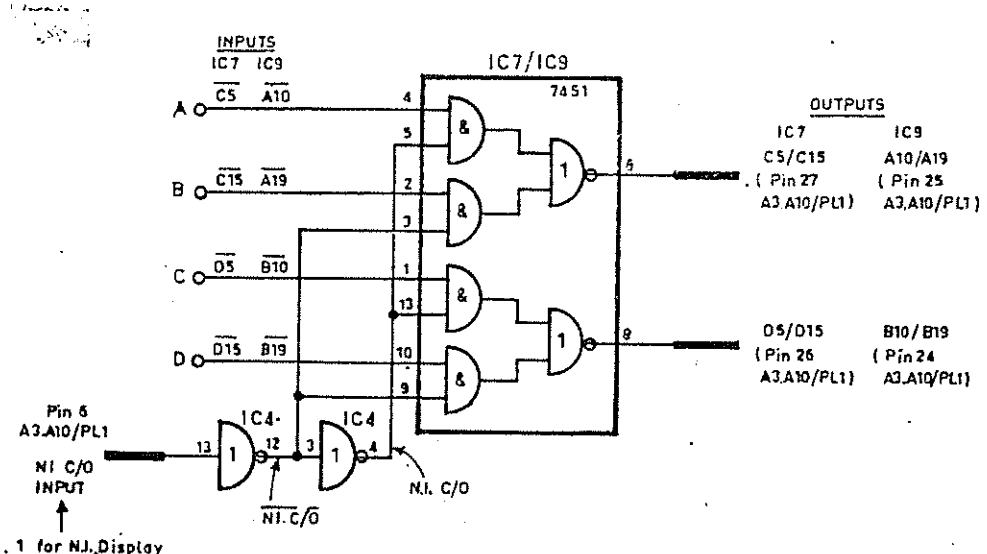
Similarly, IC11 and IC12 on A3A5 switch the four-bit binary input to the horizontal segments input of the Numeral Generator. Their operation is apparent from Fig. 3.6.10. An extra output, from pin 8 of IC12, is required for the upper segments control line of the Numeral Generator. This goes to A3A4 via pin 21 of A3A5/PL1. The lower segments control line is taken from the horizontal segments input lines. As an inverter, from IC13 is interposed between pin 8 of IC12 and pin 22 of A3A5/PL1, these two outputs are complementary-phase pulses. The output waveforms, including the switching action are illustrated in figure 3.6.6 and 3.6.7.



TRUTH TABLE IC2/IC5

N.I. C/O INPUT	IC2 INPUT PINS								IC2 OUTPUTS		IC5 INPUT PINS								IC2 OUTPUT PINS	
	1	2	3	4	5	9	10	13	X	Y	1	2	3	4	5	9	10	13	X	Y
1	3kHz	C10	0	6kHz	1	0	D10	1	6kHz	3kHz	B5	A15	0	A5	1	0	B15	1	A5	B5
0			1		0	1		0	C10	D10			1		0	1		0	A15	B15

FIG. 3. 6. 9. Operation of the 7451 digital switches, IC2 and IC5 on A3.A10.



TRUTH TABLE IC7/IC9

N.I. C/O INPUT	IC7 INPUT PINS								IC7 OUTPUT PINS		IC9 INPUT PINS								IC9 OUTPUT PINS	
	1	2	3	4	5	9	10	13	6	8	1	2	3	4	5	9	10	13	6	8
1	D5	C15	0	C5	1	0	D15	1	C5	D5	B10	A19	0	A10	1	0	B19	1	A10	B10
0			1		0	1		0	C15	D15			1		0	1		0	A19	B19

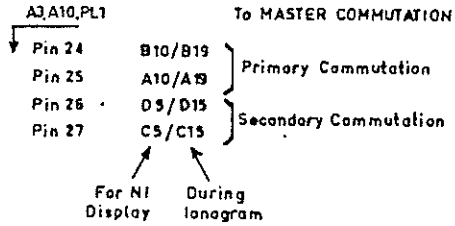
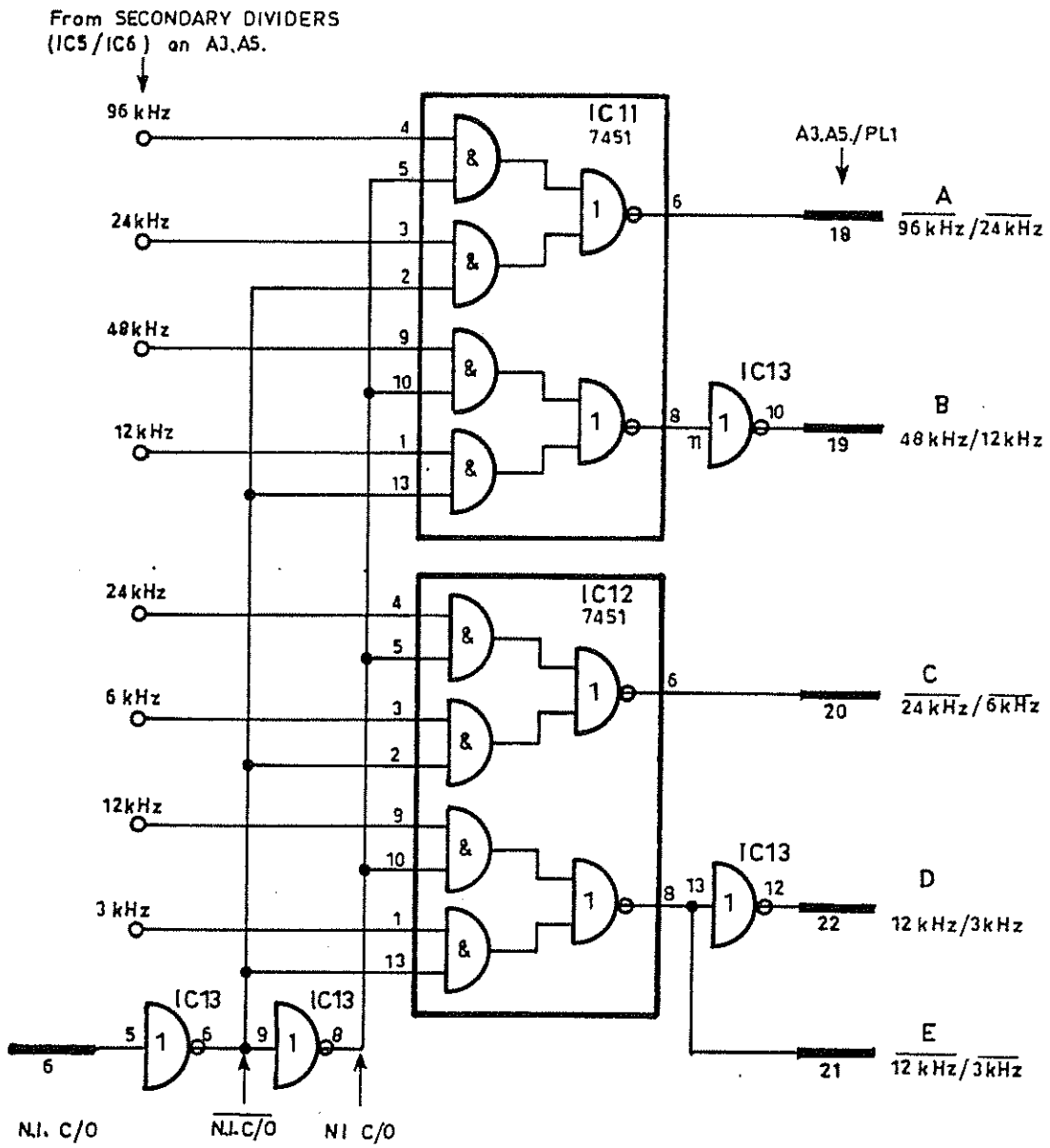


FIG. 3. 6. 8. Operation of the 7451 digital switches, IC7 and IC9 on A3.A10.



TRUTH TABLE IC11 / IC12

During Ionogram For N.I. Display

N.I. C/O INPUT	IC11 INPUTS								IC12 INPUTS								OUTPUTS				
	1	2	3	4	5	9	10	13	1	2	3	4	5	9	10	13	A	B	C	D	E
1	12kHz	0	24kHz	96kHz	1	48kHz	1	0	3kHz	0	6kHz	24kHz	1	12kHz	1	0	$\overline{96kHz}$	48kHz	$\overline{24kHz}$	12kHz	$\overline{12kHz}$
0		1			0		0	1		1			0		0	1	$\overline{24kHz}$	12kHz	$\overline{6kHz}$	3kHz	$\overline{3kHz}$

Horizontal Segments input to Numeral Generator A3.A4.

Lower segments Control line.

Upper segments Control line.

FIG. 3. 6. 10. Operation of the 7451 digital switches, IC11/IC12, located on A3.A5, which are part of the Commutation Generator.

3.6.7 The Master Commutation Circuit, A3A6
(Dwgs: CD-223Y1 and CB-30Y1)

A block diagram of the Master Commutation circuit is given in drawing CB-30Y1 together with the numeral output multiplexing circuitry associated with the Chronometer Dividers. The group of numbers displayed are divided into four 'PARTS', arranged as illustrated in CB-30Y1. Each Part is divided into four 'BLOCKS' of one numeral generation period each (ie. a period of 16 y-sweeps). Each circuit that derives the numbers to be written in each Part is selected in turn. The numeral to be displayed in each block is then gated through the numeral input lines of the Numeral Generator in turn.

The Primary Commutation Generator drives the Part 1, Part 2, Part 3 and Part 4 lines high in sequence. The Part 1 line enables the Station No. Replacement of Seconds commutation circuitry when it goes high. The Parts 2, 3 and 4 lines enable the YEARS, DAYS and HOURS/MINS output multiplexing circuitry respectively, when each goes high.

The Secondary Commutation Generator drives the Blocks 1, 2, 3 and 4 lines high in sequence during each Part, causing a blank or a numeral to be written on the CRT from the outputs of the Station Number and Chronometer output circuits as required.

On A3A6 (drawing CD-223Y1), the Primary Commutation circuit consists of the four AND-gates from IC9, a type 7408, and two inverters from IC8 (a 7404). The input to this circuit is a two-bit binary code from the COMMUTATION GENERATOR (A3A10) via pins 24 and 25 of A3A6/PL1. The Part 1 output is from pin 6 of IC9. The Parts 2,3 and 4 outputs go via pins 15, 14 and 13 respectively of A3A6/PL1 to A3A1, A3A2 and A3A3. The operation of this circuit is apparent from TABLE 4.

	INPUT From A3.A10		PART 1	PART 2	PART 3	PART 4	FUNCTION
A3.A6/PL1→	Pin 25	Pin 24	Pin 6, IC9	Pin 15	Pin 14	Pin 13	
	0	0	1	0	0	0	Enable VAR. N° & SECONDS or VAR. N° & STN. N° output.
	1	0	0	1	0	0	Enable YEARS output.
	0	1	0	0	1	0	Enable DAYS output.
	1	1	0	0	0	1	Enable HOURS & MINUTES output.

TABLE 4. TRUTH TABLE for Primary Commutation circuit of MASTER COMMUTATION A3.A6.

The Secondary Commutation circuit on A3A6 is similar and consists of the four AND-gates from IC7, also a 7408, and two inverters from IC8. The input to this circuit (via pins 26 and 27 of A3A6/PL1) is also a two-bit binary code from A3A10, but it cycles at four times the rate of the Primary Commutation input. The outputs, Blocks 1 to 4, are via pins 18, 19, 20 and 21 of A3A6/PL1 and go to the output multiplexing circuitry of A3A1, A3A2 and A3A3. In addition, the Block 3 and Block 4 outputs go to the Station Number Replacement of Seconds, Secondary Commutation circuit and the Block 1 and Block 2 outputs drive the circuitry on A3A6 which multiplexes the Variable Number and the following blank onto the numeral input lines to the Numeral Generator. The operation of the Secondary Commutation circuit is apparent from Table 5.

The Serial Number Replacement of Seconds, Secondary Commutation circuit consists of two NAND-gates from IC11 (a 7400), three AND-gates from IC10 (a 7408) and one inverter from IC8. Its operation is apparent from TABLE 6. During Blocks 1 and 2 for both the N.I. Display and the Ionogram, the output multiplexing circuit on A3A6 is 'enabled' and the

Variable Number and the following blank are gated in turn into the numeral input lines (pins 2, 3 ,4, 5 of A3A6/PL1) for the Numeral Generator and are then displayed. During Blocks 3 and 4 for the N.I. Display, the seconds (A3A5) output multiplexing circuitry is enabled and the Seconds Tens and Seconds Units gated in turn onto the numeral input lines. When an ionogram is being displayed the multiplexing circuit on A3A6 is enabled during the appropriate portion of each y-sweep during Blocks 3 and 4 and the Station Number is gated onto the numeral input lines and displayed. The outputs of the Station Number Replacement of Seconds Primary Commutation circuit are all low during Parts 2, 3 and 4, suppressing the variable Number, Station Number and Seconds outputs during these Parts.

The Station Number Replacement of Seconds Secondary Commutation circuit consists of four AND-gates from IC6, a 7408. It also involves an inverter from IC8. Its operation is apparent from TABLE 7. The Blocks 3 and 4 outputs of the Secondary Commutation circuit (pins 20 and 21 of A3A6/PL1) provide the basic commutating pulses. These are gated through to the Seconds output multiplexing circuit (via pins 28 and 29 of A3A6/PL1) when the NI c/o line (pin 6, A3A6/PL1) is high or to the Station Number multiplexing circuit when it goes low. During Parts 2, 3 and 4, the variable Number, Station Number and Seconds outputs are gated off as explained previously.

The Variable Number and Station Number multiplexing circuit is similar to the Chronometer dividers output multiplexing circuitry described in section 3.1.16. In this application, the numbers to be presented to the Numeral Generator are fixed and the circuit is 'hard-wired' to produce the required numerals. As mentioned previously, the variable number is not now used. This is followed by a blank in Block 2. The Station Number TENS and UNITS numerals are obtained by bridging the appropriate terminal pairs as indicated in the table on drawing CD-223Y1.

A3.A6/PL1 →

INPUT From A3.A10.		ENABLE BLOCK 1	ENABLE BLOCK 2	ENABLE BLOCK 3	ENABLE BLOCK 4		PART 1		PART 2	PART 3	PART 4
Pin 27	Pin 26	Pin 18	Pin 19	Pin 20	Pin 21		Ionogram	N.I. Display	(YEARS)	(DAYS)	(HRS & MINS)
0	0	1	0	0	0	write :	VAR. N°	VAR. N°	BLANK	100's DAYS	TENS HOURS
1	0	0	1	0	0	write :	BLANK	BLANK	TENS YEARS	TENS DAYS	UNITS HOURS
0	1	0	0	1	0	write :	TENS STN N°	TENS SECS	UNITS YEARS	UNITS DAYS	TENS MINS
1	1	0	0	0	1	write :	UNITS STN N°	UNITSSECS	BLANK	BLANK	UNITS MINS
						N.I. C/O Pulse	0	1			

TABLE 5. TRUTH TABLE for Secondary Commutation circuit of MASTER COMMUTATION A3.A6.

Pins 5 & 10 IC10 PART 1	Pin 26 A3.A6/PL1	Pin 6 A3 A6/PL1 N.I. C/O	Pin 4 IC 8 $\overline{\text{NI C/O}}$	Pins 3 & 4 IC 11	Pin 9 IC10	Pin 8 IC 10	Pins 3 & 4 IC10	Pin 16 A3.A6/PL1	
1	0	1	0	1	1	1	0	0	Blocks 1 & 2 for N.I. Display
1	0	0	1	1	1	1	0	0	Blocks 1 & 2 for Ionogram
1	1	1	0	1	0	0	1	1	Blacks 3 & 4 for N.I. Display
1	1	0	1	0	1	1	0	0	Blocks 3 & 4 for Ionogram
0	X	X	X	X	X	0	X	0	PARTS 2, 3, 4.

↑ Enable VAR N° & STN. N° output multiplexing circuitry

↑ Enable SECONDS output multiplexing circuitry

TABLE 6. TRUTH TABLE. for Station N°. replacement of Seconds, Primary Commutation.

Pin 6 A3.A6/PL1 NI C/O	Pin 4 IC 8 $\overline{\text{NI C/O}}$	Pin 20 A3.A6/PL1 BLOCK 3	Pin 21 A3.A6/PL1 BLOCK 4	Pin 10 IC 8 (NI C/O)	ENABLE TENS STN. N° Pin11/IC6	ENABLE UNITS STN. N° Pin3/IC6	ENABLE TENS SECONDS Pin 28	ENABLE UNITS SECONDS Pin 29	
1	0	1	0	1	0	0	1	0	Part 1, Block 3 of NI Display
1	0	0	1	1	0	0	0	1	Part 1, Block 4 of NI Display
0	1	1	0	0	1	0	0	0	Part 1, Block 3 of Ionogram N°s.
0	1	0	1	0	0	1	0	0	Part 1 Block 4 of Ionogram N°s

TABLE 7. TRUTH TABLE. for Station N° replacement of Seconds, Secondary Commutation.

3.7
CONTROL SYSTEM

Par. No.	Title	Drawing No.
3.7.1	Brief Summary	
3.7.2	Description of the Control Circuitry in the Program unit A5A1	CD-228X1 (A5A1)
3.7.3	Programmed Soundings	" " "
3.7.4	Single Soundings	" " "
3.7.5	Camera Drive Control	" " "
3.7.6	Numeral Indication Display Control	" " "
3.7.7	A-Scan Display Control	" " "
3.7.8	The Control Logic A3A8	CB-31Y1A
3.7.9	Video Control Logic	CD-250Y1 (A3A8)
3.7.10	Numeral Indicator Control Logic	" " "
		CD-249Y1 (A3A10)
3.7.11	The Transmitter Control Logic	CD-250Y1 (A3A8)
3.7.12	The X-Blank Generator	" " "
3.7.13	Control of the Transmitter Power Supply Drive, Transmit Pulse Gate and Transmit Fail Warning Logic	" " "
3.7.14	The Transmitter Power Supply Drive Circuit	" " "
3.7.15	The Transmit Pulse Gate	" " "
3.7.16	The Transmit Fail Warning Circuitry	" " "
3.7.17	Ancilliary Circuitry	
3.7.18	The X-NI Reset Circuit	CD-249Y1 (A3A10)
3.7.19	The Y-NI Reset Circuit	CD-227Y1 (A3A5)
3.7.20	Set-up Z-modulation Circuit	CD-229Y1 (A3A12)
		CD-227Y1 (A3A5)

3.7.1 Brief Summary

The Control System of the ionosonde commences with the two function switches located on the front panel of the PROGRAM unit A5. All operation modes of the ionosonde are selected from these switches. When a particular display or sounding program is selected, the Control System initiates the circuit functions required to produce that display.

There are seven functions that can be selected for the MAIN Display A8. These are:-

1. SET-UP - a 5 x 7 dot matrix for setting the CRT trace alignment, brightness, focus etc.
2. PRESET - this initiates the PRESET PROGRAM A3A9, an optional unit which can provide additional programmed soundings separately from the routine soundings.
3. SINGLE - this allows a single ionogram to be initiated by pushing the button above the function switch.
4. 15 MIN - a sounding is recorded on film every 15 minutes. This is the normal program for routine soundings
5. 5 MIN - a sounding is recorded every five minutes.
6. 1 MIN - a sounding is recorded once per minute.
7. CONT. - 'continuous' sounding. Three ionograms are recorded every minute.

A further two functions can be selected for the MONITOR Display in addition to the above seven functions, these being:-

1. N.I. - 'Numeral Indication'. The date, time and preset number are displayed.
2. A SCAN - A range-amplitude display is produced when one of the sounding modes is initiated for the MAIN display.

The Constrol System circuitry is predominantly confined to two assemblies, the PROGRAM unit A5A1 and the CONTROL LOGIC A3A8. Ancilliary circuitry is located on A3A5, A3A10 and A3A12.

Digital TTL ICs are used throughout the control circuitry.

When the PRESET program is selected, S1D grounds pin 12 of IC3 and pin 4 of IC7, one NAND gate from IC1. The output of this NAND gate, pin 6, then goes high, enabling the PRESET PROGRAM unit A3A9. The output of this unit drives one input of a NOR gate from IC3 (pin 11) via pin 7, A5A1/PL1. This output is normally high, going low for 20 seconds at the preset time selected by the operator. The Main Display Control Line will then go low in the same way as for the other programs.

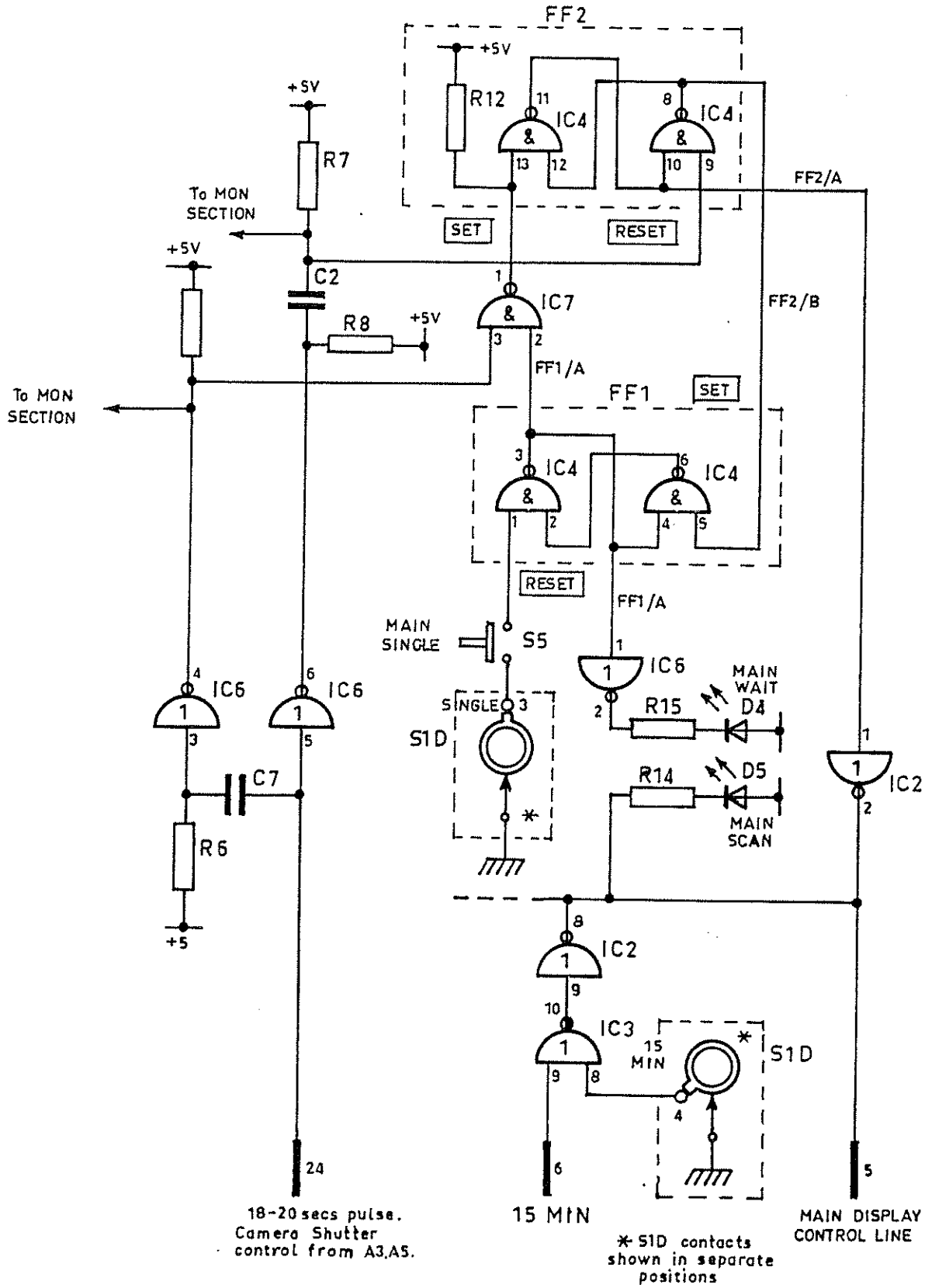


FIG. 3. 7. 1. Portion of Main Display control circuitry on A5.A1.

3.7.2 Description of Control Circuitry in the Program unit A5A1 (Dwg: CD-228X1)

This consists of the function switches S1 and S2, two groups of NOR gates and inverters (IC3, IC2 and IC11, IC10), associated with the routine programming for the Main and Monitor displays, two pairs of flip-flops involving NAND gates (IC4, IC8 and part of IC7) - these being associated with the SINGLE function, and a number of inverters and NAND gates that control the operation of the camera (IC1, IC6 and IC7).

To initiate a sounding, the MAIN DISPLAY CONTROL LINE (pin 5, A5A1/PL1) and the MONITOR DISPLAY CONTROL LINE (pin 30, A5A1/PL1) must be held LOW. this enables the control logic on A3A8.

There are four LED indicators on the front panel, two each for the Main and Monitor displays. Each pair is labelled WAIT and SCAN. The SCAN indicator lights during a sounding. The WAIT indicator lights prior to a sounding initiated from the SINGLE push button (S3 or S5), and extinguishes when the sounding commences.

Each function switch has four sections. The first three sections of each (A, B, C), switch the X-deflection, Y-deflection and Z-modulation signals to the displays A8 and A10. The fourth section on each switch enables portions of the control circuitry which initiate the various functions. Block diagrams of the function switch operations are given in CB-33Y1 (S1) and CB-32Y1 (S2).

3.7.3 Programmed Soundings

This description will be concerned with the Main Display control circuitry on A5A1, the relevant portions of which are shown in fig. 3.7.1. The Monitor Display control circuitry is similar, except for the first two functions which will be described later.

When S1 is selected to provide 15 minute soundings, S1D grounds pin 8 of IC3, one input to a two input NOR gate. The other input, pin 9, is driven by the 15 MIN output of the Program Decoding circuitry from the Minutes Dividers (A3A7) of the Chronometer section of the Clock (see 3.1.19) via pin 6, A5A1/PL1. This input is normally high, going low for the first 20 seconds of minutes 0, 15, 30 and 45 of each hour. When pin 9 of IC3 goes low, the output of the NOR gate, pin 10, goes high. This drives an open-collector output inverter from IC2, a 7406, the output of which (pin 8) drives the MAIN DISPLAY CONTROL LINE. This goes low causing the MAIN SCAN indicator to light and enabling the CONTROL LOGIC on A3A8. At second 20, pin 9 of IC3 goes high again and the Main Display Control Line High, disabling the Control Logic. The process is illustrated in fig. 3.7.2.

The X-MAIN Timebase and the Y-MAIN Timebase outputs are switched through to the display (A8) via S1A and S1B and pins 22 and 26 of A5A1. Unblanking pulses from the Control Logic are switched through to the display via S1C.

The control circuitry works in a similar manner when the 5 MIN and 1 MIN programs are selected. When the CONTINUOUS program is selected, S1D grounds the Main Display Control Line. The Operational Dividers on A3A11 then time the cycle of operations for each sounding. As these are reset every twenty seconds there are three soundings per minute.

(or 0), the negative-going edge of the '18-20 sec' pulse, pin 3 of IC6 will be momentarily grounded (low) until C1 charges again via R6. Thus, a short, positive-going pulse appears on pin 4 of IC6 and pin 3 of IC7. As pin 2 of IC7 is held high by FF1a, pin 1 of IC7 (and thus the FF2 SET input) will go low momentarily, resetting FF2. Both outputs of FF2 then change state.

FF2a latches high, driving the Main Display Control Line low, enabling the Control Logic on A3A8. The MAIN SCAN indicator then lights.

FF2b latches low, resetting FF1. Thus, at the instant FF2 is reset FF1a latches low again and the MAIN WAIT light goes out.

The Main Scan indicator remains on from second 0 to second 18. At second 18 pin 6 of IC6 goes low. This negative-going edge then resets FF2, the two outputs reverting to their original states; FF2a low, FF2b high. The control logic is then disabled and FF1 set to its initial condition.

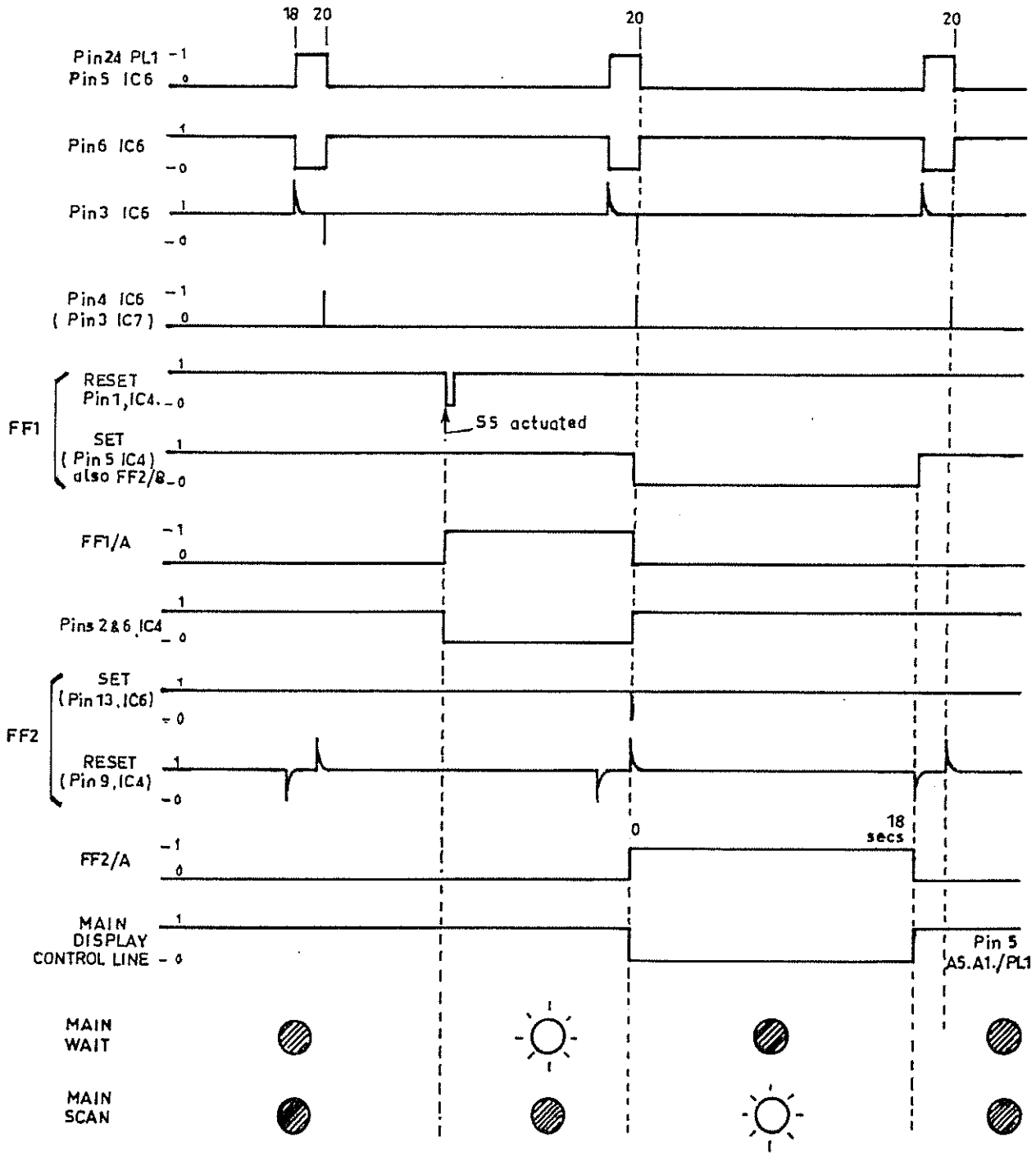


FIG. 3.7.3. Control Circuit Operation for Single sounding (refer A5.A1.)

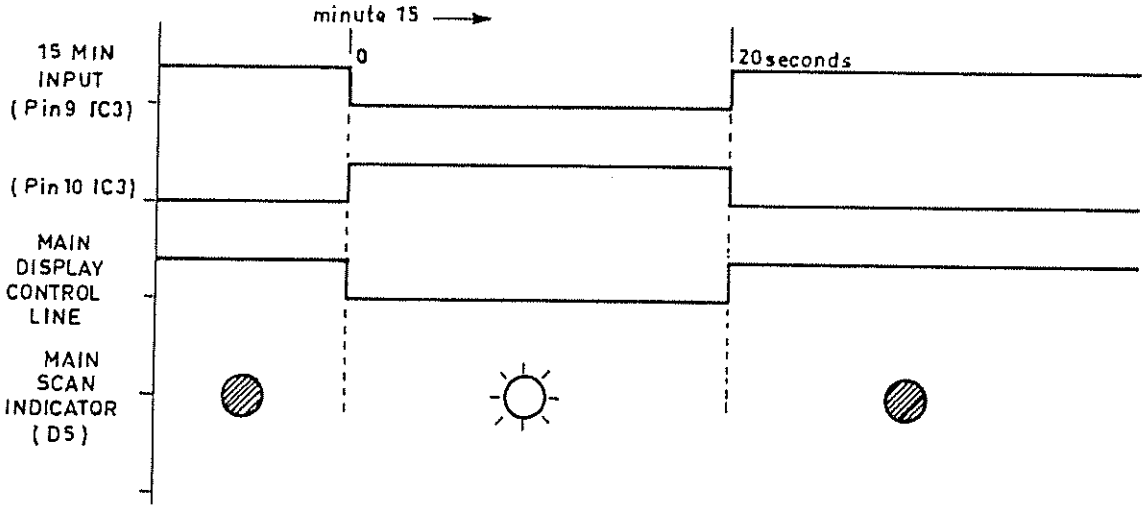


FIG. 3.7.2. Control Circuitry operation during 15 minute program.

3.7.4 Single Soundings

This description will also be confined to the Main Display control circuitry on A5A1. That for the Monitor Display is similar. Refer to fig. 3.7.1 for the relevant portion of the circuit.

When the SINGLE function is selected, S1D grounds one contact of the pushbutton S5. To initiate a single sounding, S5 is momentarily actuated.

The control circuit for this function involves two set-reset (S-R) flip-flops, FF1 and FF2, using NAND gates (IC4). The SET and RESET inputs of FF1 are normally high, the output (FF1a) is thus normally low. The MAIN WAIT indicator, D4, indicates the state of FF1a. It is driven from FF1a by an inverter from IC6.

IC6 is a type 7406 hex inverter with open-collector outputs. IC7 is a type 7401 quad NAND gate with open-collector outputs.

The SET input to FF2 is driven by the output of one NAND gate from IC7. One input to this gate is FF1a, which is normally low. The other input is driven by the output of an inverter from IC6 (pin 4). This is normally low as the inverter input, pin 3, is normally high, pulled-up by R6. If either pin 2 or pin 3 of IC7 is low, the output of this gate will be high, and thus the SET input of FF2 is high, pulled up by R12 as IC7 has open collector outputs.

The RESET input of FF2 is high, pulled up by R7. Pin 5 of IC6 is normally low, going high during second 18 to second 20 of each 20 seconds. Pin 6 of IC6 is thus normally high, pulled up by R8, and C2 is discharged as both sides are at the same potential.

FF2a is thus normally low and FF2b normally high.

When S5 is actuated, the RESET input of FF1 goes low, FF1a latches high and the MAIN WAIT indicator lights. Pin 2 of IC7 is thus held high. On the positive-going edge of the '18-20 secs' pulse, at second 18, C1 will discharge rapidly via R6 as both sides are then at the same potential. Pin 6 of IC6 will go low from 18 to 20 seconds. At second 20

3.7.5 CAMERA DRIVE CONTROL

The circuitry on A5A1 relating to the camera motor drive is shown on Fig. 3.7.4. The camera motor drive circuitry is explained in section 3.9.

The camera drive waveform (see Figure 3.7.4) is obtained from A3A5 and enters via pin 24 on A5A1/SK1. The waveform is inverted at pin 6 of IC6 and is routed through to the camera (when pin 13 of IC1 is high), inverted again at pin 11 of IC1. The MAIN DISPLAY CONTROL LINE is high prior to a scan or sounding. At the commencement of a scan, the MAIN DISPLAY CONTROL LINE goes low which turns on the MAIN SCAN, L.E.D., D5. Hence the output of IC2, pin 12 originally low, is pulled high by R11.

The input of the main gate, pin 13 of IC1, therefore goes high and consequently allows the camera drive waveform from A3A5, through to the camera via the white lead of the connecting cable.

The camera motor will then turn and the shutter will either open or close depending upon whether the next due cycle is an 'open' or 'close' cycle. Normally, at the commencement of a scan period, the MAIN DISPLAY CONTROL LINE goes low simultaneously with the camera drive waveform and therefore opens the camera shutter. The film advances each time the motor is activated.

Prior to a sounding, the MAIN DISPLAY CONTROL LINE is high and pin 13 of IC1, one input of a NAND gate, is held low by the output of an inverter from IC2 (pin 12). This forces the output, pin 11 of IC1 high regardless of the level on the other input, pin 12. Under these circumstances the camera shutter is closed.

The camera drive and gating waveforms are shown on Fig. 3.7.5.

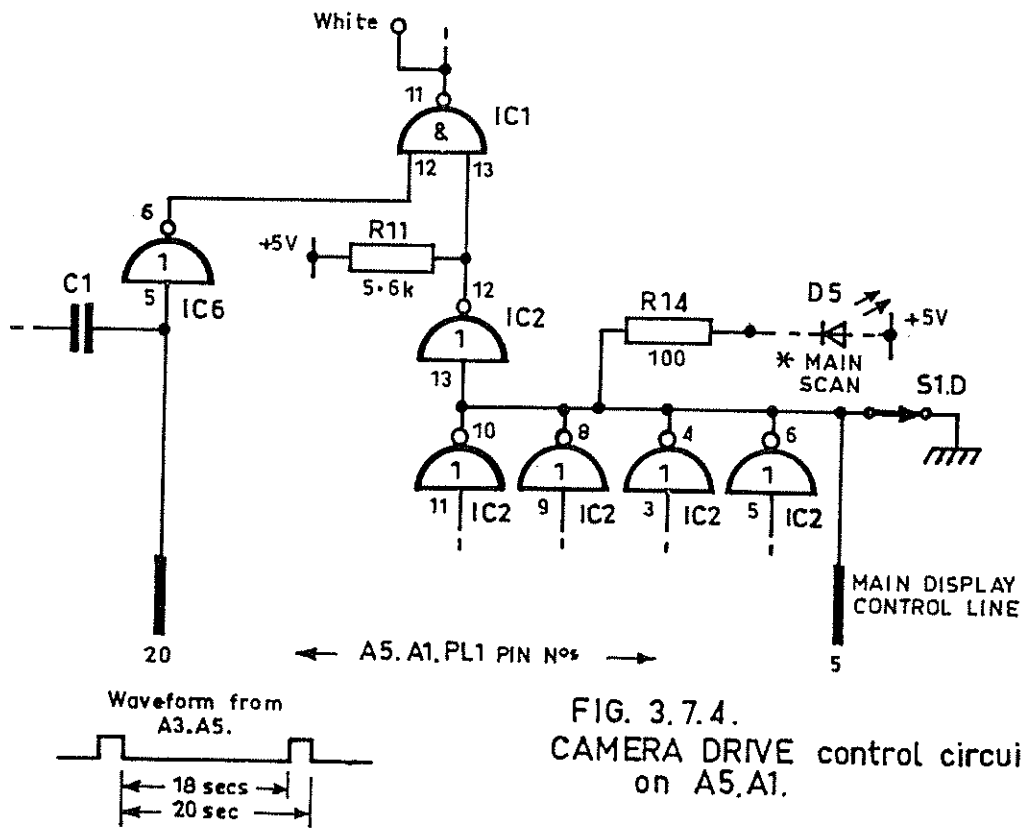


FIG. 3.7.4.
CAMERA DRIVE control circuitry on A5.A1.

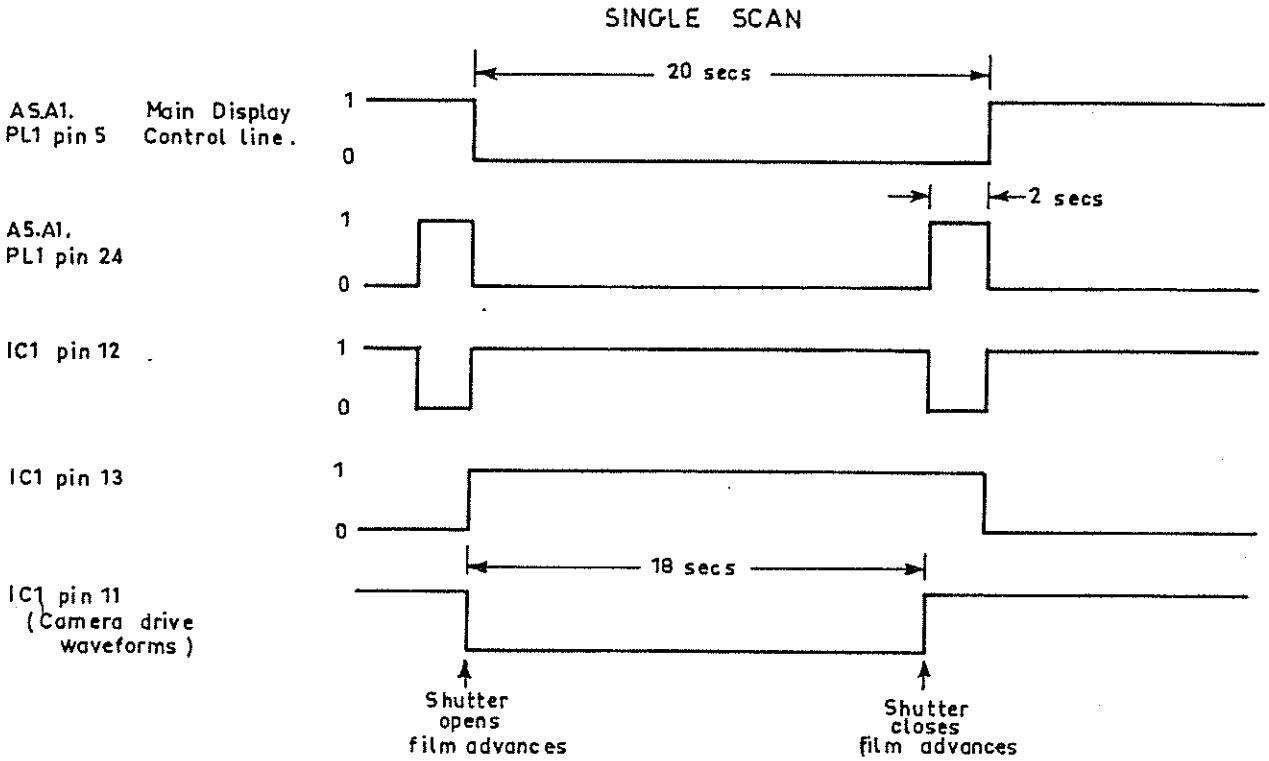


FIG. 3.7.5. Single scan control circuit operation for Camera Motor Drive.

3.7.6 Numeral Indication Display Control

When the Numeral Indication (N.I.) display is selected on the function switch, S2, the X-N.I. and Y-N.I. time base outputs are switched through to A10 via S2A and S2B. The numeral brightening pulses from the Numeral Generator, A3A4, are routed through the Control Logic, and are switched to the monitor (A10) via S2C.

3.7.7 A-Scan Display Control

The A-Scan Display is also selected on the Monitor function switch, S2. The X-A Scan timebase output is switched through to A10 via S2A. The A-Scan output of the Receiver (from A7A8) is switched through to the Monitor Y deflection via S2B. The unblanking pulse from pin 2 of IC10 is routed via S2C.

When the A Scan function is selected, the Frequency Synthesizer, A4, can be set to operate in the Single Frequency mode. S2D grounds pin 13 of A5A1/PL1 and A4A1/PL1. When S11 on the front panel of A4 is set to SF (i.e.: Single Frequency) the ten bit binary input controlling the scan is disabled enabling the synthesizer frequency to be set by the front panel switches.

3.7.8 The Control Logic A3A8.
(Dwg: CD-250Y1)

The primary functions of the Control Logic are to add and route the video blanking and brightening pulses for the main and monitor displays, generate the Numerical Indicator Changeover (N.I. c/o) pulse and control the Transmitter operation.

There are three sections to the Control Logic,

(a) Video control

(b) Numeral Indicator Control

(c) Transmitter Control.

All the circuitry is located on A3A8 and involves ten TTL digital ICs. All control functions and input and output signals are thus at TTL logic levels. In addition to its primary functions the Control Logic provides the X-Main Timebase reset pulse.

An overall block diagram is given in drawing CB-31Y1A.

3.7.9 Video Control Logic (on A3A8)
(Dwg: CD-250Y1)

With reference to the block diagram, this section is comprised of six gates. Three gates serially add the received echoes, the graticule brightening pulses, the numeral brightening pulses, the Y-blank and the X-blank pulses. These are then routed through to the MAIN and MONITOR displays via two gates which are controlled by the Main or Monitor Control Lines from A5A1. When the control line is low, the video pulses are gated through to the appropriate display Z-mod. input, the gates invert the pulses in doing so. The PROGRAM CONTROL GATE drives the PROGRAM CONTROL LINE. This line goes high when either the Main or Monitor Control Lines are low, initiating the Transmitter Control logic which gates the appropriate drive signals to the transmitter, turning it on. This line also controls the operation of the Numeral Indicator Control logic.

Referring to the circuit, CD-250Y1, one three-input NAND gate from IC4 (pins 8, 9, 10, 11) is the 'ADD VIDEO, GRATICULE & N.I.' gate. One AND gate from IC7 (pins 4, 5, 6) is the Y-BLANK gate and one NAND-gate from IC9 is the X-BLANK gate. The output of this gate (pin 3, IC9) drives one input of each of the MAIN CRT CONTROL gate and MONITOR CRT CONTROL gate. The MAIN CONTROL LINE (pin 5 A3A8/PL1) and the MONITOR CONTROL LINE (Pin 30 A3A8/PL1) drive the other inputs. Both of these gates are NOR-gates from

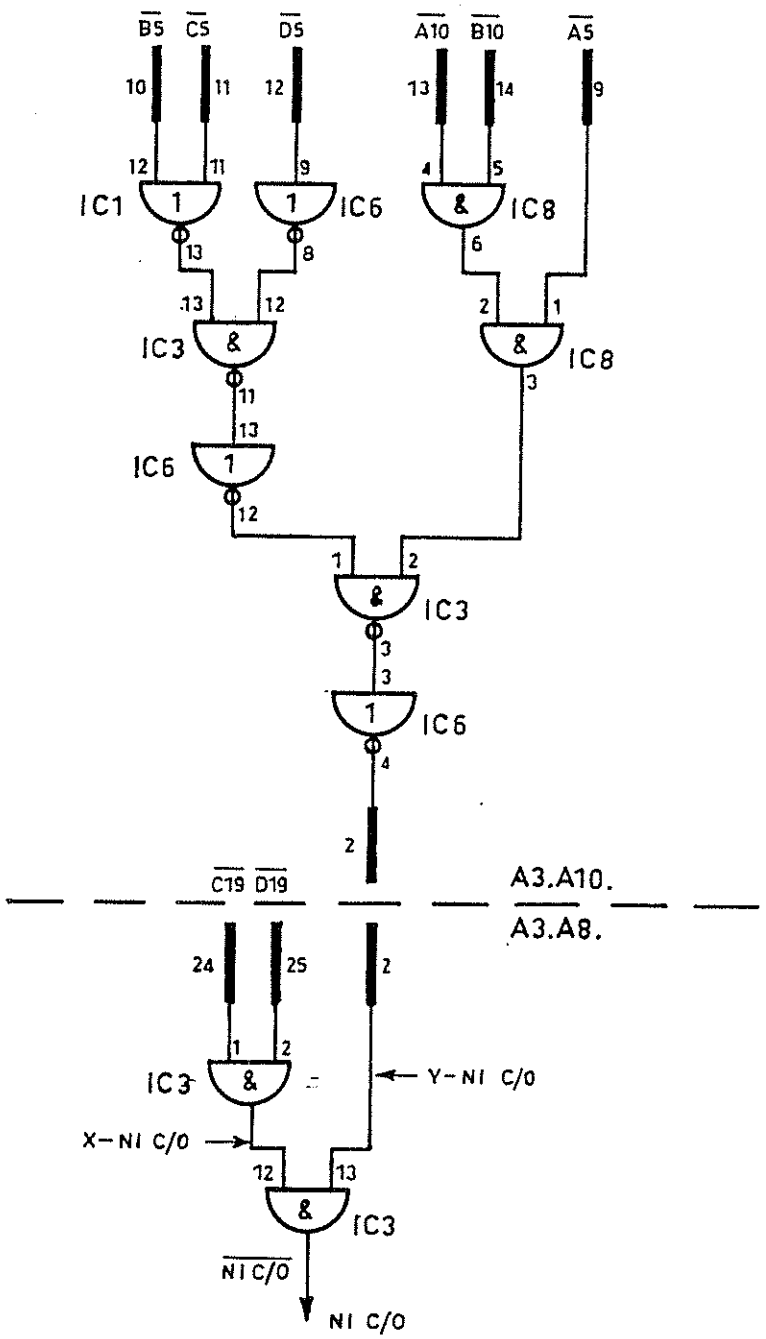


FIG. 3. 7. 6. Circuit deriving N.I. c/o pulse.

IC6, their outputs (pin 10 - MAIN, pin 13 - MON.) return to the function switches on A5A1 before being routed to the Z-mod inputs of A8 (MAIN) and A10 (MONITOR).

The PROGRAM CONTROL GATE IS a NAND-gate from IC8 (pins 1, 2, 3). The output (pin 3) drives the PROGRAM CONTROL LINE. When both the main and monitor Control Lines are high, as they are when an ionogram is not programmed, the Program Control Line is low. If either, or both, control lines go low, (i.e. for a single sounding or programmed sounding), then the Program Control Line will go high.

3.7.10 Numeral Indicator Control Logic (Dwgs: CD-249Y1, CD-250Y1 and CB-31Y1A).

From the block diagram, this consists of three blocks; the NI CHANGEOVER GENERATOR (NI c/o) the NI CHANGEOVER GATE and the NI CONTROL. The NI c/o Generator derives the NI c/o Pulse. The purpose of this pulse is twofold. Firstly, it functions as a blanking pulse on the ionogram display, preventing echoes from being superimposed on the date/time numerals. Secondly, it is a control signal for the numeral commutation, altering the rate of commutation when the date/time numerals are to be displayed on the ionogram.

The NI c/o Pulse is routed to the commutation circuitry via the NI c/o Gate, controlled by the level on the Program Control Line. The NI c/o Gate output also drives the NI Control circuit. This routes the numeral brightening pulses to the video control section and provides an output for the Monitor Display during soundings if the Monitor is programmed to present the NI display.

The Numeral Indicator Control circuitry on A3A8 involves IC2, IC3, IC4, IC5 and IC8.

The NI c/o Generator circuit is actually spread across two boards, part is on A3A10, the other part on A3A8. The complete circuit deriving the NI c/o Pulse is given in figure 3.7.6. The Operational Dividers provide eight inputs to the circuit. There are two parts to the NI c/o Pulse; the X-NI c/o pulse and the Y-NI c/o pulse. The first is a pulse of 5.4612 seconds duration at the commencement of each 20 second program cycle. This is 256 lines wide from left to right, on the ionogram. It is generated by one gate from IC3, a quad two-input AND-gate, on A3A8. The Y-NI c/o pulse is generated by the circuitry on A3A10. This generates 256 pulses that blank the ionogram between 700 and 750 km on each of the first 256 lines. Ultimately, these pulses also operate a group of digital switches in the commutation circuitry which determine which numeral is selected and in what sequence (see Section 3.6). The pulse diagrams illustrating the operation of the NI c/o Generator are given in figure 3.7.7.

The output of the NI c/o Generator, pin 11 of IC3 on A3A8, is designated $\overline{\text{NI c/o}}$ and is one input to a three-input NAND-gate from IC4, the NI c/o gate. The output of this gate (pin 12 IC4) drives the NI c/o Line (see CD-250Y1). Of the two other inputs, one is driven by the Program Control Line, the third input being tied to the +5V supply (logical 1).

When either display unit is programmed for a sounding, the program control line goes high. The NI c/o gate then acts as an inverter and the NI c/o pulse will appear on the NI c/o line.

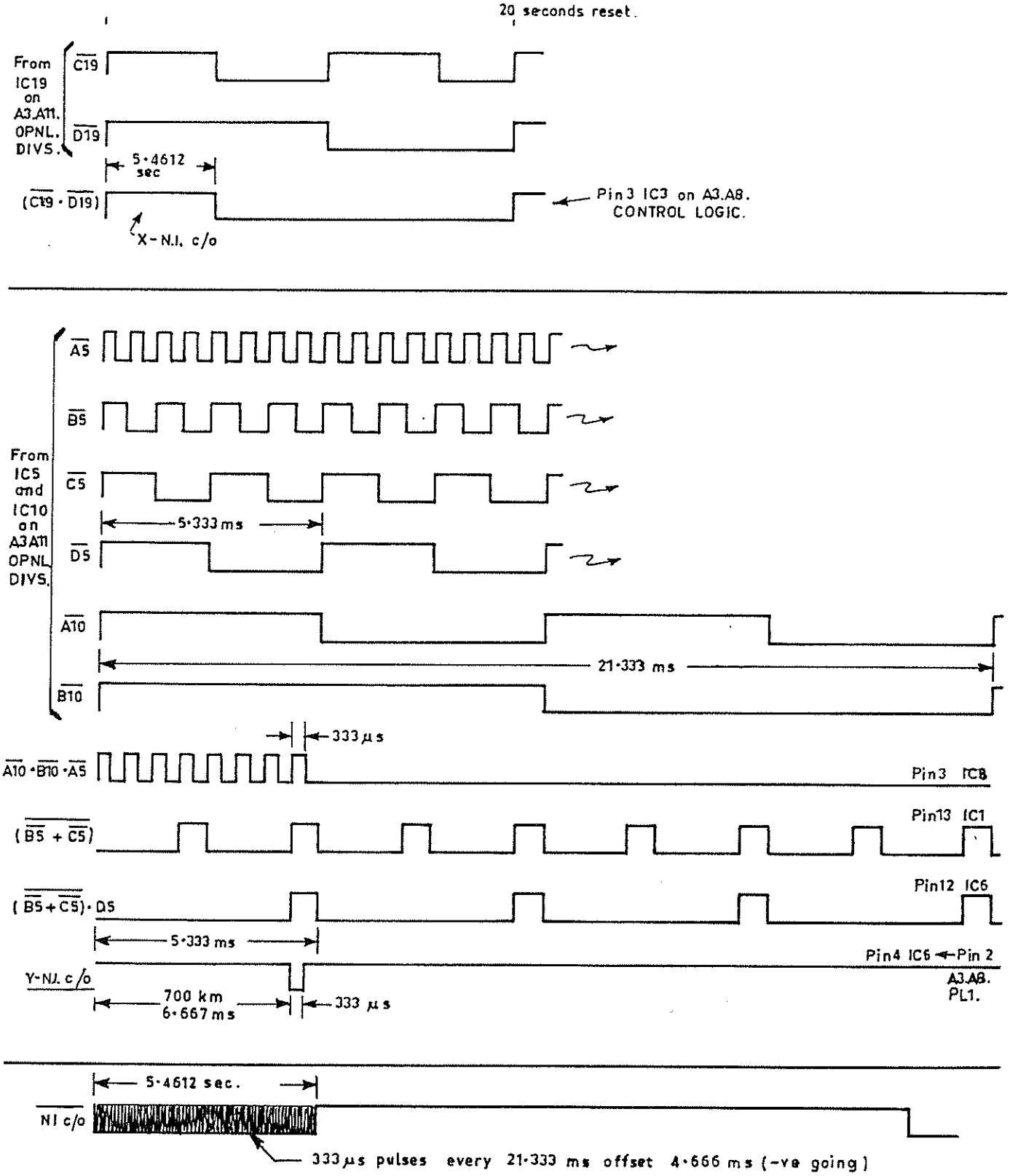
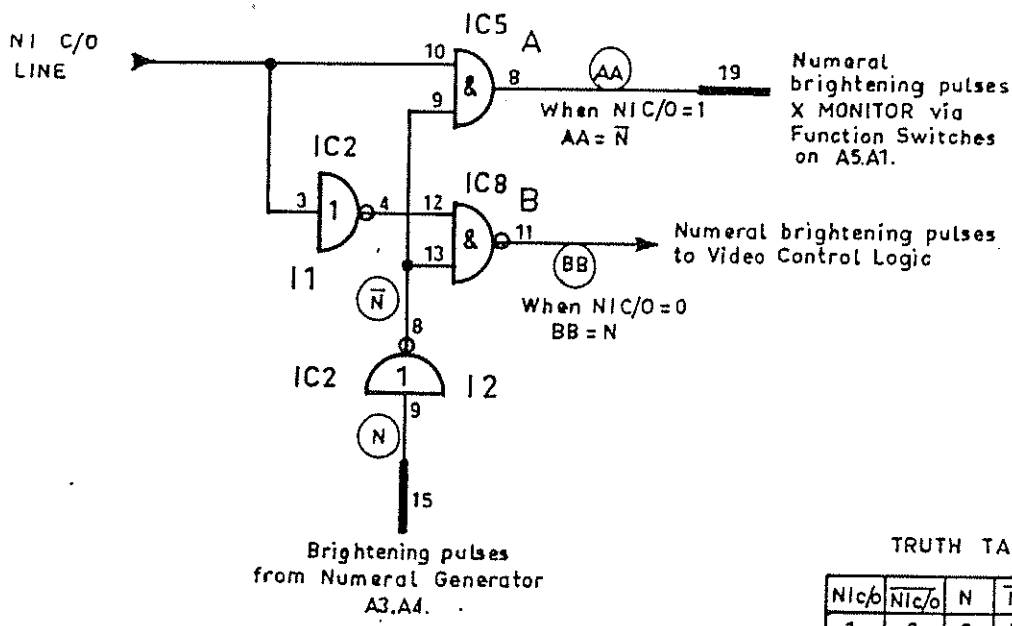


FIG. 3.7.7. Derivation of N.I. c/o pulse.

The NI Control circuit is given in figure 3.7.8. This consists of an AND gate (A), a NAND-gate (B) and two inverters I1 and I2. There are two inputs to the circuit: the NI c/o Line and the output of the Numeral Generator.

The NI c/o pulse and the inverted output of the Numeral Generator ($\overline{N}$) go to the inputs of gate A. When the NI c/o line is high, $\overline{N}$ appears at the output of A (AA). This goes to the Monitor Display (A10) Z-mod. input via the function switches on A5A1.



TRUTH TABLE

NIc/o	N̄Ic/o	N	N̄	AA	BB
1	0	0	1	1	1
0	1	1	0	0	1
0	1	0	1	0	0

FIG. 3.7.8. N.I. Control circuit.

The Z-modulation circuitry of the Main and Monitor Displays require positive-going logic pulses to brighten the CRT trace. As the output pulses of the Numeral Generator (N in fig. 3.7.8) are negative going, they need to be inverted to provide correct polarity pulses to the Z-mod. inputs of the two display units. Thus $\bar{N}$ appears on pin 19 of A3A8/PL1 when the NI c/o Line is high.

When the NI c/o Line is low, the output of I1 will be high, thus causing gate B to invert whatever is on its other input. As $\bar{N}$ is on this input, N will appear at BB when the NI c/o line is low. Pin 11 of IC8 drives one input of the 'Add Video, Graticule and NI' gate (pin 9, IC4). Referring to drawing CD-250Y1, $\bar{N}$ will appear at pin 8 of IC4, the output of the 'Add Video, Graticule and NI' gate. It will also appear at the output of the Y-Blank gate (pin 6, IC7). The X-Blank gate will invert the output of the Y-Blank gate during non-blanking periods and thus N will appear on the output (pin 3, IC9). The Main and Monitor CRT gates will invert the output of the X-Blank gate at their outputs (pins 10 and 13 of IC6 respectively) and thus $\bar{N}$, which is the correct polarity numeral brightening pulses, will be routed to the main or Monitor Z-mod. inputs when a programmed sounding occurs.

3.7.11 The Transmitter Control Logic
(Dwgs: CB-31Y1A, CD-250Y1)

The functions of this section of the Control Logic are as follows:-

(a) To gate on and off the 6 kHz drive to the transmitter power supply

(b) To gate on and off the Transmit Pulses to the transmitter

(c) To initiate the Transmit Fail Warning Logic during a sounding.

With reference to the block diagram, in drawing CB-31Y1A, those blocks primarily controlling the transmitter operation are the 'X-Blank Generator', the 'Tx Pulse Control' and the 'A-Scan Control'. The X-Blank Generator derives a pulse of 12.309 seconds duration which appears on the X-Blank Line. This pulse allows the Transmit Pulses from A3A11 to be routed to the transmitter during a sounding. In addition, it provides an unblanking pulse for the Displays during the X-period of the ionogram sweep, and also provides the X-MAIN Timebase reset pulse.

The A-Scan Control allows the Transmitter to be turned on for a single-frequency A-scan sounding, which is displayed on the Monitor CRT, between normal programs. During normal soundings it allows the Program Control Line to turn on and off the 6 kHz transmitter power supply drive and, via several other gates, the transmit pulses.

The Transmit Pulse Control gate controls the 'Tx Pulse' gate via the 'Frequency Synthesizer Override' gate. During normal soundings, the transmit pulses from A3A11 are routed to the Transmitter for the duration of the X-Blank pulse (12.309 sec). When a single frequency A-scan is selected, the Frequ. Synth. Override gate enables the Tx Pulse gate and the transmit pulses are routed through to the transmitter.

The circuit description will commence with the derivation of the X-Blank pulse.

3.7.12 The X-Blank Generator (Dwg: CD-250Y1)

This circuit consists of two four-input NAND-gates (IC10) and an inverter from IC2. It has five inputs, four derived from the Operational Dividers' outputs ($\overline{A19}$, $\overline{B19}$, $\overline{C19}$, $\overline{D19}$) which enter A3A8 via pins 22, 23, 24, 25 of A3A8/PL1, and 'Line 5' from the Graticule Generator on A3A11, which

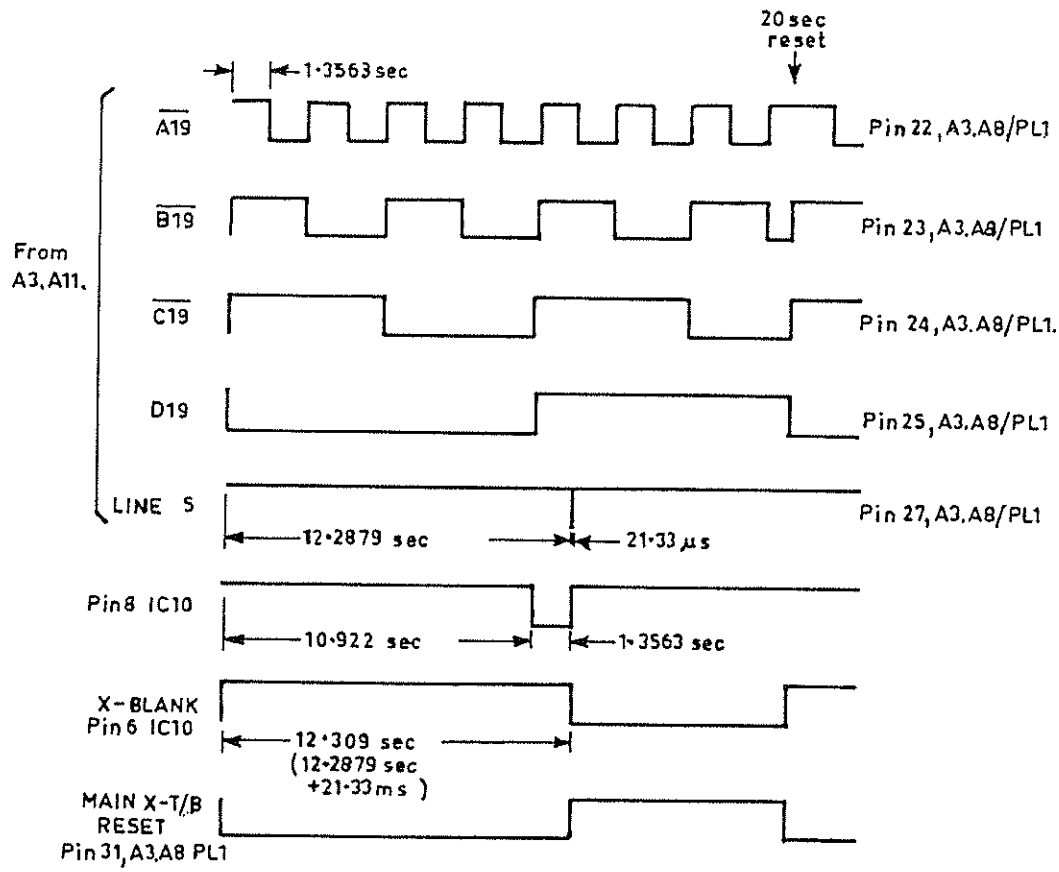


FIG. 3. 7. 9. Derivation of the X-BLANK pulse.

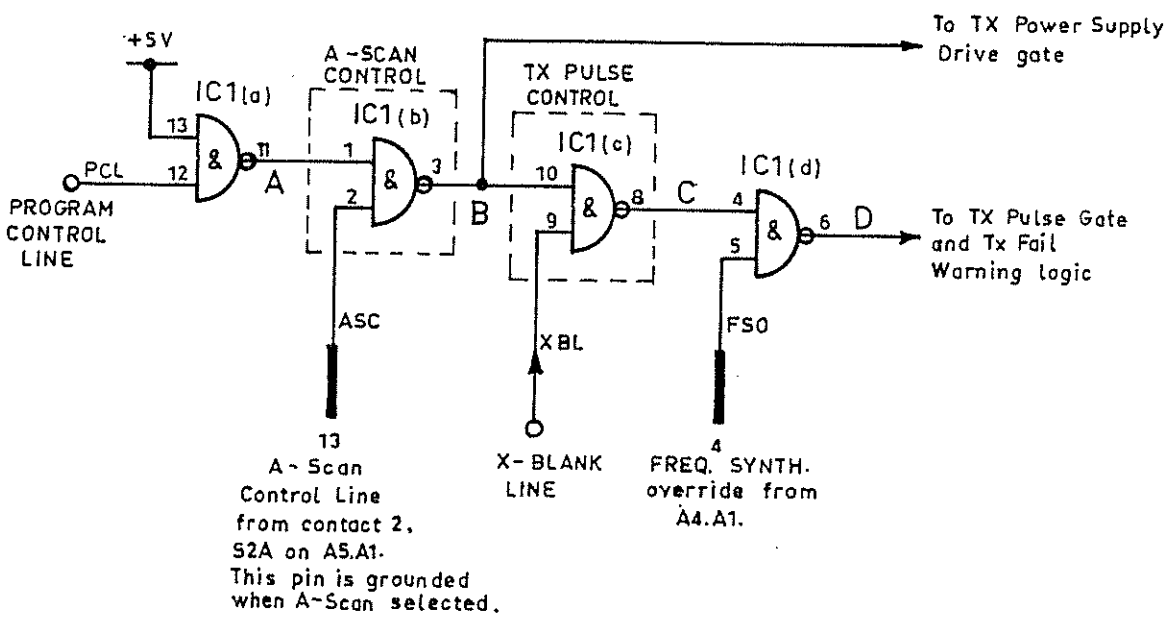
enters via pin 27 of A3A8/PL1. Two inputs, pins 24 and 25 ($\overline{C19}$, $\overline{D19}$), are shared by the NI changeover Generator from the Numeral Indicator control circuitry.

The pulse diagrams illustrating the derivation of the X-Blank pulse are shown in figure 3.7.9.

The output of the X-Blank Generator, pin 6 of IC10, drives the X-Blank Line. This goes high at the commencement of each 20 seconds and low 12.309 seconds later. An inverter from IC2, driven from the X-Blank Line, provides the X-Main Timebase reset pulse via pin 31 of A3A8/PL1.

3.7.13 Control of the Transmitter Power Supply Drive, Transmit Pulse Gate and Transmit Fail Warning Logic
(Dwg: CD-250Y1)

This is accomplished by four gates from IC1, a type 7400 quad two-input NAND-gate. This portion of the Control Logic circuit is shown in figure 3.7.10. The output of IC1 (b), B, goes high to gate the transmitter power supply drive on. Similarly, the output of IC1 (d), D, which controls both the Tx Pulse Gate and the Tx Fail Warning Logic, goes high to enable these circuits.



TRUTH TABLE

PCL	XBL	A	ASC	B	C	FSO	D	COMMENTS
0	X	1	1	0	1	1	0	Between programs
1	1	0	1	1	0	1	1	During a sounding (0-12·3 sec) Tx pulse & Tx Power Supply on.
1	0	0	1	1	1	1	0	End of sounding (12·3 to 20 sec)
1	1	0	0	1	0	1	1	A-scan, single frequency sounding, Monitor display only.
1	1	0	0	1	0	0	1	A-scan on monitor display during ordinary swept frequency sounding.

FIG. 3. 7. 10. Portion of the Control Logic controlling the Transmitter Power Supply drive, the Transmit Pulse gate and the Tx Fail Warning Logic.

The Program Control Line (PCL) is normally low between soundings, going high when a sounding is initiated. IC1 (a) is connected as an inverter. Thus, A will be high between soundings. Assuming the A-Scan function is not selected, pin 13 of A3A8/PL1 (ASC) will be open circuit, allowing pin 2 of IC1 (b) to float high. Thus the output of IC1 (b), B, will be low. This forces the output of IC1 (c), C, high regardless of the condition of the X-Blank Line (XBL). Pin 4 of A3A8/PL1 (FSO) is normally high, going low only when a single frequency sounding is selected from the Frequency Synthesizer. Thus, the output of IC1 (d), D, will be low between soundings.

When a programmed sounding or a single sounding is initiated, both the Program Control Line and the X-Blank Line will go high at the commencement of the 20 second sounding period. Now, if an A-Scan has not been selected for the Monitor, pin 2 of IC1 (b) will be high. When A goes low, B will go high. The X-Blank Line goes high for the first 12.309 seconds of the 20 second sounding period and thus C will go low for the duration of the X-Blank pulse. As pin 4 of A3A8/PL1 is high during a programmed sounding, D will go high for the duration of the X-Blank Pulse.

Thus the transmitter power supply will be operative for the full 20 seconds of a program cycle while the transmitter itself will only be pulsed for the duration of the X-scan, 12.309 seconds.

If the A-Scan function is selected, contact 2 of S2A on A5A1 will ground pin 2 of IC1 (b) via pin 13 of A3A8/PL1. This will cause B to go high, gating on the transmitter power supply drive. When the X-Blank Line goes high, C will go low and D will go high, gating the transmit pulse to the transmitter and enabling the Transmit Fail Warning Logic. However, an A-scan will only be displayed when the Monitor Control Line goes low which will occur when a programmed sounding or a single sounding is initiated.

An A-Scan on a single frequency is initiated by selecting the A-Scan function and setting the Frequency Synthesizer to the SINGLE (single frequency) mode via the slide switch on its front panel. In this mode, pin 4 of A3A8/PL1 will be held low by circuitry in the digital section of the synthesizer (A4A1). This will cause D to go high and thus the transmitter will be pulsed continuously, regardless of the condition of the X-Blank Line. The 6 kHz drive to the transmitter power supply will be gated on as B will go high when the A-Scan function is selected, as explained previously.

A display on the Monitor CRT will only appear however when the Monitor Control Line goes low. Thus, a single sounding needs to be initiated for the Monitor CRT to provide an A-Scan display.

The single frequency A-Scan is inhibited by the Main Display control logic on A5A1. When the Main Display Control Line goes low, the synthesizer is returned to the SCAN mode and the logic level on pin 4 of A3A8/PL1 is returned to a high condition via circuitry on A4A1.

Simultaneously, C will go low causing D to remain high, and the transmitter will continue to be pulsed.

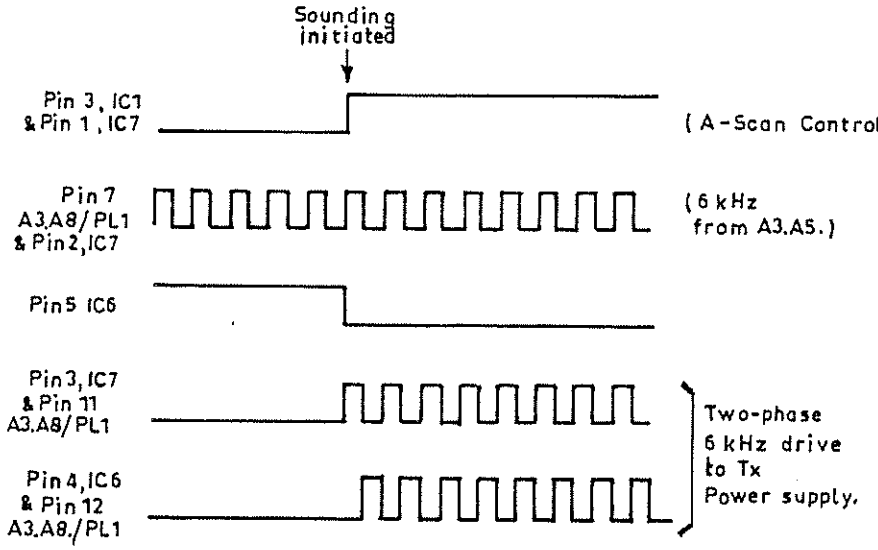
3.7.14 The Transmitter Power Supply Drive Circuit (Dwg: CD-250Y1)

The transmitter power supply requires a two-phase 6 kHz drive. The 6 kHz output from the Clock Primary Dividers (on A3A5) is converted to a two-phase signal by a digital switch which is gated on and off to turn the transmitter power supply on and off.

Refer to drawing CD-250Y1. The 6 kHz from A3A5 enters via pin 7 of A3A8/PL1. The digital switch providing the two-phase output is comprised of one AND-gate from IC7 (pins 1, 2, 3), one NOR-gate from IC6 (pins 4, 5, 6) and an inverter from IC2 (pins 1, 2). The 6 kHz drive is applied to one input of each gate. The two-phase output is provided by each output of the two gates, pin 4 of IC6 and pin 3 of IC7, via R3 and R4.

The output of the A-Scan control gate (pin 3, IC1) is low between soundings, going high when a sounding is initiated as explained in the previous section. Thus, between soundings, pin 1 of IC7 will be low and pin 5 of IC6 will be high. In this condition, the outputs of IC6 and IC7 will be held low, regardless of the condition of their other inputs.

When a sounding is initiated and pin 3 of IC1 goes high, pin 1 of IC7 will go high and pin 5 of IC6 will go low. Thus, when pin 7 of A3A8/PL1 goes high, pin 3 of IC7 will go high, but pin 4 of IC6 will go low. When pin 7, A3A8/PL1 goes low, pin 3 of IC7 will go low and pin 4 of IC6 will go high. Thus, the outputs of the two gates are in antiphase as IC7 will pass the 6 kHz input directly while IC6 will invert it. The operation of this circuit is illustrated in the pulse diagrams of figure 3.7.11, along with the truth table.



TRUTH TABLE

Pin 3 IC1	6 kHz	Pin 3 IC7	Pin 4 IC6
0	1	0	0
0	0	0	0
1	1	1	0
1	0	0	1

FIG. 3.7.11. Operation of two-phase digital switch for transmitter power supply drive.

3.7.15 The Transmit Pulse Gate
(Dwg: CD-250Y1)

This consists of another AND-gate from IC7 (pins 8, 9, 10). The transmit pulses from the operational Clock, A3A11, enter via pin 29 of A3A8/PL1. Pin 9 of IC7 is driven by pin 6 of IC1. As explained in section 3.7.13, pin 6 of IC1 goes high when a sounding is initiated. The transmit pulses on pin 10 of IC7 will then be gated through to the transmitter via R2 and pin 16 of A3A8/PL1.

The pulses reach the transmitter via a lead in the Harness (see drawing CD-262Y1). A switch in series with this lead enables the transmit pulses to be interruped for testing purposes. It is mounted on the right hand side of the harness channel opposite the battery socket, A2SK1.

3.7.16 The Transmit Fail Warning Circuitry
(Dwg: CD-250Y1)

The function of this portion of the Control System is to flash the warning lamp on the front panel of the Program unit (A5) to attract the operator's attention if there is no RF output from the transmitter during a sounding. The warning lamp will continue to flash following a sounding in which the transmitter has failed so that the operator's attention is attracted even though a sounding is not in progress.

The circuitry is in two sections, consisting of the Tx FAIL WARNING LOGIC and the WARNING LAMP GATE. As explained in section 3.3.6, the Transmitter Fail Detector (A6A4) in the transmitter will cause pin 14 of A3A8/PL1 to be held low during a sounding. If there is no RF output from the transmitter during a sounding, it will go high, 'pulled up' by R1.

The Warning Lamp Gate is one AND-gate from IC7 (pins 11, 12, 13). Pulses of one second duration, every other second, are applied to one input (pin 12). These are derived from the Chronometer SECONDS Dividers on A3A5 (see section 3.1.16) and enter via pin 9 of A3A8/PL1. The other input, pin 13, is driven by the output of the Tx Fail Warning Logic. It is normally low, and the warning lamp extinguished. When this input goes high, the '1 sec on, 1 sec off' pulses are gated through to the warning lamp which flashes on every alternate second.

The Tx Fail Warning Logic consists of three NAND-gates from IC9. Two are connected in a latch arrangement with a capacitor, C2, linking their outputs (pins 8 and 11). The operation is apparent from the pulse diagrams of figure 3.7.12.

Between soundings, pin 4 of IC9 will be low and pins 5 and 10 of IC9 will be high. This sets the latch such that the output, pin 11 of IC9, is low. Thus, pin 13 of IC7 will be low and the warning lamp will be extinguished.

When a sounding is initiated, pin 4 of IC9 will go high. If there is RF output from the transmitter, pins 5 and 10 of IC9 will be held low. This maintains the condition of the latch and pin 11 of IC9 (and thus pin 13 of IC7) remains low. Thus the warning lamp will remain extinguished.

If the transmitter fails during a sounding, pins 5 and 10 of IC9 will go high, pulled up by R1. The latch will change state, pin 11 of IC9 and pin 13 of IC7 will go high. The pulses from A3A5 will thus be gated through to the warning lamp. At the end of the sounding period, pin 4 of IC9 will return to a low condition, but the latch output (pin 11, IC9) will remain in a high condition. Thus, the warning lamp will continue to flash.

The purpose of C2 is to prevent glitches from pin 13 of IC7 accidentally resetting the latch as pin 12 goes alternately low and high.

3.7.17 Ancilliary Circuitry

This involves the circuitry that produces the reset pulses for the NI display timebases and the CRT brightening pulses for the SET-UP display. The X-NI timebase reset circuitry is located on A3A10, the Y-NI timebase reset circuitry is located on A3A5 and the SET-UP Z-modulation circuitry is in two parts, one portion is located on A3A12 and the other on A3A5.

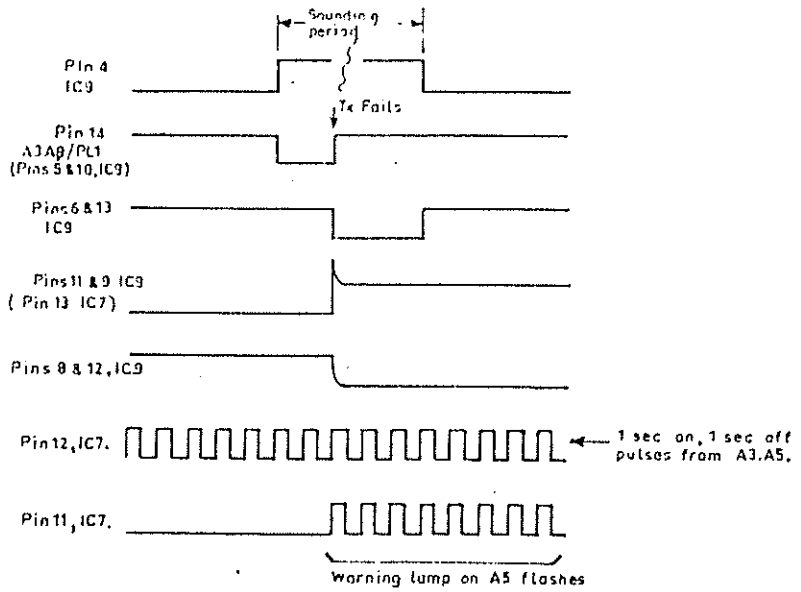


FIG. 3. 7. 12. Operation of the Tx Fail Warning Logic and Warning Lamp Gate.

3.7.18 The X-NI Reset Circuit (Dwg: CD-249Y1)

This is located on A3A10 and involves IC1, IC3 and IC6. The relevant portion of the circuit from A3A10 is illustrated in figure 3.7.13. There are seven inputs, six ($\overline{3kHz}$, $\overline{A5}$, $\overline{B5}$, $\overline{C5}$, $\overline{D5}$, $\overline{A10}$) are derived from the Operational Dividers on A3A11 and one ($\overline{6kHz}$) from the Primary Dividers on A3A5.

The X-NI timebase is reset every 10.666 ms with an 83.333 μs pulse. The pulse diagrams in figure 3.7.14 illustrate the operation of the X-NI reset circuitry. The X-NI timebase is located on A5A1 and the output of the X-NI reset circuit is via pin 4 of A3A10/PL1 and A5A1/PL1.

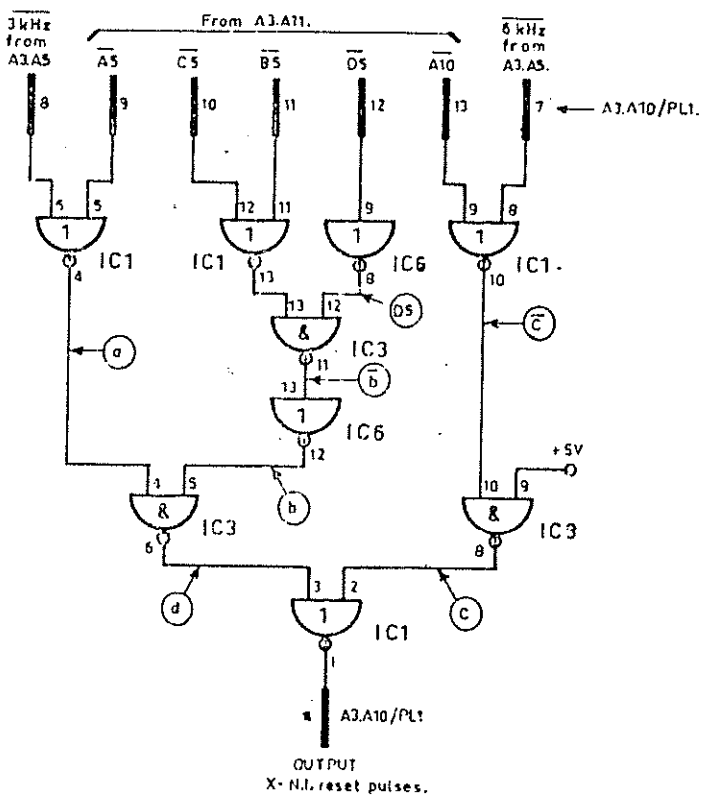


FIG. 3. 7. 13. X-NI reset circuitry.

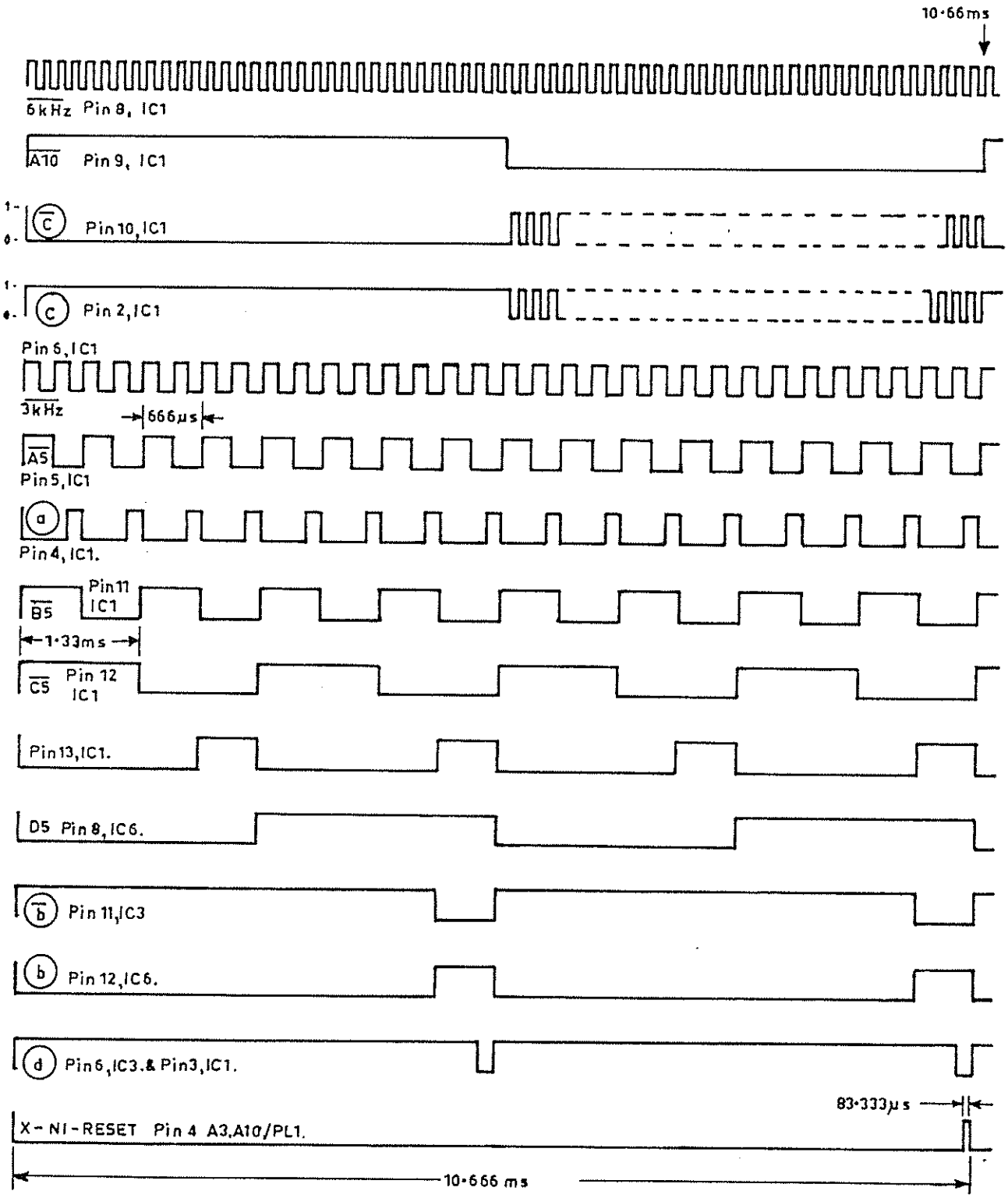
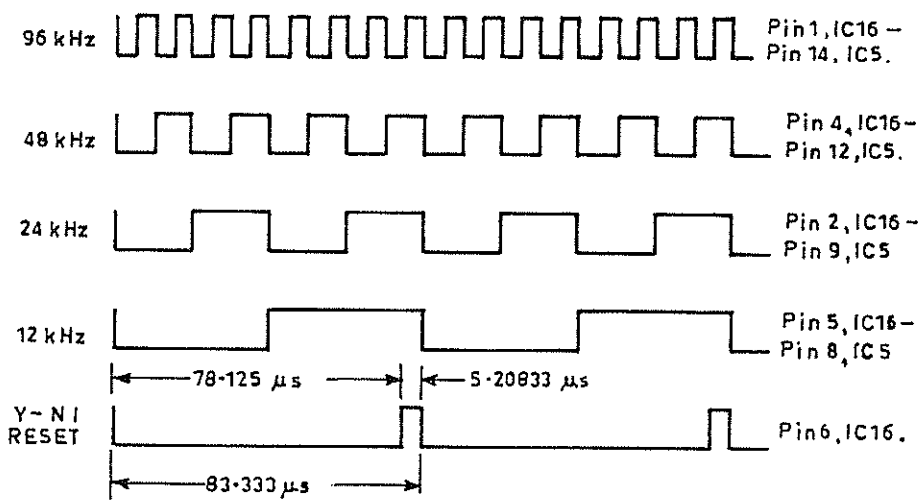


FIG. 3.7.14. Derivation of X-N.I. RESET

3.7.19 The Y-NI Reset Circuit
(Dwg: CD-227Y1)

This is located on A3A5 and involves one four-input NAND-gate from IC16. The Y-NI timebase is reset every 83.333 μs by a 5.20833 μs pulse. The derivation of this pulse is illustrated in the pulse diagrams of figure 3.7.15. The four inputs to the NAND-gate are derived from the outputs of the first of the Primary Dividers, IC5, these being 96 kHz, 48 kHz, 24 kHz and 12 kHz. The Y-NI timebase is also located on A5A1, the output of the Y-NI reset circuit being via pin 12 of A3A5/PL1 and A5A1/PL1.



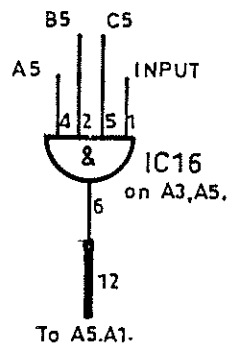


FIG. 3.7.15. Derivation of Y-N.I RESET.

3.7.20 Set-Up Z-modulation Circuit
(Dwgs: CD-227Y1 and CD-229Y1)

The Set-Up display requires the CRT trace to be brightened for each of the first five Y steps for the first seven X steps. To accomplish this, the Set-Up Z-modulation circuit produces seven groups of five pulses which brighten the CRT trace at the required times.

The complete Set-Up Z-mod. circuit is shown in figure 3.7.16. That portion on A3A12 involves four inverters from IC13 and all the three-input NAND-gates from IC14. There are six inputs to the circuit, five ($\overline{A5}$, $\overline{B5}$, $\overline{C5}$, $\overline{D5}$ and $\overline{A10}$) are derived from outputs from the Operational Dividers on A3A11 and one input ($\overline{3\ kHz}$) is derived from the Primary Dividers on A3A5. This portion of the circuit has two outputs, one from pin 12 of IC14 and one from pin 8 of IC14. These are routed through to the other four-input AND-gate from IC16 on A3A5 via pins 15 and 23, respectively, of A3A12/PL1 and A3A5/PL1. The other two inputs to IC16 on A3A5 are $\overline{6\ kHz}$ from the Primary Dividers and the Y-NI reset pulse which appears on the output of the other NAND-gate in IC16, pin 6.

The pulse diagrams in figure 3.7.17 illustrate the derivation of the set-up Z-mod. pulses.

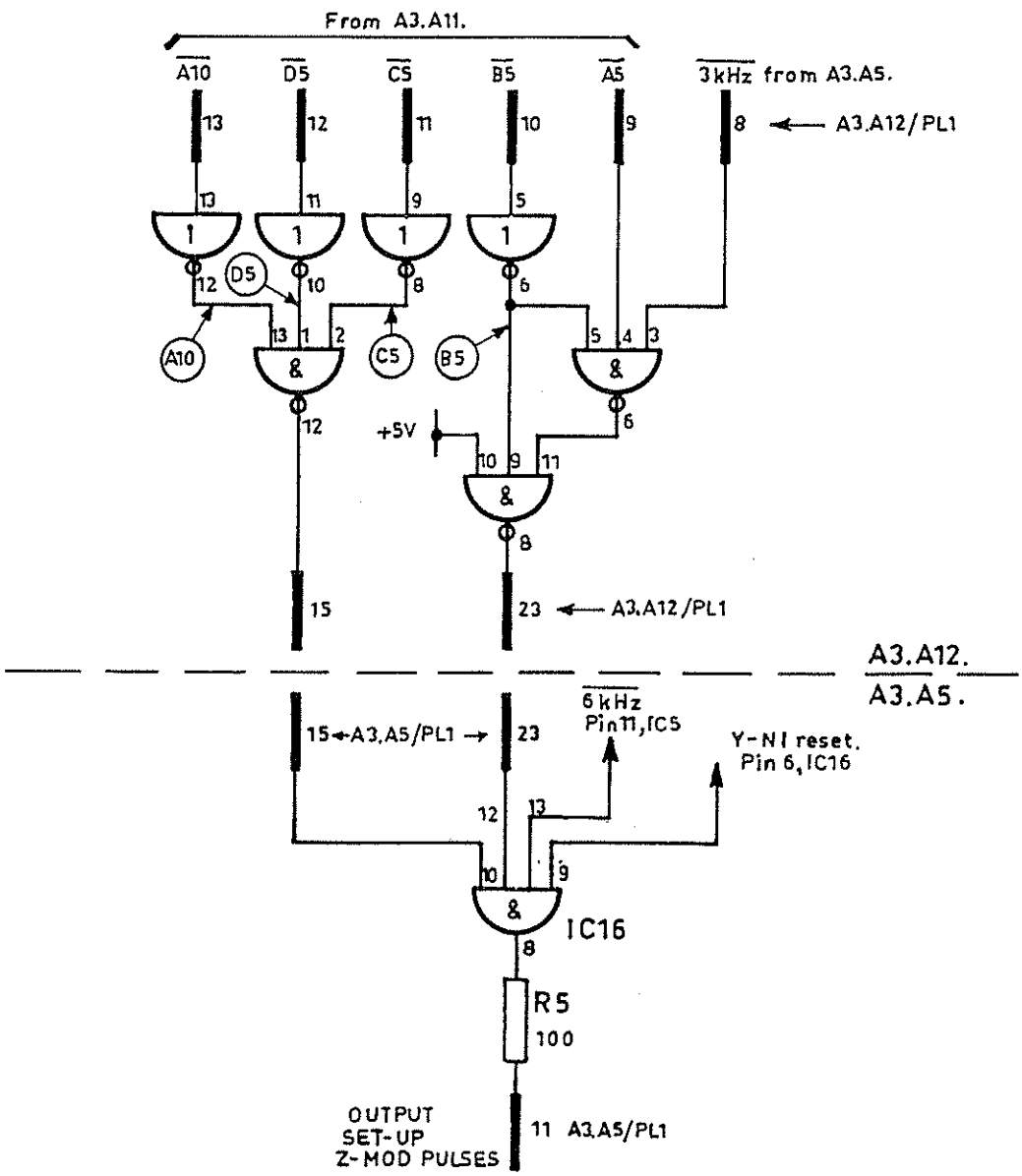


FIG. 3. 7. 16. Set-up Z-modulation circuitry.

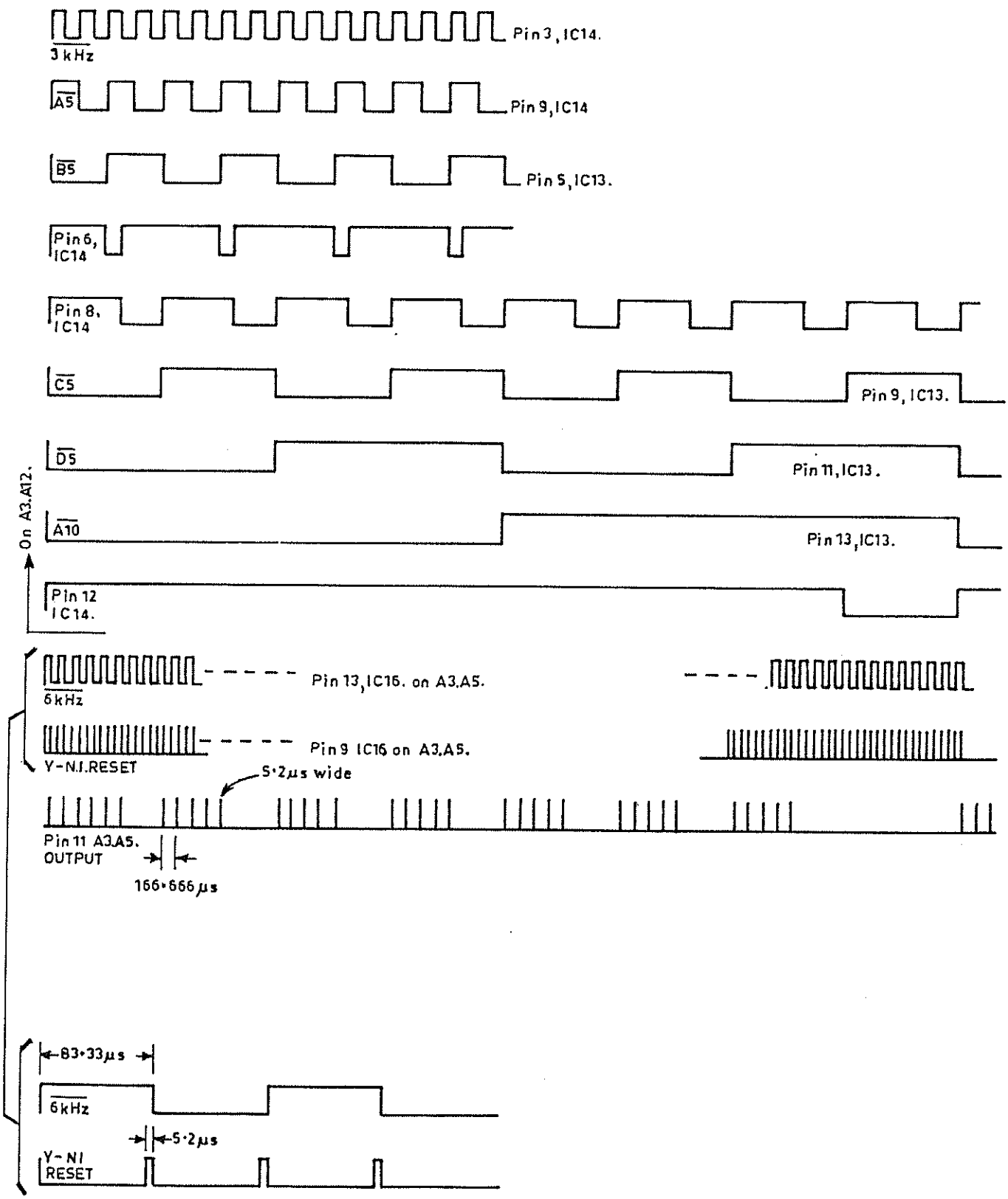


FIG. 3.7.17. Derivation of Z-MOD SET UP pulses.

3. 8
DISPLAY SYSTEM

Par. No.	Title	Drawing No.
3.8.1	Brief Summary	
3.8.2	Main and Monitor Display Assemblies	CD-230Y1 (A8/A10)
3.8.3	The 18 Volt Regulator	" " (A8A1/A10A1)
3.8.4	The Power Supply Assembly	" " (A8A2/A10A2)
3.8.5	The EHT Divider Assembly	" " (A8A3/A10A3)
3.8.6	The Deflection Circuits	" " (A8A4/A10A4)
3.8.7	Z-Modulation Circuit	" " (A8A5/A10A5)
3.8.8	THE TIMEBASES	CD-228X1 (A5A1)
		CD-229Y1 (A3A12)
3.8.9	The Miller Integrator Timebase Circuit	
3.8.10	The Ionogram Timebases, X main and Y main	CD-228X1 (A5A1)
3.8.11	The A-Scan Timebase and Blanking Circuitry	" " "
3.8.12	THE NUMERAL INDICATION TIMEBASES	" " "
3.8.13	Summary of Numeral Indication Display	
3.8.14	The NI Display Deflection Sequences	
3.8.15	The NI Timebases, X NI and Y NI	CD-228X1 (A5A1)
3.8.16	THE SET-UP DISPLAY	
3.8.17	The Staircase Generators, X SET-UP and Y SET-UP	CD-229Y1 (A3A12)

3.8.1 Brief Summary

The display system consists of three subsystems:

(a) the MAIN display assembly for film recording.

(b) the MONITOR display assembly for monitoring the sonde operation.

(c) the TIMEBASE circuitry.

The Main and Monitor display assemblies each contain their own associated power supply, deflection amplifiers and Z-modulation circuitry.

The displays appearing on each cathode ray tube (CRT) are selected by two function switches (designated MAIN and MONITOR) on the PROGRAM unit A5A1. These select the appropriate timebases and blanking signals for the display mode of the sonde function or program selected.

The blanking signals are obtained from circuitry in the CLOCK and CONTROL SYSTEM. The generation of these signals is explained in sections 3.1 and 3.7.

There are four separate display modes. Briefly, these are as follows:

(a) The IONOGRAM, which is displayed during routine soundings or single soundings. The ionogram can be displayed on either the MAIN or MONITOR CRT's, separately or together.

(b) The A-SCAN, which can be displayed on the MONITOR CRT alone and only during routine soundings or single frequency soundings.

(c) The NUMERAL INDICATION (or NI Display), which presents the Preset number, seconds, year, day and time (hours and minutes) on the Monitor CRT.

(d) The SET-UP, which presents a 5 x 7 dot matrix on either the MAIN or MONITOR CRT, separately or together.

Ramp, or sawtooth, generators provide deflection wave forms for the Ionogram, A-Scan and NI Displays, while staircase waveforms are used for the Set-Up display.

A summary of the deflection waveforms and blanking signals associated with each display is shown in drawings GC-30Y1 and GC-30Y2.

3.8.2 Main and Monitor Display Assemblies (A8 and A10, Dwg CD-230Y1)

The circuits of the Main and Monitor displays are identical. Their construction is also identical with the exception of the Main display which has the CRT oriented with X-axis vertical so that the ionograms appear with the correct orientation on the film. The display on the Main CRT is always oriented 90° to that on the Monitor. Both displays are physically and electrically independent.

The circuitry is located on five sub-assemblies in A8 and A10. Each sub-assembly is constructed on a separate printed circuit board. The power supply A8A2/A10A2 is enclosed in a diecast box to reduce radiation to the deflection circuits. The five sub-assemblies are designated as follows:

A8A1/A10A1	18 Volt Regulator
A8A2/A10A2	Power Supply
A8A3/A10A3	Extra high tension (EHT) Divider
A8A4/A10A4	Deflection Circuits
A8A5/A10A5	Z-Modulation Circuit

3.8.3 The 18 Volt Regulator A8A1/A10A1

This supplies regulated 18 volts to the power supply which requires a regulated DC voltage input to maintain constant output voltages. An LM309K or an LM340-T/18IC regulator (IC1) fulfils the functions of regulator and voltage step-down. The input voltage is from the 24 volt supply rail via A8PL1 pins 1 and 3. Those units using the LM309K require a resistive divider consisting of R1, and R2 in parallel with R3, to provide the appropriate voltage to the reference input (pin. 3., IC1) to give 18 volts output.

The input of IC1 is filtered by C1. A choke, consisting of two bifilar windings on a toroid, in series with the output leads, prevents high frequency spikes from the power supply (sub-assembly A2) appearing on the main 24. V. supply rail.

3.8.4 The Power Supply Assembly A8A2/A10A2

This unit provides -2.3 kV EHT for the CRT anodes, +250. V. HT collector supply for the deflection amplifiers together with + and - 23. V. supplies for the deflection amplifiers, bias regulators and Z-modulation input stage. In addition, two extra-insulated transformer windings provide 6.3 VAC and 23 VAC. These two windings are connected to portions of the Display assembly that operate at the EHT potential and require greater insulation.

The power supply employs a conventional push-pull switching inverter, operating at about 6 kHz, to drive two output transformers, T2 and T3. Transformer T1 is the saturating feedback transformer of the inverter. The primaries of T2 and T3 are in parallel and connected across the collectors of the two inverter transistors TR1 and TR2. The primaries are centre-tapped to provide a connection for the regulated 18 V input.

The secondary of T2 supplies a full-wave, voltage quadrupler rectifier, providing -2.3 kV EHT. This rectifier circuit causes high peak current spikes in the secondary of T2. The EHT winding has been separated from T3 to avoid undesirable coupling of these spikes into the lower voltage supplies.

Transformer T3 has four secondaries. One supplies a full-wave voltage doubler, consisting of D2, D3, C3 and C4, which provides +250 V for the collectors of the deflection amplifiers. A second winding supplies two half-wave rectifiers, consisting of D4, C5 and D5, C6, which provide +23. V. and -23. V. respectively. The other two windings provide 6.3 VAC for the CRT filament and 23 VAC for a half-wave rectifier supplying the Z-Modulation circuit.

The assembly is enclosed in a diecast box, the outputs being brought through on insulated feedthrough terminals. The two inverter transistors TR1 and TR2 are mounted using the box as a heatsink.

3.8.5 The EHT Divider Assembly A8A3/A10A3

This unit is constructed on a printed circuit board, with the exception of the intensity and focus controls which are screwdriver adjusted potentiometers accessible from the front panel. It provides the appropriate potential for the CRT cathode, the grid, G1, and the focus anode. The accelerator anode potential is derived from circuitry on the deflection assembly A8A4/A10A4.

A filter consisting of C1, C2 and R1, R2, R3 reduces the ripple from the EHT rectifier. Then follows the intensity control R4 which provides a variable potential at the grid of the CRT (V1, pin. 3.), controlling the trace brightness. This control only functions when the Z-Modulation circuit brightens the trace. The grid is always at a negative potential with respect to the cathode and the intensity control cannot vary the grid-cathode potential below cutoff (which brightens the trace) when the Z-Modulation circuit blanks off the trace. The intensity potentiometer, R4, is mounted on an insulated panel separately from the printed circuit board. An insulated shaft extension provides access at the front panel.

Resistor R5 follows the intensity control and provides a minimum potential difference between the cathode and the grid of the CRT. Terminal 5 on the printed circuit board is the cathode circuit reference potential. The Z-Modulation circuit holds the cathode at +23. V. with respect to this point to blank the trace, removing this voltage to brighten the trace. The Z-Modulation circuit 'common' is connected to terminal 5. on the printed circuit board. Capacitor C3 provides a low impedance AC path between the grid and cathode reference terminal to prevent EHT ripple modulating the trace brightness.

The focus anode potential is derived across R9. The focus control, potentiometer R8, is in parallel with R9, and provides a variable potential to the focus anode.

It is mounted separately to the printed circuit board, on the same insulated mount as the intensity control, R4. It too is accessible at the front panel via an insulated shaft extension. A further six resistors, making R10, completes the potential divider circuit.

3.8.6 The Deflection Circuits A8A4/A10A4

There are separate amplifiers to drive the X and Y deflection plates of the CRT. Each is an emitter-coupled differential amplifier with single ended input and constant current emitter supply. The circuits are almost identical. The X-amplifier has more gain than the Y-amplifier as the sensitivity of the CRT X deflection plates is much less than the Y deflection plates.

The X or Y deflection voltage is governed by the maximum available collector-to-collector voltage swing, of the deflection transistors TR1-TR4 and TR5-TR8, before clipping occurs. Potentiometer R13 sets the bias on the constant current transistors TR2-TR3 and TR6-TR7, thus setting the quiescent collector currents of TR1-TR4 and TR5-TR8 and thus the available collector-to-collector voltage swing. The gain of each amplifier is individually adjusted over a small range by varying the resistance coupling the emitters of the two amplifier transistors. Decreasing this resistance increases the gain. Potentiometer R8 is the X GAIN control and R21 the Y GAIN control. Both of these potentiometers are multiturn trimpots, mounted on the printed circuit board and accessible from the front panel. Note: that R13 is a trimpot, also mounted on the printed circuit board, but is not accessible from the front panel. It is set for maximum deflection voltage swing during initial set-up procedures.

The X SHIFT control, R2, varies the base bias on TR1, increasing or decreasing the static potential difference between the collectors of TR1 and TR4, thus affecting the position of the trace at the commencement of a sweep. The Y SHIFT (R15) functions in the same manner. Both potentiometers are multiturn trimpots, as for R8 and R21, and are accessible from the front panel.

The inputs to the X and Y deflection amplifiers are positive going ramp waveforms of five volt amplitude, or in the case of the SET-UP display, staircase waveforms, which are selected by the 'function control' switches on the PROGRAM unit A5A1.

These switches provide the appropriate inputs according to the display mode selected. The inputs are always positive going. Capacitors C1 and C2 in the X-amplifier prevent high frequency signals from the Y-amplifier appearing on the X plates of the CRT by providing a low impedance to ground at these frequencies.

Regulated, +20. V. bias for the shift controls is obtained from an IC regulator, an LM305AH (IC1). The input is +23. V. obtained from the power supply A8A2/A10A2. The required voltage for the reference terminal (pin. 6.) is provided by the resistive divider R25/R30. Diode D5 prevents the destruction of IC1 should the input voltage exceed 30. V. A regulated -20. V. emitter supply for the constant current transistors TR2-TR3 and TR6-TR7 is derived from the -23. V. output of the power supply via a zener diode regulator circuit. This supply rail does not require the same degree of regulation as the +20. V. bias supply. Diode D2 is an 18. V. zener, the regulated output being raised to 20. V. by the addition of diodes D3 and D4 in series with D2.

The collector HT for the X and Y amplifiers is regulated at +200. V. by the zener diode D1. The power supply +250. V. output supplies the zener regulator circuit.

The CRT astigmatism is adjusted by varying the potential on the accelerator anodes with respect to the mean potential of the deflection plates. Potentiometer R28 derives a potential of about 100. V., for the CRT accelerator anodes, from the collector HT supply. This can be varied about $\pm$ 20. V. to adjust the astigmatism. This control is a multiturn trimpot, mounted on the deflection board, and accessible from the front panel.

3.8.7 Z-Modulation Circuit A8A5/A10A5

The CRT trace is normally blanked. Positive pulses applied to the input of the Z-Modulation circuit turn on the trace at the appropriate time of a sweep to form the display. CRT blanking is achieved by holding the grid-cathode potential beyond cutoff. Brightening pulses to the Z-Modulation input reduce the grid-cathode potential below cutoff, brightening the CRT trace.

The circuit employs an LM311N voltage comparator IC, operating as a switch, to provide negative-going brightening pulses to the CRT cathode. As the 'common' rail for this circuit is at near-EHT potential, the input has to be DC isolated. This comprises a light-emitting diode (LED) optically coupled to a photodiode, the arrangement being encapsulated in an opaque material. When the LED is energised, the reverse resistance of the photodiode is greatly reduced. As the input and output devices are only connected by a light beam they are DC isolated, the insulation between them having a high breakdown voltage.

The photodiode of the MCD-1 is in one arm of an unbalanced bridge forming the input circuit of IC1. With no input to TR1, the photodiode reverse current is low and the bridge is unbalanced such that the non-inverting input of IC1 (pin. 2.) is more positive than the inverting input (pin. 3.). The output of IC1 is then +23. V. with respect to the common rail and the CRT is blanked. The positive brightening pulses cause TR1 to conduct and the photodiode unbalances the bridge in the opposite direction causing the output of IC1 to drop to the common rail, reducing the CRT grid-cathode potential below cutoff and brightening the CRT trace.

3.8.8 THE TIMEBASES (Dwgs. CD-228X1 and CD-229Y1)

The four different display modes require different X and Y timebases or deflection waveforms to produce the display. The display modes are:

The IONOGRAM
The A SCAN
The NUMERAL INDICATION (or NI)
and the SET-UP

Five ramp (or sawtooth) waveform timebases are used for the Ionogram, A-Scan and NI displays. They are located in the PROGRAM unit A5A1 (Dwg CD-228X1). The table below lists the timebases used for each display mode:

IONOGRAM	-	X MAIN	Y MAIN
A SCAN	-	X A SCAN	
NI	-	X NI	Y NI

These timebases all employ 'Miller Integrator' circuits, the general form of which is shown in fig. 3.8.1.

The sweep widths of the four timebases X main, Y main, X NI and Y NI are all adjustable by four preset controls accessible from the front panel of the program unit. Each is a multiturn trimpot and is designated accordingly.

The X A Scan sweep width is also adjustable, this control also being a multiturn trimpot. It is mounted on the printed circuit board of the Program unit (A5A1), but is not accessible from the front panel.

The Set-up display employs two 'staircase' generators for the X and Y deflection. These are located on A3A12 (Dwg. CD-229Y1).

3.8.9 The Miller Integrator Timebase Circuit

The five timebases mentioned above each employ an LM301 IC operational amplifier (op-amp). As indicated in fig. 3.8.1, the capacitor of an RC circuit, Ct is connected between the output and the inverting input of the LM301. The resistor, Rt, is connected from the inverting input to a set voltage 'V'. A transistor (TR1), in parallel with the capacitor, Ct, sets the initial condition of zero output when the reset input is held at a logic level of one (1), causing TR1 to conduct, holding Ct discharged and the op-amp. at unity gain.

The ramp is initiated when the reset input goes to a logic level of zero (0), removing base drive from TR1, which ceases conducting. The capacitor, Ct, will then charge via Rt, part of the charging current also flowing to the inverting input. The resultant output is a linearly increasing voltage. The DC input offset bias of the op-amp. will add to the charging current of Ct, further increasing the voltage at the output. The final amplitude (the 'sweep width'), is determined by the voltage V, adjustable by the potentiometer R1, and the period of the reset pulse.

The capacitor Ct provides compensation for the LM301 operational amplifier to ensure that it remains stable during the ramp period. The 100 ohm resistor in series with the collector of TR1 limits the current through the reset transistor to a safe value during reset.

3.8.10 The Ionogram Timebases, X Main and Y Main (Dwg CD-228X1)

The X main timebase is initiated at the commencement of each 20 second period when the logic level on pin. 31 of A5A1/PL1 goes low. The ramp output of IC13 rises to about five volts amplitude just prior to reset. After 12.3 seconds, the logic level on pin. 31. goes high, TR6 then conducts, resetting the output of IC13 to zero. The output remains at zero until the commencement of the next 20 second period, as the level on pin. 31. remains high. The X Main reset pulse is obtained from circuitry on A3A8 and is described in Section 3.7. The output and reset waveforms are illustrated in fig. 3.8.2. The amplitude of the ramp, the sweep width, is set by R48 ('X-MAIN').

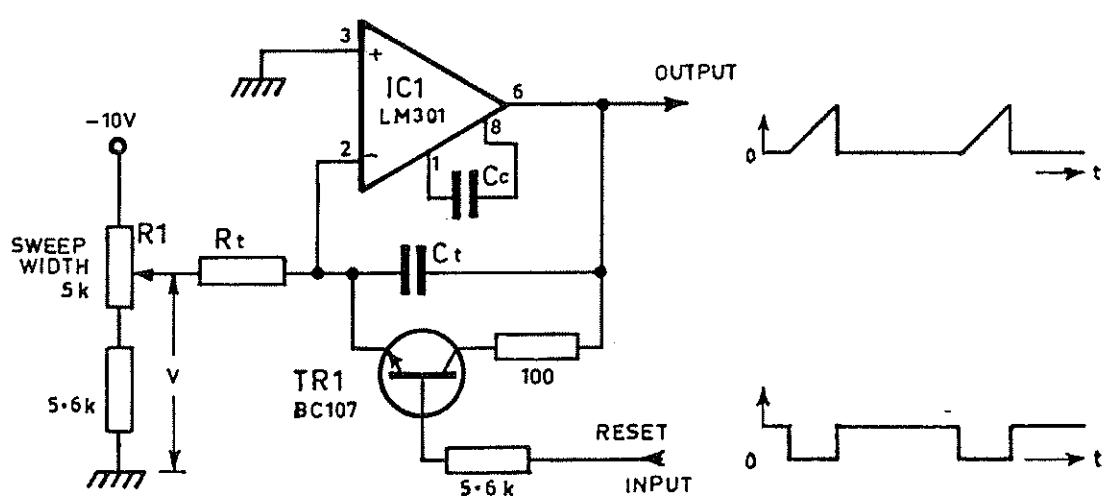


FIG. 3.8.1. 'Miller Integrator' timebase circuit.

The Y Main timebase is initiated at the commencement of the 'first part' of each transmit pulse sequence and reset 6 mS later. The first transmit pulse sequence commences at the lowest frequency channel, at the same time as the X Main timebase is initiated. The Y Main timebase commences its next sweep 21.333 mS later and completes 577 sweeps during the X timebase period. The sweep is initiated when the logic level on pin. 28 goes low (0). The ramp output of IC12 rises to about five volts amplitude just prior to reset. The output remains at zero until the commencement of the next transmit pulse sequence. The Y Main reset pulse is obtained from circuitry on A3A11 and is described in Section 3.1. The output and reset waveforms are illustrated in fig. 3.8.3. The amplitude of the ramp (sweep width) is set by R37 ('Y-MAIN').

The outputs of both timebases are routed through the Main and Monitor switches, S1 and S2 respectively, to the MAIN and MONITOR display units, A8 and A10.

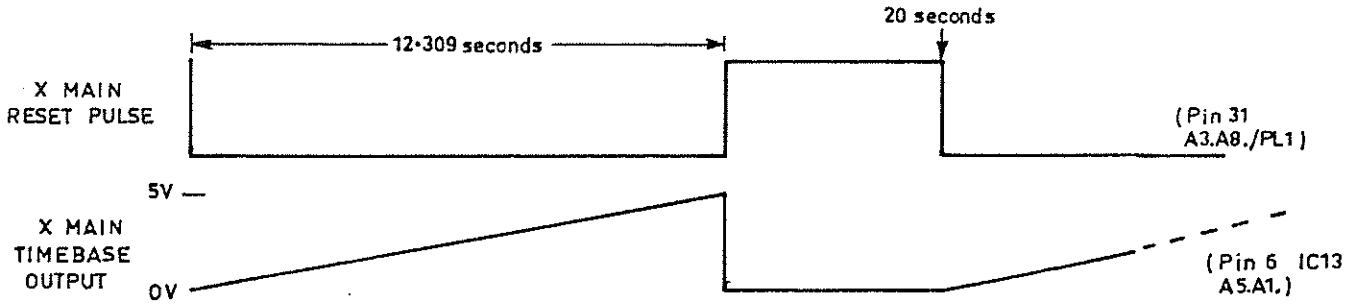


FIG. 3.8.2 X Main Timebase, Reset & Output waveforms.

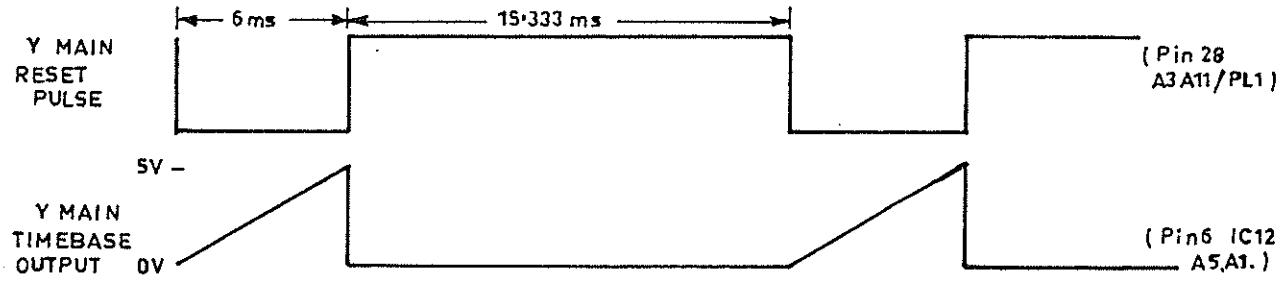


FIG. 3.8.3. Y Main Timebase Reset & Output waveforms.

3.8.11 The A-Scan Timebase and Blanking Circuitry (Dwg. CD-228X1)

The A-Scan can only be displayed on the Monitor CRT, either during routine or single soundings.

The X A-Scan timebase is initiated during the 'second part' of the transmit pulse sequence following the first transmitted pulse. It commences 666 μS after the transmit pulse so that the ground pulse and signals in the first 100 km are not displayed. The timebase is reset 4.666 mS later, the sweep covering the virtual height range from 100 km to 800 km.

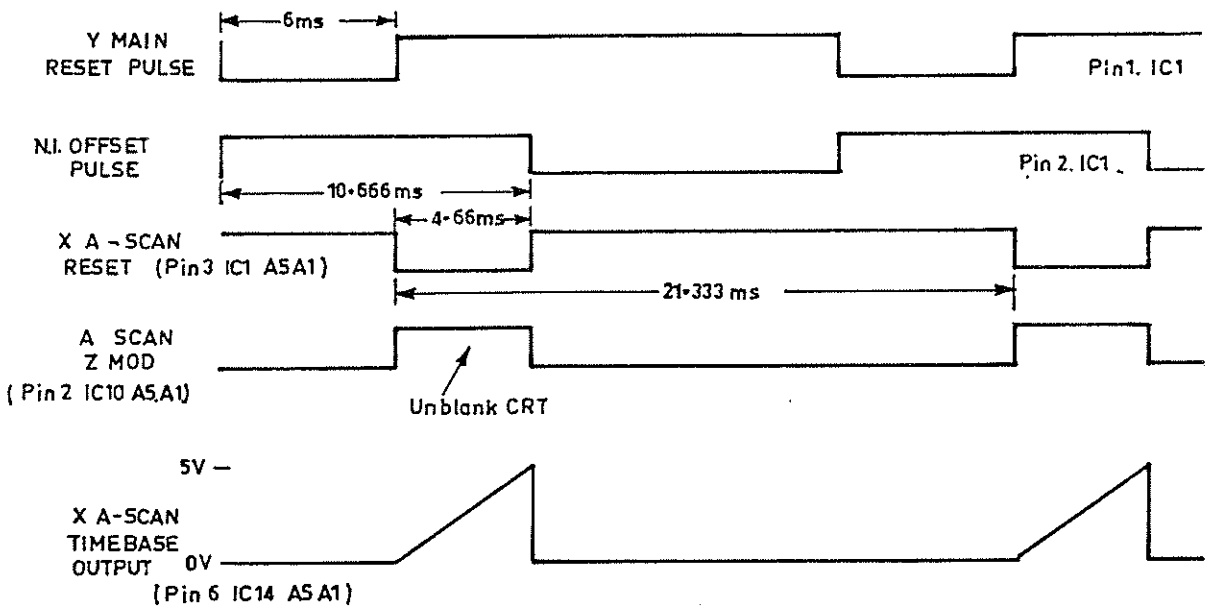
Input to the Y deflection amplifier of the MONITOR Display A10, is a signal derived from the receiver detector (on A7A8) routed through the Monitor function control switch S2.

The reset pulse is derived from the Y Main reset pulse (on pin. 28, A5A1/PL1) and a 10.66 mS pulse from the Operational Dividers on A3A11. This pulse also serves to control the 'NI offset' and appears on pin. 14, A5A1/PL1. These two pulses go to a two-input NAND gate (IC1, pins. 1 and 2), the output of which is high at the commencement of the transmit pulse sequence and goes low 6 mS later. After a period of 4.66 mS, the output again goes high. This is repeated every 21.33 mS, the period of the transmit pulse sequence.

The CRT trace needs to be unblanked during the X A-Scan ramp period. An inverter (IC10, pins. 1 and 2) provides a positive pulse to the MONITOR Display Z-mod to brighten the CRT trace. The waveforms are shown in fig. 3.8.4.

The amplitude of the X A-Scan ramp is set to about five volts by R17, which is on the printed circuit board A5A1 and is not accessible from the front panel.

The timebase output and blanking signals are both routed through the Monitor function control switch S2.



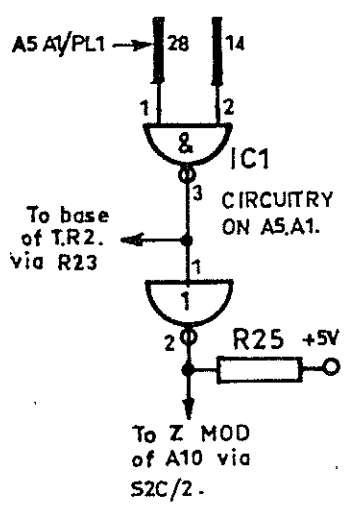


FIG. 3. 8. 4. X A-SCAN Timebase Reset & Output waveforms and CRT Unblanking pulse.

3.8.14 The NI Display Deflection Sequences

The CRT trace completes two sweeps in the X direction during the period it takes to write all the numbers of the NI display. For each X-sweep, the CRT trace completes 128 Y-sweeps to provide the 256 lines needed to display the complete sequence of numbers. The Y-sweep is 'offset' during the period of the second X-sweep so that the Day and Time numbers, which are generated during the last half of the NI numeral generation period, are written on the CRT above the Preset Number, Seconds and Year. This action is called 'NI OFFSET'. It is effected by a pulse operating a transistor switch which changes the DC level of the NI deflection voltage.

So that the numbers appear centred on the CRT screen, each timebase does not commence at zero volts output, but has an initial DC offset. The X-sweep commences at about one-quarter of the CRT deflection width and the sweep width is set so that the X-sweep terminates near three-quarters of the CRT deflection width.

The Y NI sweep width is somewhat less than one-fourth of the total CRT deflection width for both rows of numbers.

For the bottom row of numbers, the Y-sweep commences at about one-quarter of the CRT deflection width and terminates a little prior to the horizontal centre line of the CRT screen. Following the end of the first X-sweep, the 'NI Offset' Pulse causes the Y-sweep to commence a little above the horizontal centre line of the CRT. The Y-sweep then terminates at about three-quarters of the deflection width, to trace out the top row of numerals during the second X-sweep period.

3.8.15 The NI Timebases, X NI and Y NI (Dwg CD-228X1)

The X NI timebase completes two sweeps every 21.333 mS, the NI numeral generation period (see Section 3.6). It is first initiated at the commencement of this period and is then reset so that it commences a second sweep 10.666 mS later. The reset pulse period is 83.333 µS, and thus the X NI timebase period is slightly shorter than 10.666 mS. The logic level on pin. 4 of A5A1/PL2 goes high to reset the timebase. The reset pulse is provided by circuitry on A3A10, the operation of which is explained in Section 3.7.

The X deflection voltage, which is taken from the junction of R28, R32 and R34 commences at about 1.25 V. and rises to about 3.75 V. The initial DC offset is provided by the voltage divider network, from the 10 V. supply rail, formed by resistors R34, R32 and R28. The output of IC9 (pin. 6) is initially zero, thus R32 and R28 will be effectively in parallel at that time. As the output voltage of IC9 rises, so does the voltage at the junction of the three resistors, thus providing the deflection voltage. The amplitude of the ramp at pin. 6 of IC9 is set to about 5 V., as for the other timebases, by R20 ('X NI').

The X NI timebase ramp, deflection and reset wave forms are illustrated in fig. 3.8.7.

The Y NI sweep is initiated at intervals of 83.333 µS, completing 256 sweeps during the 21.333 mS of the NI numeral generation period (see Section 3.7). The first Y-sweep commences at the same time as the first X-sweep.

The Y deflection voltage is taken from the junction of R40 and R44. During the first X-sweep the level on pin. 14 of A5A1/PL1 is high and TR5 conducts. At the beginning of each Y sweep that occurs during the first X-sweep, the output of IC5 (pin. 6) is at zero volts and the voltage divider

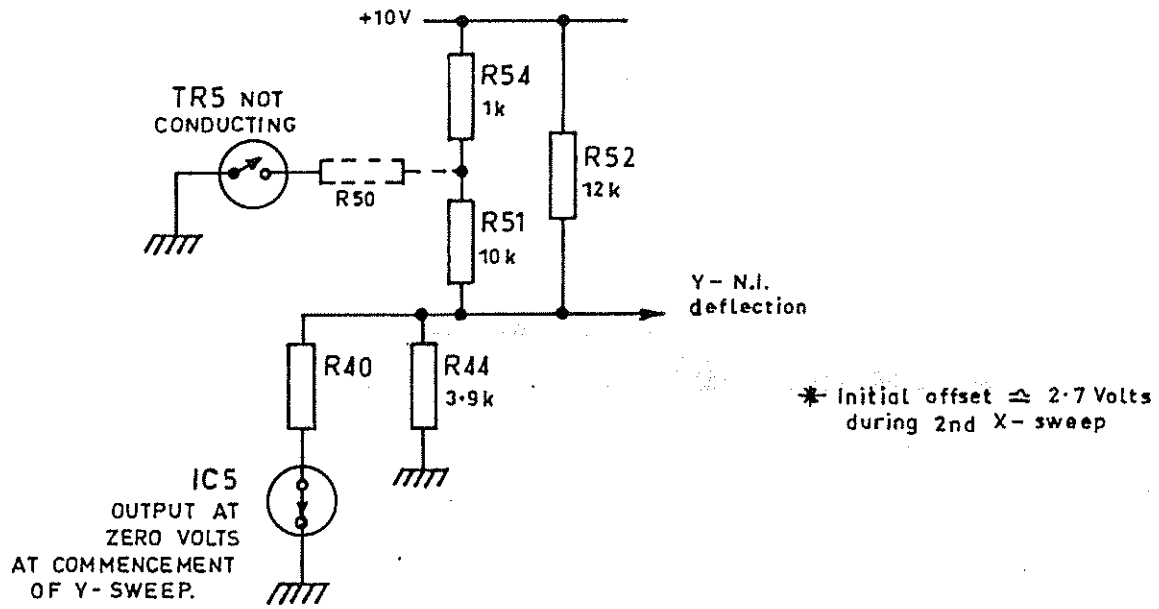


FIG. 3.8.9. Resistive divider circuit during second X-sweep.

The Y NI timebase is reset by a 5 μS pulse, which appears on pin.12 of A5A1/PL1 and is derived from circuitry located on A3A5. The Y-sweep period is thus about 78 μS. The reset, timebase ramp, NI offset and deflection waveforms are illustrated in fig. 3.8.10. The relationship between the X NI and Y NI deflection waveforms and the NI offset pulse is illustrated in fig. 3.8.11.

The NI offset pulse is derived from the dividers of the Operational Section of the CLOCK, located on A3A11.

The amplitude of the ramp at pin. 6 of IC5 is a little over three volts. This is set by the trimpot R31 ('Y NI').

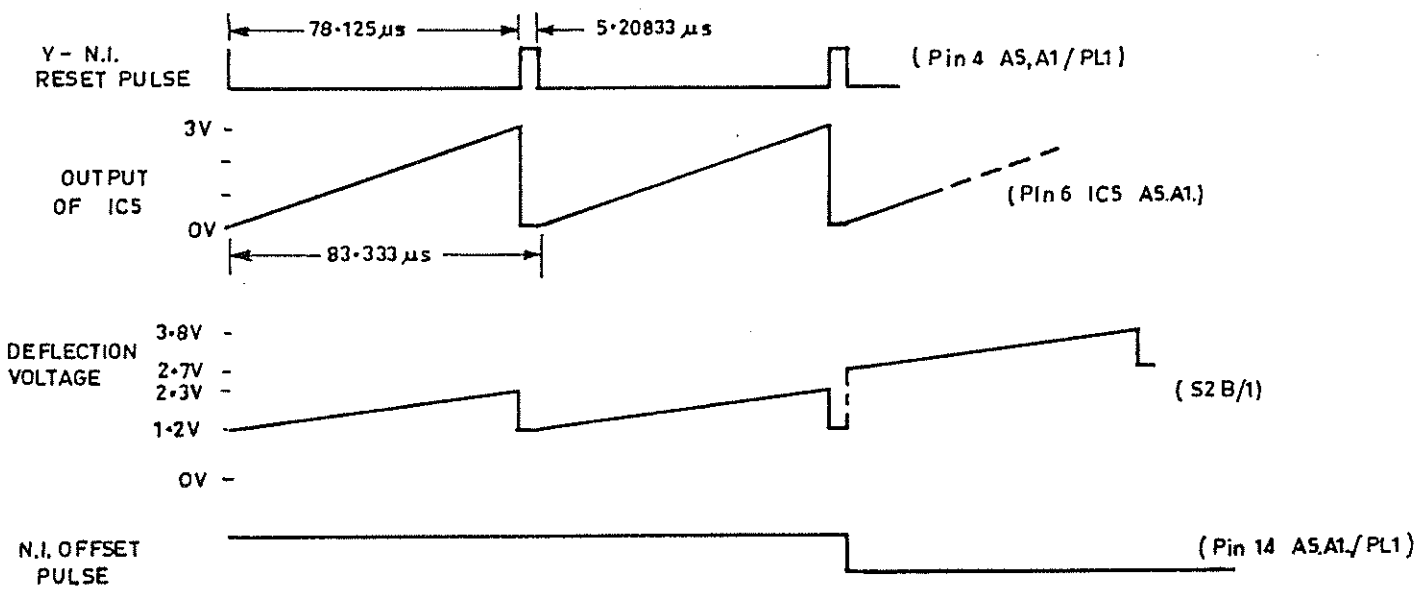


FIG. 3.8.10. Y-N.I. Timebase waveforms.

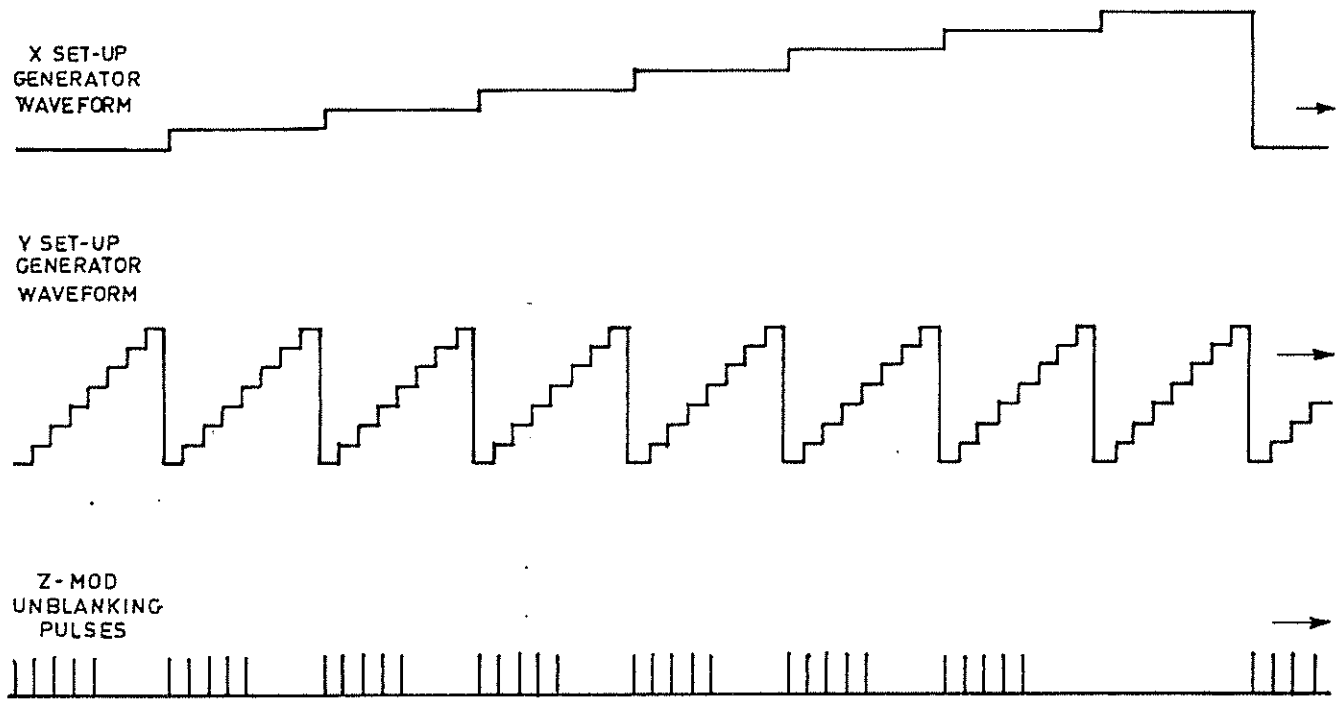


FIG. 3.8.13. Set up display, deflection waveforms & Z-mod pulses.

In addition, the voltage level of the sixth and succeeding steps of the Y Set-Up generator also deflects the CRT trace beyond cutoff when the Y-gain of both the Main and Monitor display units is correctly set. The eighth step of the X Set-Up generator deflects the CRT trace beyond cutoff when the X-gain of both display units is correctly set.

The period of each step of the Y Set-Up staircase is 166.66 mS. the eight steps being completed in 1.33 mS. The period of each step of the X Set-Up generator is 1.33 mS,its eight steps taking 10.66mS to complete.

3.8.17 The Staircase Generators, X SET-UP and Y SET-UP (Dwg. CD-229Y1)

The X and Y Set-Up staircase generators are located on assembly A3A12, their outputs being routed through the function switches (S1 and S2) on the Program unit A5. The unblanking pulses for the Z-modulation of the CRT's are derived from circuitry on A3A5 and A3A12 (see Section 3.7 for an explanation). These pulses are also routed through the function switches.

Both generators are identical in operation. Only the output levels and duration of the steps differ. Each generator consists of a D/A converter followed by an inverting amplifier. The output of the D/A converter is a negative-going staircase, the inverting amplifier converting this to a positive-going staircase. The gain of each amplifier being such that the levels of the fifth step of the Y staircase and the seventh step of the X staircase are at five volts. The succeeding steps of each generator will exceed five volts and thus deflect the CRT trace beyond cutoff.

The general form of the circuit is illustrated in fig. 3.8.14. The three inverters from the inputs A, B and C are of the open-collector type, the collector load at each inverter being the resistor between the +5V supply and the inverter output.

Each inverter acts as a switch. When the input is low (logic level 0), the inverter output will be high (logic level 1), allowing a current to flow into the op-amp. input from the +5V supply. The input current, and thus the output voltage level, is determined by the two resistors in each

either of two open collector NAND-gates from the Camera Drive Control Circuitry on A5A1 (see figure 3.7.4 in section 3.7). The output of whichever of these NAND-gates is connected to R1 via the cam switch, will go low during the 15.333 mS period of the camera drive pulse. This will draw current through R1/R2, causing TR1 to conduct. No current will be drawn during the 6 mS period of the camera drive pulse and TR1 will cease conducting. When TR1 conducts, the voltage across R3 will increase, turning TR4 on for 15.333 mS. As the camera motor, M1, is the collector load of TR4, it will receive current for this period, and will commence to turn. So long as the camera drive is applied, the motor will receive a pulse of current for the 15.333 mS period of the camera drive waveform.

Also during the 15.333 mS period, TR2 will conduct as its base is driven from the collector load of TR1. The collector voltage of TR2 will drop to almost zero volts and C1 will discharge rapidly via D1. The base of TR3 will be reverse biased when this happens, thus TR3 and TR5 will remain off. During the following 6 mS period TR1, TR2 and TR4 will be turned off. C1 will then charge via R6, the charging current turning TR3 and TR5 on. When TR5 conducts, it will short-circuit the motor and the back-emf created by its motion, thus acting as an electromagnetic brake. TR3 and TR5 will remain on until C1 charges to about 4V, but this takes longer than 6 mS and thus both transistors will remain on for the duration of the 6 mS portion of the camera drive waveform.

Thus, the drive voltage to M1 is pulsed on and off, 15.333 mS on - 6 mS off, the inertia of the attached load of gears, shutter and film, averaging the motor speed.

When the camera drive is removed, TR1, TR2 and TR4 will turn off, TR5 will then brake the motor as explained above, stopping it rapidly. When C1 has charged to greater than 4V, TR3 and TR5 will turn off and the circuit is then restored to its initial condition.

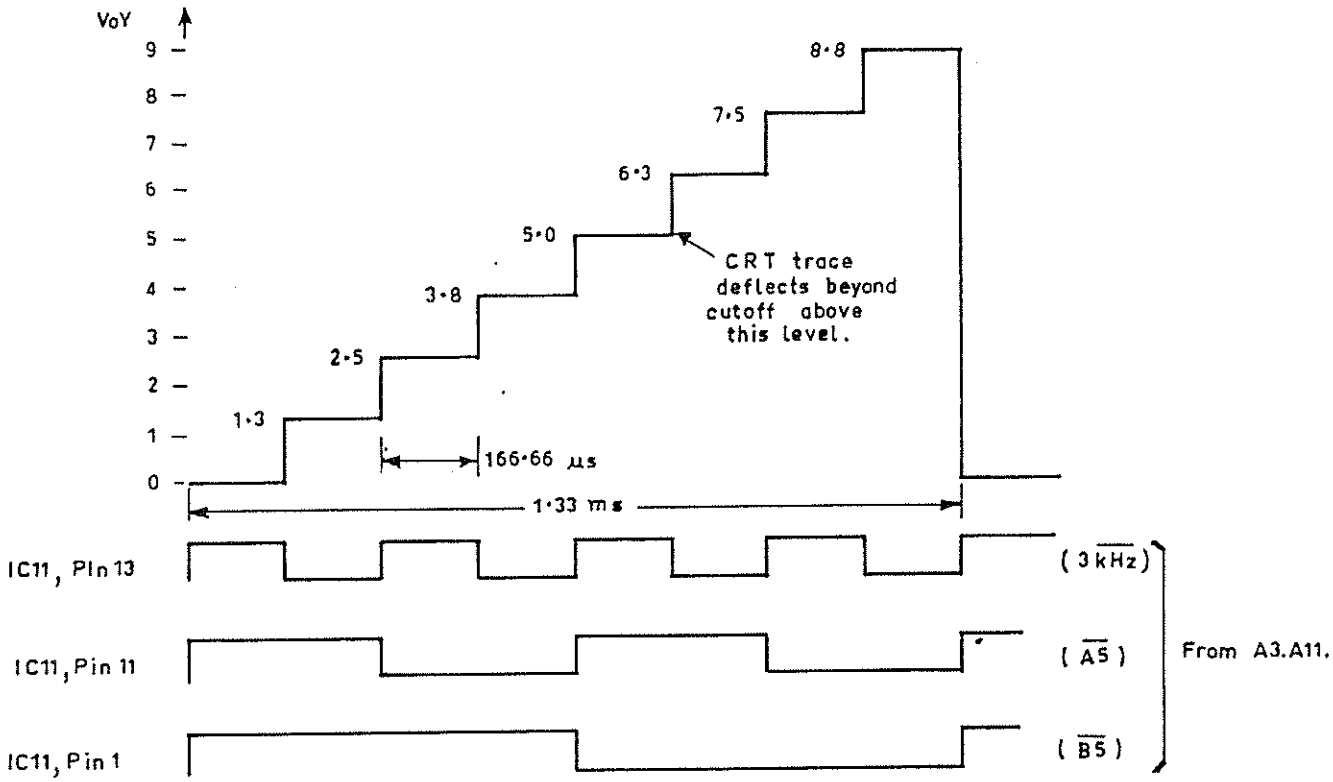


FIG. 3.8.16. Y set-up, input & staircase.

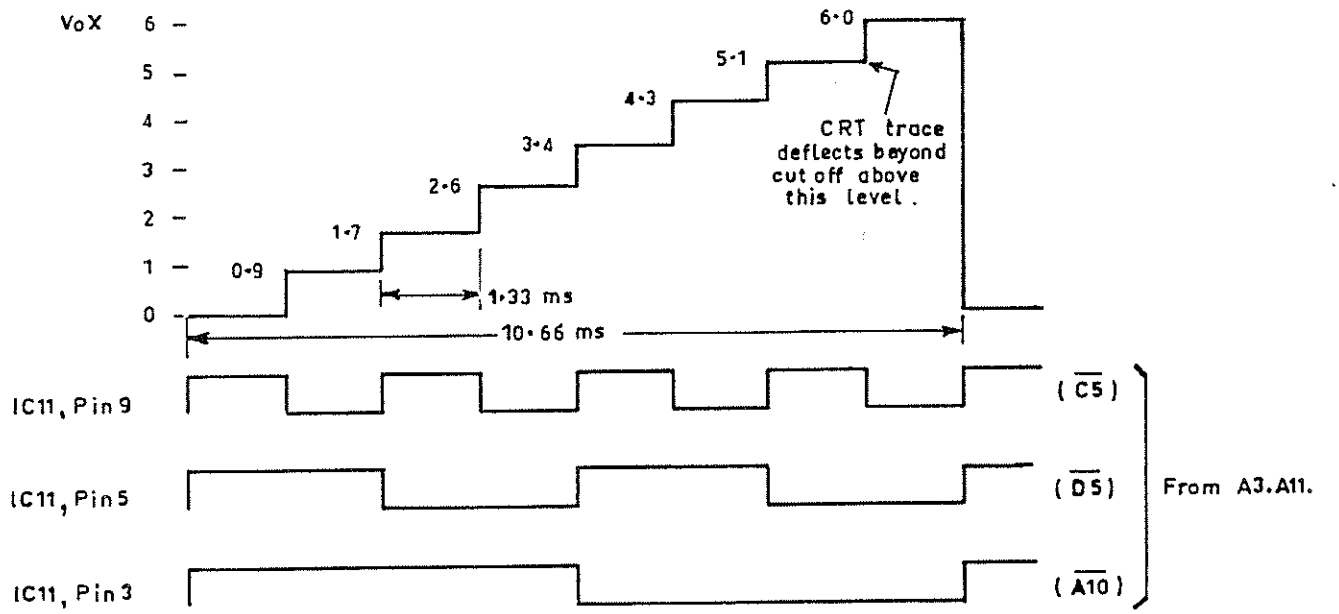


FIG. 3.8.17. X set-up, input & staircase.

3.9.1 Brief Description

The camera is a Vinten Mk III 16mm scientific movie camera modified for this application. A Schneider-Kreuznach/Companon 1:4/28mm enlarger lens is used as this provides the least distortion of the CRT image. The original lens mount has been discarded and replaced by a brass extension bush which accepts the lens used.

The film drive and shutter are operated by a small DC electric motor via a set of gears which can be adjusted to vary the film speed. The speed selection knob is located on the side of the camera housing and is normally set at "8 & S.S.". The camera motor is driven by circuitry (the CAMERA MOTOR DRIVE, A9A1) mounted inside the camera housing. This receives drive information derived from the CLOCK SECONDS BOARD on A3A5, via portion of the Control circuitry in the PROGRAM unit A5 (see section 3.7.5). Film recording is controlled from the Main Display function switch mounted on the front panel of this unit. An ionogram is recorded on the film each time a sounding is initiated at intervals according to the program selected. No film record can be made when the SET-UP function is in use. The shutter is opened and the film advanced slightly at the commencement of each sounding period. During the last two seconds of each sounding period, from second 18 to second 20, the shutter is closed and the film advanced.

The camera focus is set when the ionosonde is originally commissioned and should not normally need subsequent adjustment.

3.9.2 The Camera Motor Drive Circuit A9A1

The circuit and p.c. board layout are given in drawing CD-404Y1. The drive waveform +5V supplies and common return leads enter via A9A1/SKI which is mounted on the camera housing. A plug, A9A1/PLI connects to the circuitry on A5A1 via a 500m lead which passes through a hole in the front panel of A5.

Camera Drive

The camera drive waveform enters via the white wire connected to pin 7 of A9A1/SKI. It is connected to the camera shutter 'position direction' circuitry comprising TR1, the J-K flip-flops (IC1), the two opto-interrupters (OI2) and associated bias circuitry.

Two separate +5 volt supplies are used in the drive circuitry; one enters via pin 1 of A9A1/PL1 (red wire) the other via pin 2 (orange wire). The supplies are separated so that the heavy load current drawn by the motor does not effect other circuitry.

A slotted brass disc (see drawing CD-404Y1) is mounted on a shaft common to the gear train in the camera and positioned such that it activates two opto-interrupters, OI.1 and OI.2 which detect the end of the 'open shutter cycle' and the end of the 'close shutter cycle' respectively.

The camera drive waveform is a voltage step that is low for 18 secs and high for 2 secs., each 20 seconds during a scanning period. This waveform drives the base of TR1 via R1 when camera drive is initiated from the control circuitry on A5A1. The bias component R1, R2, R3 for TR1 and IC1 actually

form an output load for an open collector NAND-gate (IC1) in the Camera Drive Control Circuitry on A5A1 (see figure 3.7.4 in section 3.7). The output of this NAND-gate, pin 11 and therefore the input of the camera drive board will go low at the commencement of the 20 seconds scan period.

When the input to the camera drive board goes low, TR1 ceases conduction and its collector, and therefore the clock input to IC1 (a) goes high. The Q output IC1 (a), pin 1, originally is low but goes high causing TR2 to conduct. This will draw current through R8/R9 turning TR3 on. When TR3 conducts, its emitter current turns TR6 on. As the camera motor, M1, is the collector load of TR6, it will receive current for a period, and will commence to turn. So long as the camera drive is applied, the motor will receive current until the end of the open cycle is detected. Also at the commencement of open cycle, TR4 will conduct as its base is driven from the collector load of TR3. The collector voltage of TR4 will drop to almost zero volts and C3 will discharge rapidly via D3. The base of TR5 will be reverse biassed when this happens, thus TR5 and TR7 will remain off.

As the motor turns, the slotted brass disc also turns until the slot passes through the lower opto-interrupter OI.1 giving a positive going pulse on the reset line of IC1 (a). This causes the Q output of the J-K flip flop IC1 (a) to reset to zero and thus conduction in TR2 ceases. TR3, TR4, and TR6 will then be turned off. C3 will then charge via R15, the charging current turning TR5 and TR7 on. When TR7 conducts, it will short-circuit the motor and the back e.m.f. created by its motion, acts as an electomagnetic brake. TR5 and TR7 will remain on until C3 charges to about 4 volts. The motor is thus stopped and the camera shutter at this stage is open. During a scan, the camera shutter remains open for about 18 seconds.

The close shutter cycle is activated when the input to the camera drive board goes high to +5 volts and the J-K flip flop, IC1 (b) is clocked. The Q output, pin 15, goes high causing transistor TR2 to conduct. Consequently, the motor M1 again turns, this time to close the camera shutter. As the slot in the disc passes through the upper opto-interrupter OI.2, the resulting positive going pulse is applied to the reset input of IC1 (b) causing the Q output, pin 15, to go low and thus stop the drive to the motor via TR2, TR3 etc. The electromagnetic brake is again applied, stopping the motor. The shutter is now closed and displaced 180° from the open shutter position.

Resistor R3 connects the clock input of IC1 (b) to +5 volts so that if for some reason, the input terminal of the camera drive board is open circuited, the camera shutter remains closed. Capacitor, C4, is a supply bypass.

Advance Film

The 'advance film' push button switch is located on the camera body. When the SET terminal, pin 12 of the J-K flip flop, IC1 is taken to +5 volts the Q output, pin 15 goes high and remains high for as long as the SET terminal is placed at +5 volts. This means that the motor will be continuously driven whilst the 'advance film' switch is activated. Thus film advance is achieved.

3. 10.
POWER SUPPLIES

Par. No.	Title	Drawing No.
3.10.1	Introduction	
3.10.2	The Main Power Supply / Battery Charger	CD-247Y1A (A1)
3.10.3	Voltage Regulation	" " "
3.10.4	Current Limiting	" " "
3.10.5	The I.C. Power Supply	CD-260Y1 (A12A1)
3.10.6	The I.C. Regulators	CD-261Y1 (A12A2)

3.10.1 Introduction

There are two major power supplies in the 4A Ionosonde. These are: the MAIN POWER SUPPLY/BATTERY CHARGER, A1, and the IC POWER SUPPLY A12 A1. In addition, two series-connected, 12V lead-acid batteries may be connected to supply the ionosonde in the event of a 24V mains failure. The complete power supply system in the ionosonde involves units A1, A12 A1 and A12 A2.

The Main Power Supply/Battery Charger operates from the 240V mains, providing a nominal 28V output. It is the primary power supply to all the assemblies in the ionosonde. Following a 240V mains failure period, this supply will also recharge the batteries. It is mounted in a half-frame ISEP rack and located in the cabinet below the MONITOR DISPLAY (A10), beside the RECEIVER (A7).

The IC Power Supply is a switching regulator deriving a number of voltages for a series of eight IC regulators on A12 A2 which provide a variety of positive and negative regulated voltages for all the digital circuitry, the Frequency Synthesizer and the Receiver. It is located in the extreme left card file of the top rack assembly in the cabinet, next to the PROGRAM unit A5. The associated IC regulators (A12 A2) are located on a horizontal panel behind the card file sockets in the top rack.

3.10.2 The Main Power Supply/Battery Charger, A1.
(Dwg: CD-247Y1A)

This unit consists of a step-down transformer and rectifier combination followed by a series-pass voltage regulator. The regulator circuit employs 'fold back' current limiting to prevent damage to the regulator in the event of a heavy load or short circuit being placed on the output.

The 240V main enters via A1/PL1 and S1. A 5A fuse (FS 1) in series with the active mains lead provides protection for the transformer primary (T1) and the fan M1. The neon lamp, LP1, is mounted on the front panel and indicates when the equipment is on. The transformer, T1, steps the voltage down to about 30 V (RMS) at the secondary. An encapsulated bridge rectifier type PA40 (DB1) rectifies this, an 8000 μF capacitor, C2, providing smoothing. R1 discharges C2 whenever the power supply is turned off. Output voltage, across C2, is about 42V at no load, falling to about 32-35V under load.

The series-pass element consists of TR3 and TR1 which are two, type 2N3055, power transistors connected in a darlington configuration. The combination forms a high gain current amplifier. TR1 supplies most of the load current and thus dissipates a considerable amount of power under load. It is mounted on a large heatsink (A1A2) on the right hand side of the assembly frame. As the temperature rise of the heatsink is considerable, a fan (M1) draws air over the heatsink, exhausting through the front panel. TR3 is mounted on the printed circuit board A1A1 and has a small heatsink attached.

Two high current diodes, D2 and D5, connected in series from the collector of TR1, go to the output connections on A1/PL2. D2 prevents current flow from the batteries into the power supply circuit during a mains failure. D5 prevents damage to the ionosonde circuitry should the batteries be accidentally connected in reverse. Both D2 and D5 are mounted on the heatsink A1A2 with TR1.

As D2 is in series with the regulator output, which supplies a nominal 28V, approximately 27V is supplied to the battery. D5 is in series with D2 and thus about 26V is supplied to the ionosonde circuitry.

3.10.3 Voltage Regulation
(Dwg: CD-247Y1A)

When S1 is turned on, the rectifier provides a voltage input to the regulator circuit (terminals A-E on A1A1). Zener diode D1 will conduct via R2, forward biasing TR2. The voltage across R4 is held constant, by the action of D1, at about 9V. As TR2 drives the base of TR3, TR3 and TR1 will conduct. Thus the regulator output voltage will rise and TR4 will conduct via D3 and D4. The bias provided by R6-R7 will cause TR4 to saturate, and thus its collector current will be constant.

As the voltage across R4 is maintained constant at 9V, and the voltage across D3-D4 will be maintained at about 18.7V as D3 is a zener diode, the output voltage can not rise above the sum of these; that is: about 28V.

If the regulator input voltage increases, the collector current of TR1 will tend to rise. The diodes D3-D4 will tend to draw more current, but as the collector current of TR4 is constant, this extra current will be drawn through R4. This will reduce the emitter current available to TR2 as the voltage across R4 is constant. Thus the base current to TR3 is reduced, reducing the collector current in TR1 to compensate for the tendency for it to rise as the voltage input to the regulator circuit rises.

If the input voltage decreases, the collector current of TR1 tends to decrease. The current through D3-D4 will also tend to decrease. The emitter current of TR2 will increase as more current must flow through R4 to maintain the voltage across it constant. Thus the base current to TR3 will increase, increasing the collector current in TR1, compensating for the tendency for it to drop as the input voltage drops.

3.10.4 Current Limiting

As the load current increases, the input voltage to the regulator will decrease owing to the internal resistance of the transformer and rectifier. Eventually, a point will be reached where the collector-emitter voltage of TR1 will be so low that the darlington pair, TR3-TR1, will have insufficient current gain. At this point, voltage regulation is lost and the output voltage will drop, along with the input voltage, as the load resistance decreases. This occurs at a load current of about 8 amps and there is little increase in load current beyond this point.

When the output voltage drops below 27V, D3 and D4 cease conduction and the regulator goes into a "Constant current" mode. The collector current of TR4 will now be supplied by TR2, increasing the base current to TR3 and TR1 will maintain the output current. Any further decrease in load resistance will cause the output voltage to drop further. When it reaches about 22V, the output current will reduce, or 'foldback'. This occurs because R6 and R7 are proportioned so that at this output voltage TR4 will no longer be saturated and the collector current will decrease. Thus, the emitter current of TR2 will decrease, decreasing the base current of TR3, and therefore causing a reduction in output current.

If the output is short circuited, TR4 will cease conducting and the emitter current of TR2 will be limited by R4 to about 0.3 mA. This limits the base current to TR3 and thus the collector current of TR1, which will be a maximum of about 1A under these conditions.

A block diagram of the IC Power Supply is given in figure 3.10.2. Basically, it consists of a transistor switch which connects the 24V supply to L and C at intervals determined by the repetition rate of a pulse oscillator which drives it. The output voltage is derived across the capacitor C following smoothing which averages the ripple voltage on C. Feedback from the output to the pulse oscillator is arranged to provide a regulated output voltage of about 7V.

Each pulse from the oscillator turns the switch on, allowing the storage capacitor, C, to charge. The rising current in the inductance L, stores energy in its magnetic field. When the switch turns off, C will commence to discharge via the load, but the collapsing magnetic field in L will generate a back-emf which forward biases the commutating diode D, and

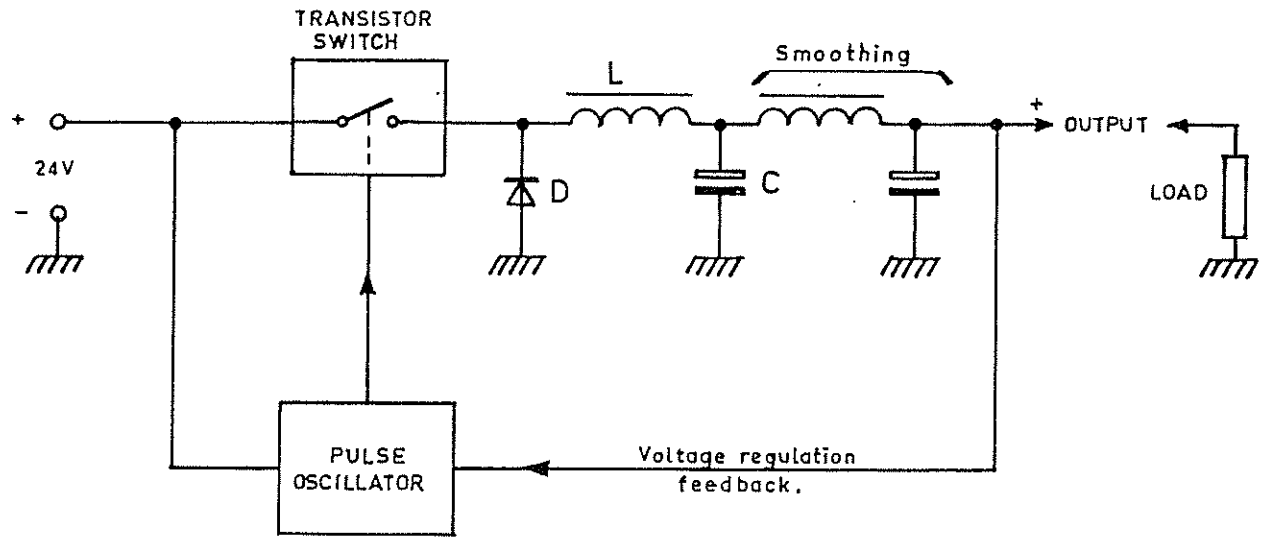


FIG. 3.10.2. Block diagram of the I.C. Power Supply.

the rising voltage across L (due to the back-emf) charging C during this period. If the pulse repetition rate (p.r.r.) is increased, less charge will be drained from C between pulses, the ripple voltage across C will decrease, and the output voltage will rise. Conversely, if the pulse repetition rate is decreased, more charge will be drained from C between pulses, increasing the ripple voltage, and the output voltage falls.

In the circuit diagram, CD-260Y1, TR5 is the switching transistor. It is driven by TR4 via a pulse transformer, T1. Pulses from the collector of TR2 drive the base of TR4. The collector current pulses of TR4 are coupled to the base of TR5 via the secondary of T1, causing TR5 to saturate for the duration of each pulse.

The inductance L, from figure 3.10.2, is provided by the primary winding of T2. The commutating diode (D) is D4, a BYX50 high speed, high current type. The storage capacitance (C) is provided by C12, a 1000 µF electrolytic. The output is smoothed by L2 and C11. The main output appears on pins 27 and 29 of A12 A1/PL1. Capacitors C13 and C14 bypass high frequency transients caused by the switching action. Three secondaries are wound on T2. These provide other output voltages which are rectified by D5, D6 and D7. These rectifier outputs provide inputs to four IC regulators on A12 A2.

Transistors TR1 and TR2, and associated circuitry, form an astable multivibrator, the pulse repetition rate of which can be varied by varying the emitter current of TR2. An increase in the emitter current of TR2 increases the p.r.r. of the oscillator, a reduction decreases it.

Control of the p.r.r. of the oscillator is provided by TR3. The emitter current of TR2 flows via R6 and the collector of TR3. Voltage regulation is obtained by feedback from the main output to the emitter of TR3 via R8 and D3. This works in the following way:-

TR3 is biased by D2 and establishes a constant current in R7. When the 24V supply is turned on, the output voltage at pins 27 and 29 of A12 A1/PL1 will, initially, be zero volts. The collector current of TR3 and thus the emitter current of TR2, will be at a maximum (about 15 mA). This forces the astable to oscillate at its highest p.r.r. causing the output voltage to rise rapidly. When it reaches about 6V, D3 will be forward biased as the emitter potential of TR3 is about 5V. Current will then flow into R7 via D3. As the emitter current of TR3 must remain constant, this will reduce the collector current of TR3, reducing the pulse repetition rate of the oscillator, slowing the rise in output voltage which stabilises at about 7V.

If the load current increases, the ripple voltage on C12 will increase, and the output voltage will tend to decrease. This will allow the collector current of TR3 to increase as less current flows into R7 via D3. The p.r.r. of the oscillator will increase, causing the output voltage to increase to compensate for the effect of the increased load current.

Similarly, if the load current decreases, the output voltage will tend to rise, increasing the current through D3 and decreasing the collector current of TR3. The p.r.r. of the oscillator will decrease, causing the output voltage to fall, compensating for the effect of the decreased load current.

Typical waveforms for the oscillator circuit are illustrated in fig. 3.10.3.

As quite high pulse currents flow when TR5 turns on, the input is heavily decoupled to prevent transients being coupled to other units via the 24V supply. Capacitors C5, C6, C7, C8, C9, C10 and the inductance L1 provide the required decoupling.

Capacitors C18, C19, C20 and C21 bypass high frequency transients that may be present on the four outputs to the associated IC regulators on A12 A2.

Both TR5 and D4 dissipate some power during the switching cycle and, to reduce their temperature rise, are mounted on a small heatsink which is bolted to the printed circuit board.

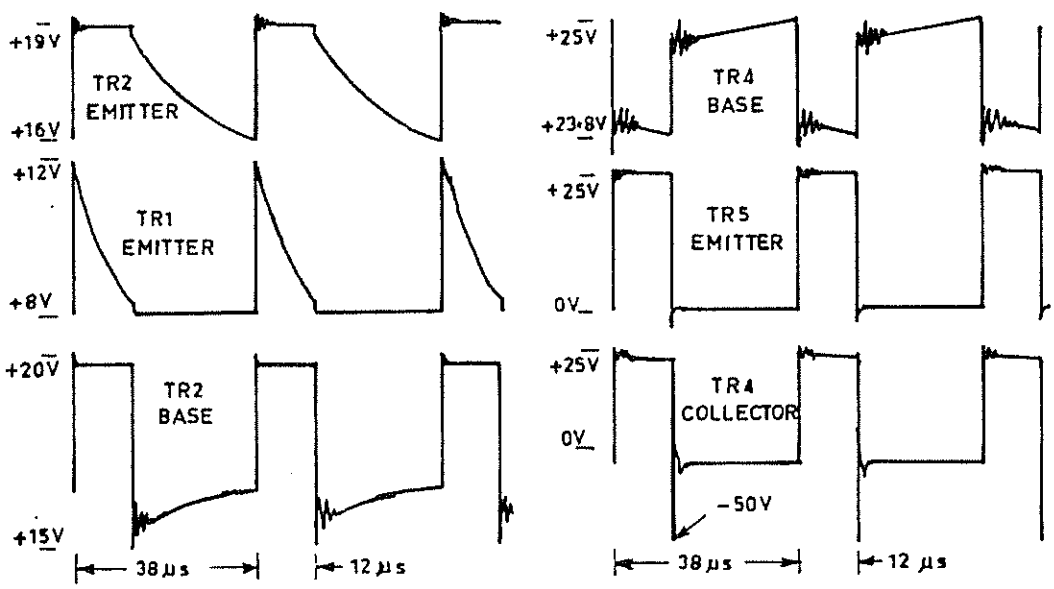


FIG. 3. 10. 3.

The output voltage versus current characteristic is illustrated in figure 3.10.1.

The ionosonde draws approximately 3 amps between soundings and about 4 amps during a sounding when the transmitter is on. Following a mains failure period, the batteries may draw an extra 4 amps or so, running the regulator into the constant current region. The battery terminal voltage may be as low as 22V following a long mains failure period, but will rise rapidly as the batteries charge, reducing the load current on the regulator which will return to a constant voltage output when the battery charging current drops below 4 amps.

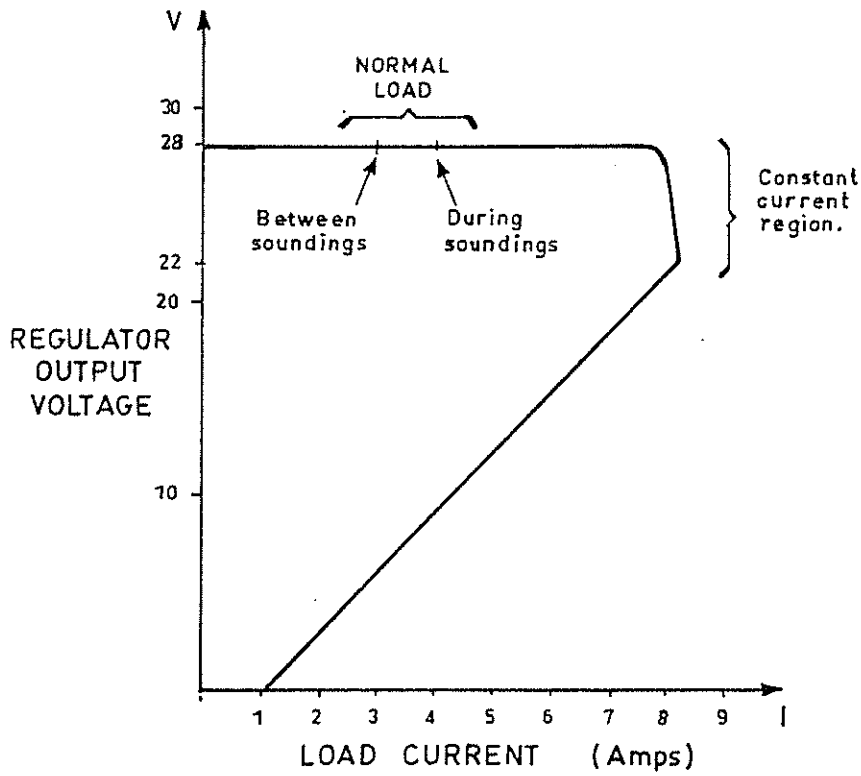


FIG. 3.10.1. Main Power Supply / Battery Charger output voltage - current characteristic.

3.10.5 The I.C. Power Supply A12 A1.
(Dwg: CD-260Y1)

This unit provides five outputs for the associated IC regulators on A12 A2. The main output is about 7V and appears on pins 27 and 29 of A12 A1/PL1. It supplies five of the IC regulators on A12 A2, these being IC1, 2 3,7 and IC8, each of which provide a regulated +5V output to various other units in the ionosonde.

The other four outputs from A12 A1 appear on pins 19, 21, 23 and 25 of A12 A1/PL1. The output on pin 23 is about +15Vand supplies IC4 on A12 A2 which provides a regulated +10V supply. Pins 19 and 25 supply IC5 on A12 A2 which is connected to provide a regulated -10V supply. Refer to section 3.10.6 for a complete description of A12 A2.

3.10.6 The IC Regulators A12 A2
(Dwg: CD-261Y1)

These are a series of eight LM309K voltage regulator IC's mounted on a horizontal panel behind the card file sockets in the top rack of the ionosonde assembly. Five of these (IC's 1, 2, 3, 7 and 8) provide regulated +5V supplies to the digital circuitry in the ionosonde, as follows:-

IC1	supplies	A3A1	- Clock, years
		A3A2	- Clock, days
		A3A3	- Clock, hours
		A3A4	- Numeral Generator
		A3A5	- Clock, seconds.
IC2	supplies	A3A6	- Master Commutation
		A3A7	- Clock, minutes
		A3A8	- Control Logic
IC3	supplies	A3A9	- Preset Program
		A3A10	- Commutation Generator
		A3A11	- Operational clock
		A3A12	- Clock, Master Osc./Divider
IC7	supplies	A4A1	- Frequency Synthesizer
IC8	supplies	A5A1	- Program Unit

The inputs to each of these IC's are paralleled and connect to the +7V output of the IC Power Supply, A12 A1 (pins 27 and 29 of A12 A1/SK1).

The other two regulator IC's IC4 and IC5, provide regulated +10V and -10V supplies respectively.

IC4 provides the +10V supply for the X and Y set-up Generators on A3A12, the RF circuitry in the Frequency Synthesizer (A4) and for all the timebases in the Program Unit A5. The +10V supply appears on pin 3 of each of the card file sockets for A3A12, A4A1 and A5A1. The +10V supply is also connected to the Receiver circuitry via A3-A5/PL1 and the wiring harness. The output to IC4 comes from the +15V output of the IC Power Supply (pin 23, A12 A1/SK1). Resistors R1 and R2 bias the reference terminal of IC4 so that the output is raised to +10V.

The input to IC5 comes from pin 19 of A12 A1/SK1, the output being grounded. The reference terminal of IC5 is biased by resistors R3 and R4, the latter returning to pin 25 of A12 A1/PL1. Thus a -10V supply is obtained. This is used in the circuitry requiring plus and minus ten volt supplies, the positive voltage being regulated by IC4.

Capacitors C1 to C11, inclusive, prevent self-oscillation in the regulator IC's.

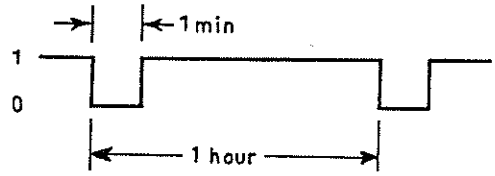
The aluminium panel, on which all the regulator IC's are mounted also provides heatsinking.

3.11.
PRESET PROGRAM

3.11 PRESET PROGRAM

The PRESET PROGRAM facility enables "selected" programs to be run by the operator. This is done through the insertion of a "PRESET PROGRAM" board, A3A9, into the slot provided in the clock and processing section. The operator then selects the PRESET position of the switch located on the PROGRAM board front panel (A5.A1). Either S1 or S2 on A5.A1 may select the PRESET board program since the MAIN display and MONITOR display are independent of each other.

A 'low' on either DISPLAY CONTROL LINE will activate a scan. The frequency of the scan and the duration of the "selected" program depends entirely on the circuitry on the PRESET board (A3.A9). For example, a program requiring three continuous soundings every hour requires the DISPLAY CONTROL LINE to go low each hour for one minute. Thus the waveform required on the DISPLAY CONTROL LINE would be:



N.B. Each scan period is 20 seconds.

"Selected" waveforms may be derived from appropriate gating of clock waveforms. In fact, two waveforms which may be used for derivation purposes are provided on pins 2 and 3 of A3.A7/PL1.

An "enabling" output, located on A5.A1/PL1 pin 23 is provided to allow gating of the "selected" program waveform through to the DISPLAY CONTROL LINES.