A Digital Single-Dish Backend for the New Triple-Band Receiver at the Metsähovi Radio Observatory

Bela Dixit, Kaj Wiik, and Talvikki Hovatta

Abstract – Aalto University's Metsähovi Radio Observatory is upgrading its 14 m radio telescope with a state-of-the-art triple-band receiver designed and built by the Max Planck Institut für Radioastronomie. This receiver enables simultaneous dual-polarization observations across K (18 GHz to 26 GHz), Q (34 GHz to 50 GHz), W1 (80 GHz to 96 GHz), and W2 (100 GHz to 116 GHz) bands, significantly enhancing sensitivity and bandwidth for single-dish astronomical studies. To complement this upgrade, we developed a cutting-edge digital backend using Radio Frequency System-on-Chip boards to digitize and process the receiver's signals. This article presents the initial development steps, including prototype implementation and simulation results.

1. Introduction

The Aalto University's Metsähovi Radio Observatory is a key facility for radio astronomical research in Finland, equipped with a 14 m radio telescope mostly dedicated to single-dish monitoring of active galactic nuclei (AGNs) and the Sun [1]. Over the years, the observatory has primarily used its 22 GHz and 37 GHz receivers, achieving significant contributions to the study of variable radio sources. However, the upcoming introduction of a state-of-the-art triple-band receiver, designed and built by the Max Planck Institut für Radioastronomie and expected to arrive in late 2025, marks a transformative phase in the Metsähovi's capabilities. This new receiver is designed to enable simultaneous observations across four wide frequency bands: K, Q, W1, and W2, each in full polarization. Each band has two linear feeds to remove the atmospheric effects via the beam differencing method. This configuration offers, to the best of our knowledge, the widest instantaneous bandwidth for single-dish radio telescopes globally. The enhanced bandwidth and sensitivity will open unprecedented opportunities for studies of AGNs and solar phenomena.

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In addition to the receiver, we need a data sampling and acquisition system that will record the data, so we are developing a cutting-edge digital polarization backend. This backend will digitize and process the radio signals from the receiver using advanced Radio Frequency System-on-Chip (RFSoC) boards, which integrate fast samplers and programmable logic. The design uses tools from the Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) [2] group, which make it easier to develop, test, and update the firmware.

This article highlights the initial steps in developing the backend, emphasizing prototype design, simulation, and testing. It presents our early results, including the implementation of a basic interleaved analog-to-digital converter (ADC) design on a ZCU111 (Gen-1) RFSoC board.

2. System Overview

The triple-band receiver's key feature is its ability to simultaneously observe dual polarizations across all three bands. This system significantly extends the observatory's observational frequency range, spanning from 18 GHz to 116 GHz. The K and Q bands are observed through common wideband linear feed horns, while the W band has its own separate feed horns. All the bands are simultaneously observing the same part of the sky. The basic principle of the receiver is the beam differencing: the two feed horns (per band) are simultaneously observing, and the signal is calculated as the difference between the two. Essentially, the frontend consists of eight individual receivers, one for each feed horn (beam) and each polarization, all having their own electronics. The separate amplifier chains require the balance between the gains to be very precisely known, because any gain imbalance will directly affect the final sensitivity at each band. This requires us to devise a careful calibration strategy.

As shown in Figure 1, the signal flow block diagram illustrates that the receiver has two downconverter stages. The first stage converts the K band to 4 GHz to 12 GHz, while the Q, W1, and W2 bands are converted to 2 GHz to 18 GHz. The second stage downconverts these IFs into two 8 GHz wide IQ basebands for ADC interleaving. Therefore, each RFSoC board handles 8 GHz of bandwidth for both X and Y polarization, resulting in a total bandwidth of 16 GHz per board.

3. Digital Backend Development

The radio signal from the receiver is digitized using RFSoC boards equipped with fast samplers. The

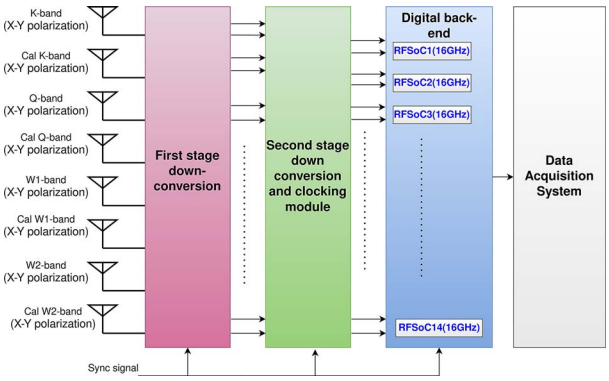

Figure 1. Signal flow block diagram. Block diagram of a triple-band extremely wideband single-dish system showing the signal flow through the first and second downconversion stages, followed by digitization and processing using 14 RFSoC modules (each module processes 16 GHz band) and data acquisition.

field-programmable gate array (FPGA) firmware calibrates the signal and calculates the polarization state of the signal using cross-correlation and autocorrelation. In Figure 2, we show the basic design of such a backend and describe in more detail in the following: 1) The RF input signal needs to be downconverted to a common IF bandwidth, which is done using an IQ mixer (Figure 2, left-hand side). However, minor phase discrepancies may arise due to imperfections in the RF mixers and analog components, which need to be corrected for during digital processing. This calibration scheme needs to be carefully assessed (step 3 in the following). 2) We use multiple ADCs to achieve higher effective sampling rates and, in this case, 16 Gsps for K band and 32 Gsps for Q, W1, and W2 band. This will be achieved using time-interleaved ADC (TIADC) techniques designed to achieve higher sampling rates by parallelizing two lower speed ADCs. Despite the advantages, TIADCs face challenges, such as channel mismatches, which can lead to nonlinearities and distortions in the combined output and also need to be calibrated. 3) A digital processing method is used to calibrate the imperfections in the downconversion and the TIADC, as shown on the right-hand side in Figure 2. With two ADC inputs, we demonstrate the benefits of ADC interleaving for increasing bandwidth in Figure 2. Following digitalization by ADCs, time domain sequences are Fourier transformed to generate frequency spectra. Subsequently, the frequency channel outputs are interleaved. This interleaved spectrum is processed using a digital hybrid method, yielding two sidebands: the upper sideband and the lower sideband [3]. By concatenating these sidebands, the full 8 GHz spectrum is reconstructed, as shown in Figure 2. This backend development further extends to process two polarizations and obtain Stokes parameters.

As part of the digital backend development, we initially simulated an 8 GHz spectrometer in Python (version 3.8.19) and Julia (Version 1.10), and a portion of it, specifically, the interleaved ADC (IADC) part, has been implemented on the Gen-1 RFSoC, as described in the following sections.

3.1 The 8 GHz Spectrometer Simulation

The 8 GHz spectrometer was simulated in Python and Julia using the IADC method, as shown in Figure 2, with tone signals at different input frequencies. Because each ADC (12 bit) has a 2 GHz bandwidth, four identical ADCs were interleaved to achieve an 8 GHz bandwidth. To replicate real-world conditions, amplitude and phase mismatches arising from hardware imperfections were incorporated into the simulation. These simulated errors, common in practical scenarios, were evaluated for the effect on the output. The left-hand side of Figure 3 displays the ideal case without mismatches, while the right-hand side illustrates the presence of multiple peaks caused by amplitude and phase errors, emphasizing the importance of robust calibration techniques to address such discrepancies [4].

These findings underscore the challenges of implementing wideband spectrometers and highlight

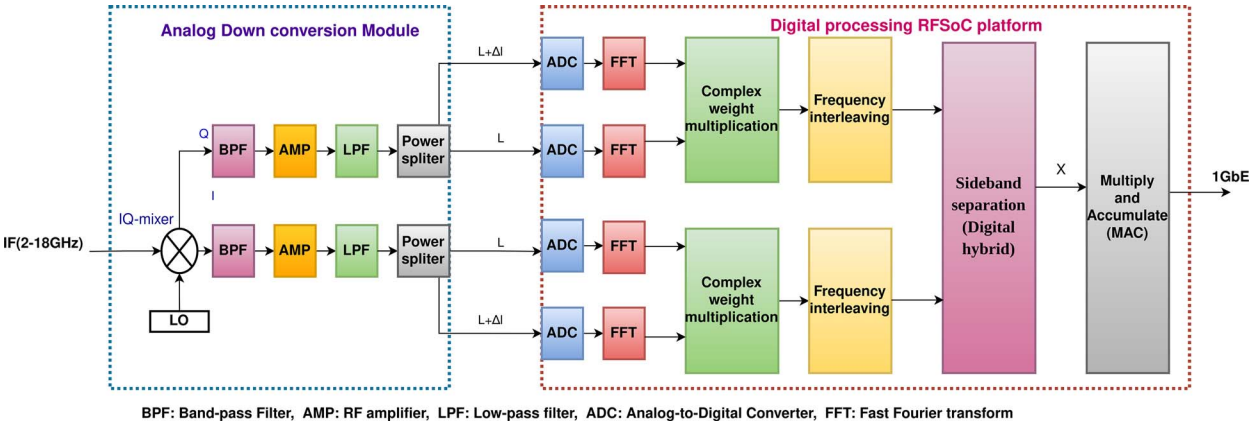

Figure 2. The 8 GHz spectrometer signal flow block diagram, with a left-hand side second-stage downconversion module, and the right-hand side is a digitizer and signal processing RFSoC platform. This is one polarization, and there will be a replica of the digital signal processing for the second polarization.

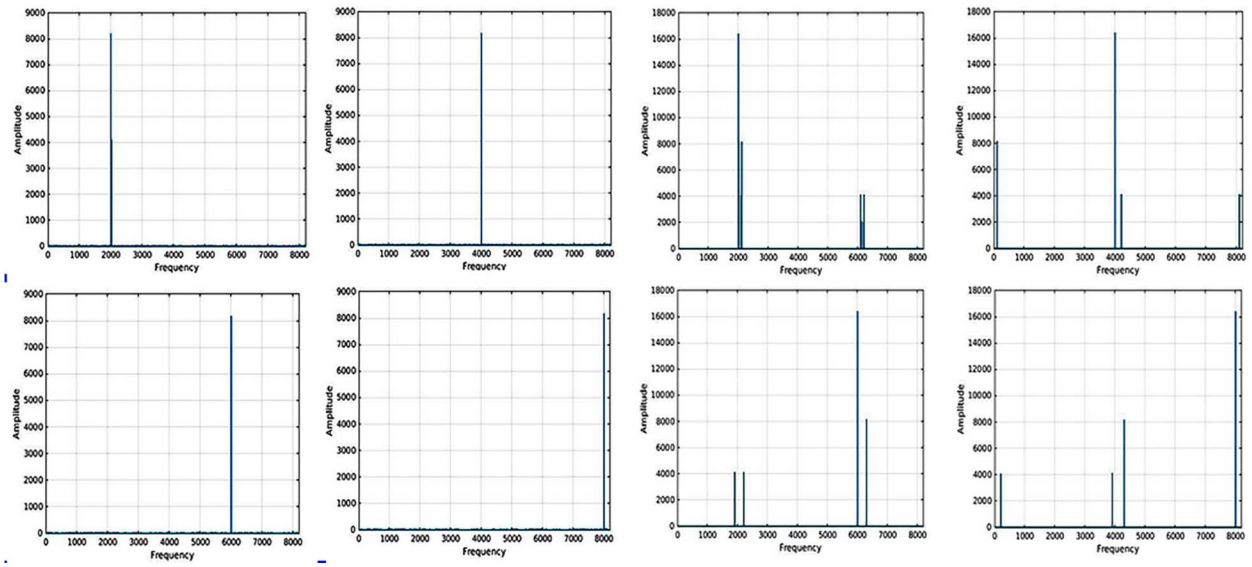

Figure 3. Left-hand side: 8 GHz spectrometer simulation amplitude (arbitrary counts) versus frequency (megahertz) plot at 2000 MHz, 4000 MHz, 6000 MHz, and 8000 MHz in the ideal case. Right-hand side: 8 GHz spectrometer simulation amplitude (arbitrary counts) versus frequency (megahertz) plot at 2000 MHz, 4000 MHz, 6000 MHz, and 8000 MHz with amplitude and phase errors. Note the difference in the *y*-axis due to amplitude errors.

the critical role of error correction in achieving accurate signal processing.

3.2 The 4 GHz Spectrometer Implementation on ZCU111

A 4 GHz spectrometer was implemented on a Xilinx ZCU111 RFSoC board, which integrates high-speed ADCs and programmable logic (FPGAs). The CASPER tool set was used for the firmware development, allowing for easy updating and testing.

The spectrometer was tested using tone signals as inputs at varying frequencies to assess its accuracy and robustness. Figure 4 shows how the signals were processed: a sine wave was created using a signal generator and then split into two identical signals with an RF splitter. One of these signals was delayed by $1/2Fs$ (where Fs is the ADC sampling frequency) using a cable length difference (Δl, in Figure 4). This approach was used to achieve IADC instead of phase shifting the ADC reference clocks. Each signal was digitized by a high-speed ADC on the ZCU111 RFSoC board, with each ADC handling a 2 GHz signal. To calibrate the ADCs, a complex weight multiplication block will be required in the frequency domain to remove amplitude and phase mismatch errors between the ADCs. Currently, we are not calibrating the ADCs, but we plan to implement this calibration in the future. By interleaving the outputs of these two ADCs, a total bandwidth of 4 GHz was achieved. The interleaved signal spectrum was then obtained using a multiply and accumulate block.

The experimental setup snapshot is shown in the left-hand side of Figure 5. Results from these experiments, shown in the right-hand side of Figure 5, revealed that each spectrum exhibited small, unintended peaks at unexpected frequencies. These spurious peaks were attributed to hardware imperfections. Such discrepancies underscore the importance of hardware calibration and compensation techniques to minimize nonidealities and ensure precise signal analysis in practical applications.

The implementation serves as a critical step in identifying and addressing these challenges for future scalability to 8 GHz bandwidth. In the future, we plan to use Gen-3 RFSoC boards, which include features such as ADC tile synchronization and external ADC clocking. We are also designing a carrier board to handle

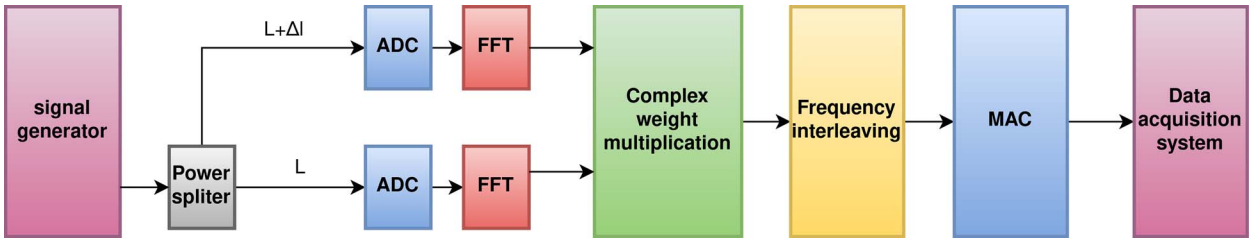

Figure 4. The 4 GHz spectrometer signal flow.

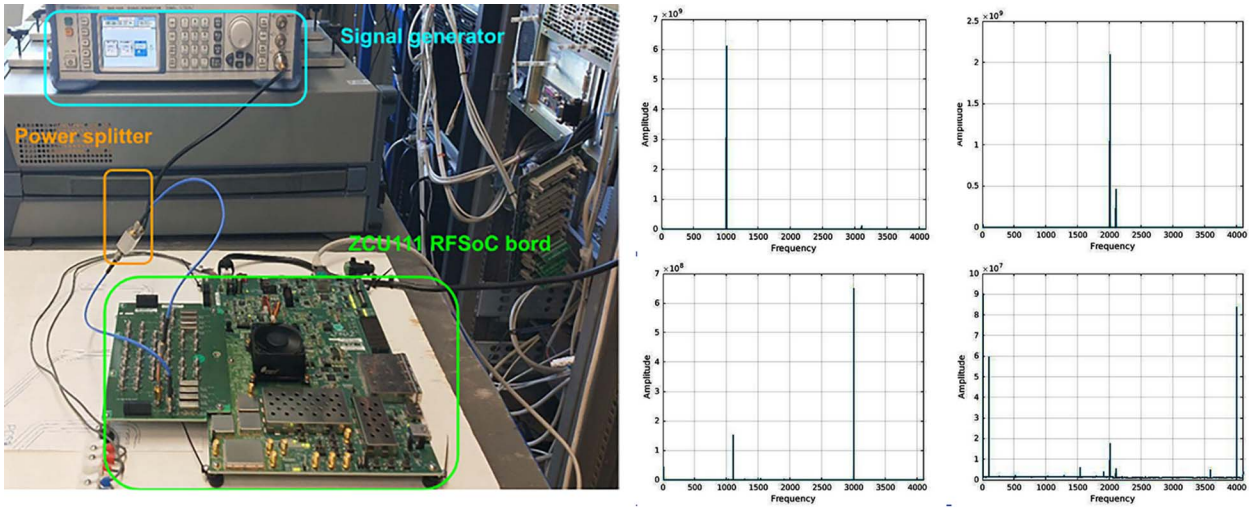

Figure 5. The left-hand side is the 4 GHz spectrometer test setup snapshot; the right-hand side is a lab test of the 4 GHz spectrometer implementation on the ZCU111 (Gen-1) RFSoC board, using tone signal inputs at frequencies of 1000 MHz, 2000 MHz, 3000 MHz, and 4000 MHz. All spectra have tone input signals and small spurious spikes.

second-stage downconversion and ADC clocking. These will be essential in reducing the phase mismatch between the ADC outputs.

4. Conclusion and Future Work

The development of a digital backend for Metsähovi's new triple-band receiver is a critical step in advancing the observatory's capabilities. Preliminary results from simulations and hardware prototypes demonstrate the feasibility of processing wideband signals, while highlighting areas for improvement, particularly in calibration and scalability. Our future work will focus on extending the prototype to process dual polarizations, integrating the backend with the receiver, and conducting on-sky tests.

5. Acknowledgments

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6. References

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