Dual-Band FET-Based Reflection Amplifier for Backscatter Modulator Performance Enhancement

Diogo Matos, Ricardo Correia, and Nuno Borges Carvalho

Abstract – This article presents a dual-band reflection amplifier (RA) based on a transistor to enhance the efficiency and range of backscatter communications. The theoretical background of RA design is provided along with the circuit design and considerations. The circuit presented in this article is capable of performing both amplitude and phase modulation at two different frequencies (2.37 GHz and 2.57 GHz) at low input power levels (–60 dBm and –50 dBm). The circuit proposed achieves a gain of 36.19 dB at –60 dBm and 35.83 dB at –50 dBm for, respectively, 2.37 GHz and 2.57 GHz. Among the works on the state of the art related to RAs based on transistors, this work presents better performance with lower DC bias power.

1. Introduction

The Internet of Things scenario is expected to have tens of billions of devices connected in the most varied networks in a near future. However, the overall structures must be concentrated to reduce maintenance periodicity and cost in order to maximize profit. Also, the increase of devices leads to a power issue, since all these devices are usually battery dependent. For this reason, some alternatives to power up and supply sensors should be found and explored.

Backscatter radio systems are a very versatile solution, which make them a very interesting topic to explore. Usually the tags establish communication with a unique or single reader and do not have energy storage capabilities. Passive tags collect power from the dedicated or ambient transmitter, which limits their use for short-range communications. The forward link is limited by the minimum amount of power needed to wake the tag and power up, and the reader sensitivity limits the return link. Thus, it is crucial to improve the link's range. Several studies have reported the use of reflection amplifiers (RA)s, which are based on an amplifier that presents a negative load impedance to amplify the backscattered RF signal with a certain bias power, to improve the communication range of these systems. There are two approaches that can be found in the literature: one using transistors [1] and the other based on tunnel diodes [2]. Tunnel diodes present better DC performance, since they achieve high gain with very low DC bias. However, most tunnel diodes operate only at low frequencies, which do not occur in some transistors—which is an advantage.

This work presents a transistor-based RA capable of operating at different frequencies depending on the DC voltage applied. Moreover, the proposed circuit requires much less DC bias power than in the state-of-the-art work, and presents the highest gain reported in transistor-based RAs. Also, the circuit can work at different levels of input power, and it allows performance of amplitude shift keying and phase shift keying at both frequencies.

This article is organized in the following sections: Section 2 gives an overview of RA theory. Section 3 introduces the circuit design and considerations. In Section 4 the measurement setup is presented and the obtained results are discussed. Lastly, some final remarks are made in Section 5.

2. Theoretical Background

Following the theory presented in [2], RAs are known and characterized by presenting a negative load impedance Z_L that is produced and can be changed by a bias voltage V_{bias}. This negative load impedance will amplify and reflect an incident RF signal with a certain power P_{in} and frequency f_{in}. With these considerations, it is possible to express Z_L as a function of V_{bias}, P_{in}, and f_{in}:

$$Z_L(f_{in}, V_{bias}, P_{in}) = -R_L + jX_L, \quad R_L > 0 \tag{1}$$

The load impedance of an RA can also be written as a function of secondary parameters, such as the device temperature. However, for now, it will not be considered. Consider an RA fully matched to an impedance $Z_A = R_A(f_{in}) + jX_A(f_{in})$ so that

$$X_A(f_{in}) + X_L(f_{in}, V_{bias}, P_{in}) = 0 \tag{2}$$

Then the DC power provided by the bias voltage will be converted into RF power that, when reflected, will be added to the original incident signal. In this process, the principle of energy conservation is preserved. Thus, the added power and gain corresponds to the negative load impedance presented by the RA that presents a reflection coefficient Γ greater than 1, and can be represented by the following equation:

$$|\Gamma|^2 = \left|\frac{Z_L - Z_A}{Z_A + Z_L}\right|^2 = \left|\frac{R_A + R_L}{R_A - R_L}\right|^2 > 1 \tag{3}$$

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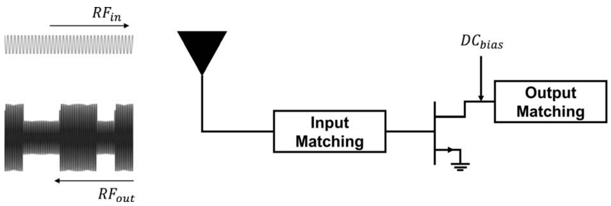

Figure 1. Block diagram of a reflection amplifier.

From (3) it is easily perceptible that by a wise choice of R_A, positive gains can be achieved. This gain is limited by the finite size of the negative resistance of the active component (tunnel diode or transistor). Additionally, the value of R_A should be carefully determined to avoid spontaneous oscillation mode in the devices. Then, as mentioned, the RA will convert the DC power into RF power, which will be added to the reflected signal by a form of injection locking. The locking RF range for a given device, designated by $2\Delta f$, is given by

$$\frac{2\Delta f}{f_{\text{in}}} = \frac{2}{Q}\sqrt{\frac{P_{\text{in}}}{P_O}} \tag{4}$$

The locking range depends on the quality factor Q of the circuit, the power level P_{in} of the incident signal, the locked power P_O, and the considered frequency f_{in}. The Δf corresponds to the one-side locking bandwidth.

3. Reflection Amplifier Design

As seen in the previous section, and more specifically in (3), the main objective is to have $|\Gamma| > 1$. However, some considerations must be followed. The reflection gain shows a value greater than 1 when the real part of the input impedance is less than zero—$\text{Re}(Z_{\text{in}}) < 0$. However, as mentioned in [2], in order to avoid the amplifier entering an oscillation state, the value of Z_{in} must be different from $-Z_L$.

The configuration or the architecture followed is the same as in [1] or [3], consisting of a common source field-effect transistor (FET) configuration in which the drain is loaded with an open circuit stub to assure that the transistor operates with $|\Gamma_{\text{in}}| > 1$. On the gate side, another open circuit stub is considered for matching purposes, as can be seen in Figure 1.

The substrate used was a Rogers RO4350B, with $\varepsilon_r = 3.48$ and $h = 0.508$ mm, and the circuit was optimized to operate between 2.4 GHz and 2.45 GHz with an input power of –60 dBm. The transistor used was a GaAs HJ-FET NE3509M04 from Renesas, resulting in the circuit presented in Figure 2

The circuit in Figure 2a, simulated and designed using Advanced Design System, produced the simulation results presented in Figure 3, which shows that for a bias voltage of 1.1 V the peak appears at 2.44 GHz, and for 0.51 V at 2.42 GHz, with respective reflection gains of approximately 24 dB and 26 dB. Figure 2b shows the produced prototype, where the left-side

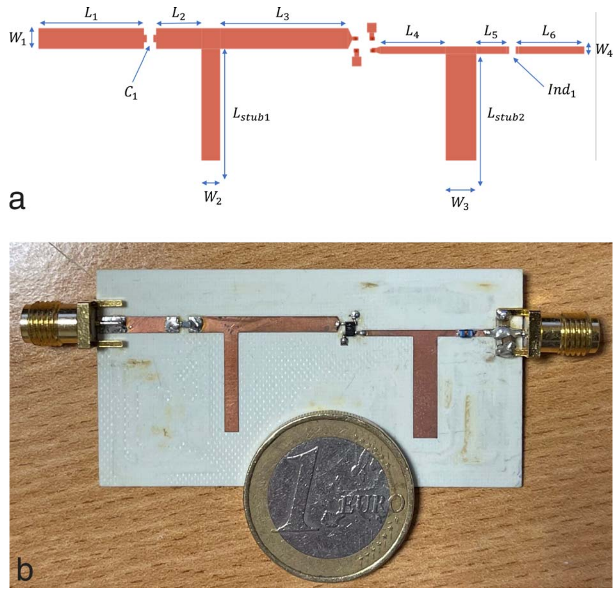

Figure 2. (a) Layout and (b) produced circuit. $W_1 = 2.24$, $W_2 = 1.84$, $W_3 = 3.34$, $W_4 = 0.8$, $L_1 = 10.8$, $L_2 = 4.81$, $L_3 = 13.65$, $L_4 = 6.78$, $L_5 = 3.09$, $L_6 = 7$, $L_{\text{stub1}} = 14.51$, $L_{\text{stub2}} = 14.09$, $C_1 = 51$ pF, $\text{Ind}_1 = 10$ nH. All dimensions are in millimeters.

connector is an RF port and the right-side connector is for DC bias purposes.

4. Measurement Setup, Results, and Discussion

To evaluate the performance of the circuit regarding its reflection coefficient (S_{11}) and phase, we considered a measurement setup composed of a performance network analyzer (PNA E8316C, from Agilent Technologies) calibrated from 2 GHz to 3 GHz for different input powers, from –60 dBm to –30 dBm and a power supply to provide the DC bias to the

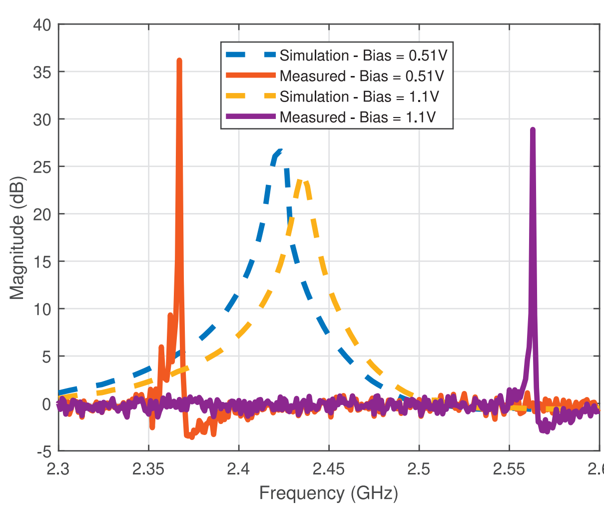

Figure 3. Simulated versus measured results with input power of –60 dBm.

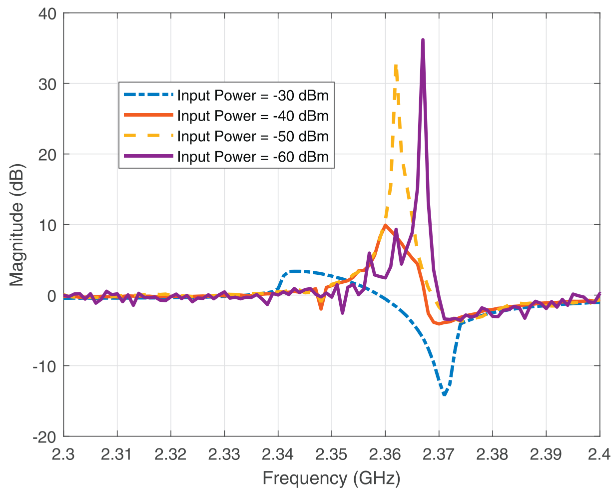

Figure 4. Power sweep analysis for 0.51 V case.

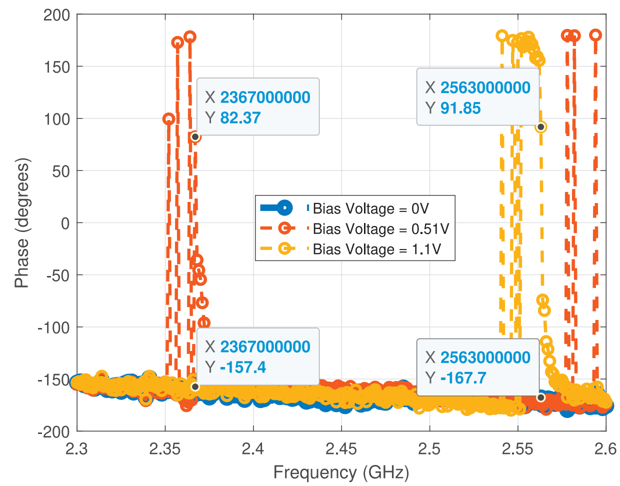

Figure 6. Phase comparison for the different bias points with input power of –60 dBm.

amplifier. In Figure 3 is possible to observe the comparison between the simulated and the measured results. From simulation to measurements a shift occurred and a reflection gain of 36.19 dB at 2.37 GHz with 0.51 V of bias and of 35.83 dB at 2.57 GHz with 1.1 V of bias was achieved. These differences can be linked to the transistor model used in the simulations, but also some error in the manufacturing and assembling process and the tolerance of the lumped elements. Nevertheless, the results obtained are very promising and allow the system to be operated as a dual-band system.

Figure 4 shows a power sweep from –60 dBm to –30 dBm for the case where the bias is 0.51 V. It is possible to see that when the input power increases, the reflection gain decreases and also has a shift to lower frequencies. Nevertheless, until –30 dBm the amplifier still shows a reflection coefficient greater than 1.

Figure 5 shows a power sweep from –60 dBm to –30 dBm for the case where the bias is 1.1 V. In this case it is possible to see that when the input power increases, the frequency shift is not that noticeable compared with the other case, and the reflection gain is higher than 15 dB at every input power value.

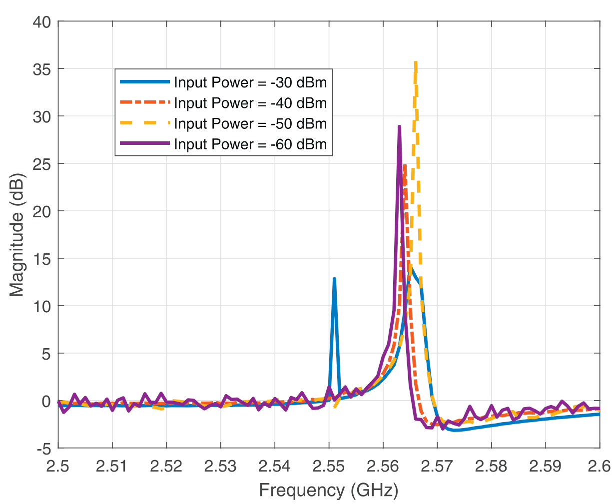

Figure 5. Power sweep analysis for 1.1 V case.

Lastly, in Figure 6 the phase is analyzed for a single value of input power (60 dBm), but with three different states of bias voltage. So if the bias voltage applied is equal to 0 V, it is possible to see that the RA presents a phase of 157.48 and 167.78 for 2.37 GHz and 2.57 GHz, respectively. When 0.51 V is applied, the phase changes to 82.48 at 2.37 GHz. When 1.1 V of bias is applied a phase of 91.98 at 2.57 GHz is achieved. With this, it is possible to perform not only amplitude modulation (the case analyzed in the previous figures) but also phase modulation, since the phase difference between each stage (not biased to biased) is considerable, making the circuit even more versatile.

The proposed circuit will increase the signal-to-noise ratio by about 35 dB to 36 dB with regard to the communication range enhancement. For example, in a traditional system at the frequency of the proposed circuit, with the transmitter/receiver 1 m away from the tag, the losses in free space are roughly 38 dB considering monopoles (1 dBi) as antennas, and the transmitted power is –50 dBm and the received power approximately –102 dBm—which is usually lower than the sensitivity of every system. Using an RA with the same transmitted power, the received power would be –40 dBm, which is a difference of 62 dB. With this it is possible to conclude that using an RA increases the communication range.

5. Conclusions

The theory, design, implementation, and measurement of a dual-band reflection amplifier are presented in this manuscript. The proposed circuit is described, along with the design considerations. Moreover, the measurements were performed for different bias voltages and power levels. For a frequency of 2.37

Table 1. Comparison of works on reflection amplifiers

Reference	Device type	DC bias power (mW)	Gain (dB)	RF input power (dBm)	Frequency (GHz)
This Work	FET	1.53 at 0.51 V	36.19	−60	~2.37
		5.5 at 1.1 V	35.83	−50	~2.57
[1]	FET	—	11.5	—	2.45
[3]		2.4	17.6	—	1.8
			16.75	—	2.4
[4]	Bipolar	0.53	29	−50	0.9
[5]		2	13	−55	5.25
[6]	pHEMT	209.3	14	−75	21

FET = field-effect transistor; pHEMT = pseudomorphic high-electron-mobility transistor

GHz and –60 dBm of input power, a gain of 36.19 dB with 1.53 mW of DC bias was achieved, and for 2.57 GHz and –50 dBm of input power, a gain of 35.83 dB and a DC bias of 5.5 mW were recorded. Nevertheless, among the state-of-the-art work in FET-based Ras, this work presents better performance, as shown in Table 1.

6. Acknowledgments

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7. References

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