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ASM-HEMT Embedding Model for Accelerated Design of PAs

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Abstract

A nonlinear embedding model for a body-grounded version of the industry standard ASM-HEMT model is presented in this paper for accelerated power amplifier (PA) design. This embedding model is able to simulate any PA mode of operation at its intrinsic reference planes and predict the impedances and harmonic terminations required at the extrinsic reference planes to sustain that targeted mode for the modeled transistor. The ASM-HEMT embedding model is further extended to account for the transistor's manifold using six-port ABCD parameters, enabling more accurate design of MMIC PAs.

1 Introduction

Today, the power amplifier (PA) designer has an extensive array of compact transistor models from which to choose. Transistor models can be based on empirical measurements, derived from analytical physical equations, or contain both empirical and physical elements. There are models for numerous different device types including MOSFETs, BJTs and HEMTs. However, most of these models share the same characteristic: simulation is done extrinsically, at the same manifold reference planes (MRF) as the physical measurement.

A nonlinear embedding model instead receives input from the circuit simulator at the current source reference plane (CSRP), also referred to as the intrinsic plane. At the CSRP, the model is simulating the ideal transistor behavior without parasitic elements and memory effects. After calculating the intrinsic IV behavior of the device, the voltage and current waveforms are embedded from the CSRP to the MRP.

Embedding models have been reported for various type of models including the Angelov model utilized in reference 1 and an artificial neural network model for SOI-MOSFET. In this conference paper, we seek to extend the embedding model to the ASM-HEMT model and verify its accuracy.

2 Concept

Transistor models are typically composed of different layers embedded concentrically within each other, with each inner layer reference plane's output connected to the outer layer reference plane's input. Moving from an inner plane to an outer plane is called *embedding*, conversely, moving from an outer plane to an inner plane is called *de-embedding*.

The innermost plane, the CSRP, is the location of the core simulation. With the specific values determined by device parameters input into the model, the behavior of the device is modeled by a voltage controlled current source. In order for the simulation at the CSRP to resemble what one would physically measure from a device, one is going to have to use models that will replicate parasitic effects inherent to the device being simulated. These effects are modeled with simple circuit elements and accounted for using basic circuit analysis. Fig. 1 illustrates a simple example of a CRSP embedded inside of an extrinsic reference plane (ERP) containing parasitic elements.

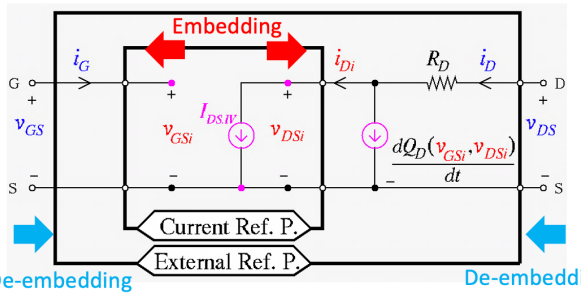

Figure 1. Simplified example of a transistor model consisting of an intrinsic model at the CRSP embedded within an extrinsic model of the device's parasitics accessed at the ERP.

The mathematical process of embedding can be seen in equations 1-3. De-embedding is simply the inverse of these equations, solving for the intrinsic value.

$$i_D = i_{Di} + \frac{dQ_D(v_{GSi}, v_{DSi})}{dt} \tag{1}$$

$$v_{DS} = v_{DSi} + i_D R_D \tag{2}$$

$$v_{GS} = v_{GSi} \tag{3}$$

This is the basic method of how a transistor model will embed or de-embed simulated data between planes throughout the entire model.

The advantage that an embedding model provides over a standard transistor model is control over the intrinsic

mode of operation of the transistor. When simulating from an extrinsic plane, the simulated current and voltage is affected by the parasitics in the intermediate planes. On a loadline these memory effects would present themselves as hysteresis that obscures the transistor's mode of operation. A comparison of an intrinsic and extrinsic loadline is presented in Fig. 2. By directly applying textbook multi-harmonic load terminations and bias to the transistor at the CSRP, one is able to control the transistor's mode of operation. From here, embedding the model's voltage and current waveforms at the CSRP will provide the transistor's voltage and current waveforms at the ERP for the chosen mode of operation. With an embedding model that accurately simulates the behavior of its physical counterpart, PA designers can then obtain the required transistor's source and load impedances, as well as necessary harmonic terminations at the ERP sustaining the desired mode of operation. This capability greatly speeds up the PA design process, as there is no need for lengthy multi-harmonic load and source-pull measurements. This method of PA design is introduced in reference 2.

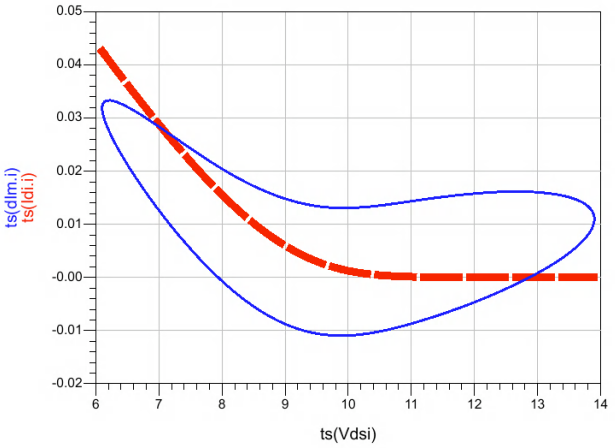

Figure 2. Comparison of a Class B loadline at the intrinsic plane (red, dashed), and the manifold plane (blue, solid) at 5 GHz.

3 Implementation

This section will summarize the modifications that were made to the ASM-HEMT model in order to implement the embedding model's functionality. Embedding models have been created for other transistor models before, but the model reported here is the first designed for the industry standard ASM-HEMT model.

The ASM-HEMT model is coded in Verilog-A, an analog circuit modeling language. The model consists of an intrinsic, or CSRP, and an extrinsic plane. There are five external nodes on the standard ASM-HEMT model: gate, source, drain, body, and temperature change (ΔT). These are the nodes that are declared as module inputs. The model also has three corresponding internal nodes only seen in the model's source code for the intrinsic gate, source, and drain, separated by access resistances. The model also has options for gate-connected and source-connected field plates, though these options will not be utilized in this paper.

To begin the process of adapting a standard transistor model to an embedding model, it is advisable to make a circuit diagram of the model, including all the parasitic elements and nodes used to model the transistor's behavior at the extrinsic plane. Such a diagram for the ASM-HEMT model is presented in Fig. 3.

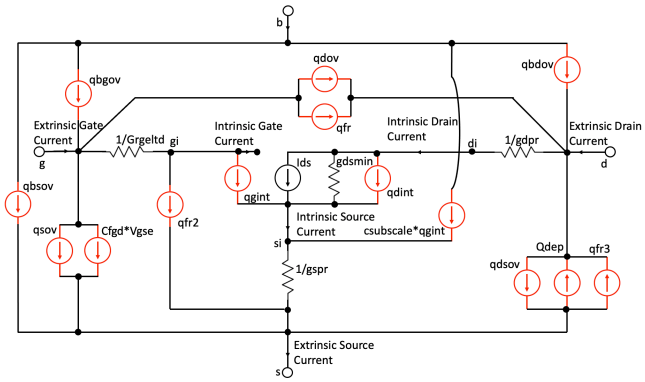

Figure 3. Topology of standard ASM-HEMT model (without field plates). Red current sources represent parasitic capacitances within the model.

After the transistor's topology and parasitics have been mapped out, it is now possible to begin coding the embedding model. Verilog-A is designed as a circuit modeling language, so this process is done very similarly to the example in section 2 of this paper. We note that for this version of the ASM-HEMT embedding model, both the body and source have been grounded, as is common for in PA design.

In addition to the mathematical embedding that is carried out in Verilog-A, there are also a number of modifications that were carried out to the model itself. Verilog-A defines nodes that interact with the software as *external nodes*. However, in an embedding model, the CSRP nodes of the model are the ones that interface with the simulation software, so the CSRP nodes for gate, source, and drain must now be declared as external nodes at the module level, and the extrinsic nodes are now removed from the module declaration and are now defined as *internal nodes.* The extrinsic currents and voltages calculated via embedding for both the gate and drain are assigned to four separate external nodes.

Once the necessary modifications have been made to the model's code, the embedding model's output must be verified to match the standard model's input.

4 Verification

At this juncture it is important to reiterate that an embedding model does not affect behavior or performance of the original model. The embedding model is simply allowing the simulation software to access the model's internal plane.

Therefore, the behavior at the extrinsic output of the embedding model can be compared to the extrinsic input of the standard model. This can be done simply by modifying the standard model to *de-embed* to the intrinsic plane. This model will function exactly the same as the normal model, except for the addition of extra external nodes in the Verilog-A code that are assigned the calculated current and voltages of the gate and drain at the intrinsic node. In the simulation, the output data from this de-embedding model is sent to the intrinsic plane input of the embedding model. This creates a chain of accountability: the modified standard model's extrinsic input is de-embedded to the intrinsic plane, then the de-embedded data is sent to the intrinsic input of the embedding model, which is then embedded in the same extrinsic plane as the standard model. If the embedding model is functioning properly, the output at the extrinsic reference planes should equal the inputs of the standard model exactly.

Fig. 4 contains time-domain plots of the extrinsic source-drain voltage and drain current from the simulation described above. These curves completely overlap, indicating that our embedding model is accurately embedding the intrinsic plane within the same extrinsic plane as the standard model.

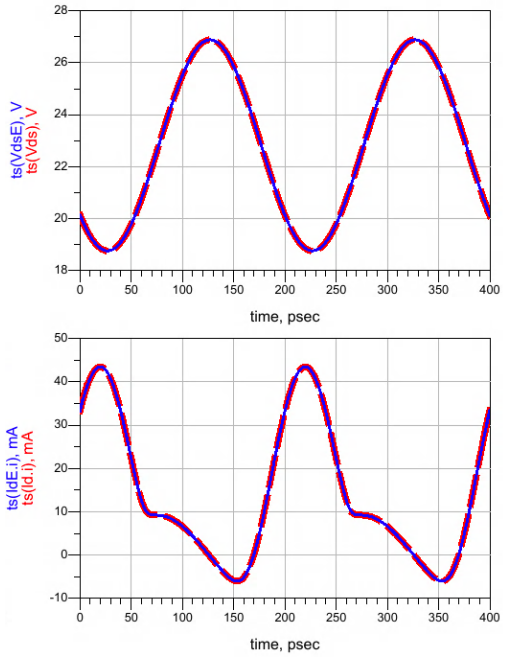

Figure 4. Time domain measurements of a Class B simulation at 5 GHz for drain current and source-drain voltage at the embedding plane. The blue, solid line is the embedding model's output and the red, dashed line represents the standard model's input.

5 Simulating the Manifold Plane

While the ASM-HEMT model is proficient at modeling the behavior of a GaN HEMT to the extrinsic plane, there are parasitics that arise from the manifold of the transistor that, if included in the simulation, will further replicate the measured behavior of the device. However, the ASM-HEMT model does not natively include a manifold plane, so the manifold plane simulated in the simulation software.

The manifold is represented in simulation software as a passive network of lumped components, so it is possible to model the manifold with small-signal parameters. The manifold has six ports: extrinsic gate, source, and drain and manifold gate, source and drain. Since the output from the embedding model is in the form of currents and voltages, the manifold is modeled with a 6x6 ABCD matrix. However, most modeling software will not simulate a circuit's ABCD matrix, so it must be converted to T-parameters, then ABCD parameters using equation 4 from reference 3 and equations 5-8 from reference 4.

$$[T] = \begin{bmatrix} [S_{em}]^{-1} & -[S_{em}]^{-1} \cdot [S_{ee}] \\ [S_{mm}] \cdot [S_{em}]^{-1} & [S_{me}] - [S_{mm}] \cdot [S_{em}]^{-1} \cdot [S_{ee}] \end{bmatrix} \quad (4)$$

$$[A] = \frac{Z_{0m}^{*}([T_{mm}] + [T_{me}]) + Z_{0m}([T_{em}] + [T_{ee}])}{2(R_{0m} * R_{0e})^{1/2}} \quad (5)$$

$$[B] = \frac{Z_{0e}^{*}([T_{mm}] \cdot Z_{0m}^{*} + [T_{em}] \cdot Z_{0m}) - Z_{0e}([T_{me}] \cdot Z_{0m}^{*} + [T_{ee}] \cdot Z_{0m})}{2(R_{0m} * R_{0e})^{1/2}} \quad (6)$$

$$[C] = \frac{[T_{mm}] + [T_{me}] - [T_{em}] - [T_{ee}]}{2(R_{0m} * R_{0e})^{1/2}} \quad (7)$$

$$[D] = \frac{Z_{0e}^{*}([T_{mm}] - [T_{em}]) - Z_{0e}([T_{me}] - [T_{ee}])}{2(R_{0m} * R_{0e})^{1/2}} \quad (8)$$

Where S_{mm}, S_{me}, S_{em}, S_{ee} are defined as 3x3 submatrices of the total 6x6 matrix as seen in equation 9.

$$[S] = \begin{bmatrix} [S_{mm}] & [S_{me}] \\ [S_{em}] & [S_{ee}] \end{bmatrix} \quad (9)$$

Equation 10 is then implemented in circuit form, as seen in Fig. 5.

$$\begin{bmatrix} V_{gm} \\ V_{dm} \\ V_{sm} \\ I_{gm} \\ I_{dm} \\ I_{sm} \end{bmatrix} = \begin{bmatrix} A_{gg} & A_{gd} & A_{gs} & B_{gg} & B_{gd} & B_{gs} \\ A_{dg} & A_{dd} & A_{ds} & B_{dg} & B_{dd} & B_{ds} \\ A_{sg} & A_{sd} & A_{ss} & B_{sg} & B_{sd} & B_{ss} \\ C_{gg} & C_{gd} & C_{gs} & D_{gg} & D_{gd} & D_{gs} \\ C_{dg} & C_{dd} & C_{ds} & D_{dg} & D_{dd} & D_{ds} \\ C_{sg} & C_{sd} & C_{ss} & D_{sg} & D_{sd} & D_{ss} \end{bmatrix} \cdot \begin{bmatrix} V_{ge} \\ V_{de} \\ V_{se} \\ -I_{ge} \\ -I_{de} \\ -I_{se} \end{bmatrix} \quad (10)$$

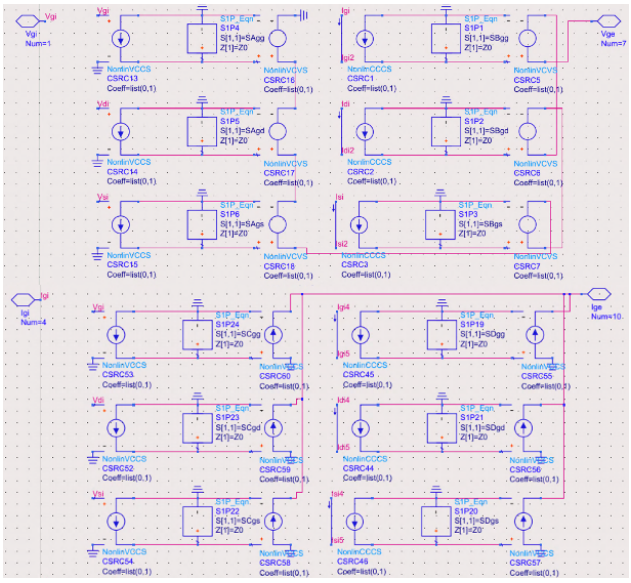

Figure 5. Circuit implementation of matrix multiplication in equation 10. Circuits for V_{gm} and I_{gm} are shown.

Similarly to section 4, the embedding model connected to an ABCD matrix must also be validated against the standard model connected to the simulated manifold. This is done in the same manner as in section 4, and the results are seen in Fig. 6.

Modeling the manifold with a 6x6 ABCD matrix perfectly replicates the simulation of the manifold, allowing the embedding model to be used with an external manifold separate from the Verilog-A code.

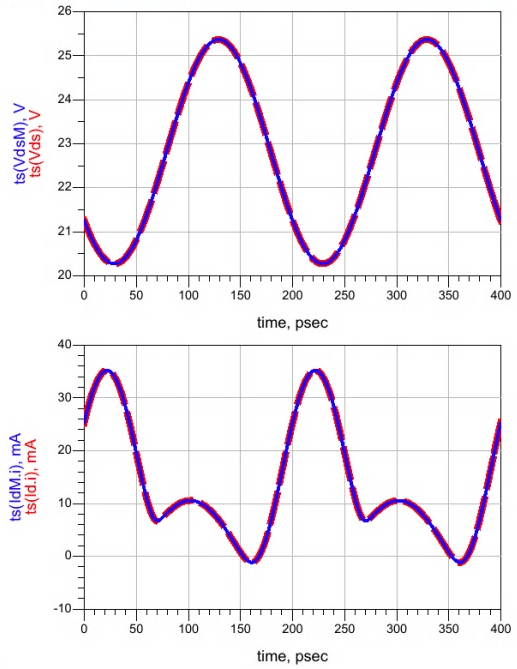

Figure 6. Time domain drain current and source-drain voltage measurements of a Class B simulation at 5 GHz. The blue, solid line is the embedding model's output with the ABCD representation of the manifold plane and the red, dashed line represents the standard model's input through the manifold's simulated circuit.

6 Conclusion

In this conference paper, we reviewed the underlying concept and motivations behind nonlinear embedding and its use in transistor models. We detailed the modifications that must be made to the standard model in order to transform it into an embedding model. We also explained the process that was used to add a manifold plane further outside the extrinsic plane using simulation software and parameter conversion.

Embedding models have been made for other transistor models, but it is especially useful to have an embedding model for a physical model like the ASM-HEMT. The ASM-HEMT model allows for more granular control over physical parameters like gate length, width, number of gate fingers, barrier thickness, etc. The control afforded by a physical model combined with the operative control that the embedding model gives not only greatly increases the speed at which PA designers are able to complete their designs but also reveals the impact of the physical device parasitics on the device performance for the targeted mode of operation at the CSRP.

7 References

1. H. Jang, P. Roblin, and Z. Xie, "Model-Based Nonlinear Embedding for Power-Amplifier Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 9, pp. 1986–2002, Sep. 2014, doi: 10.1109/TMTT.2014.2333498.

2. A. Raffo, F. Scappaviva, and G. Vannini, "A New Approach to Microwave Power Amplifier Design Based on the Experimental Characterization of the Intrinsic Electron-Device Load Line," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 7, pp. 1743–1752, Jul. 2009, doi: 10.1109/TMTT.2009.2022816.

3. T. Reveyrand, "Multiport conversions between S, Z, Y, h, ABCD, and T parameters," in *2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC)*, Jul. 2018, pp. 1–3, doi: 10.1109/INMMIC.2018.8430023.

4. D. A. Frickey, "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205–211, Feb. 1994, doi: 10.1109/22.275248.