Evaluation of Microwave Transistor Degradation Using Low-Frequency Time-Domain Measurements

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Abstract

We present a measurement technique for the characterization of the degradation in microwave transistors. The time-domain setup operates in the megahertz range to set a realistic load-line for the device. Data on the degradation of a microwave transistor are reported.

2 Introduction

The development of new microwave technologies requires a proper evaluation in terms of performance and reliability, to investigate the device robustness and guide their design to further improvements.
To this aim, DC stress measurements are commonly adopted to test device response to high-field conditions [1], though do not implement a realistic operation regime for the transistors. From this perspective, stress tests under RF excitations are surely more suitable [2] but may require expensive instrumentation and do not allow a clear view of some of the electrical quantities directly related to device degradation, e.g., the Schottky junction conduction regime in HEMT devices.
In this work, we adopt the low-frequency (LF) measurement setup described in [3] for the evaluation of the performance degradation in a microwave transistor. It consists of a time-domain load-pull setup, operating in the megahertz range, composed by low-cost general-purpose instrumentation. By operating at LF, it allows neglecting the influence of the reactive phenomena of the device, providing the intrinsic electrical variables at the current-generator plane, as well as some important parameters directly related to the device degradation phenomena, such as the resistive gate current waveform [4]. The operating frequency above the cut-off of LF dispersion [3] allows the collection of data representative of the device microwave behavior.

2 Experiment Description

The LF load pull setup has been adopted for the evaluation of the degradation of a microwave HEMT device. We considered a class-F stress condition with a quiescent bias point at V_{DQ} = 10 V and I_{DQ} = 12.5 mA/mm. The load impedance was synthesized with a passive termination to 17.2 Ω·mm at the fundamental frequency of 2 MHz, whereas 2nd and 3rd harmonics were properly terminated according to class-F theory. Under this condition, the device provided an initial output power of 2.45 W/mm with an efficiency of 75.8 %. The stress condition has been applied for a total time of 234 hours, according to the sequence summarized in Fig. 1.

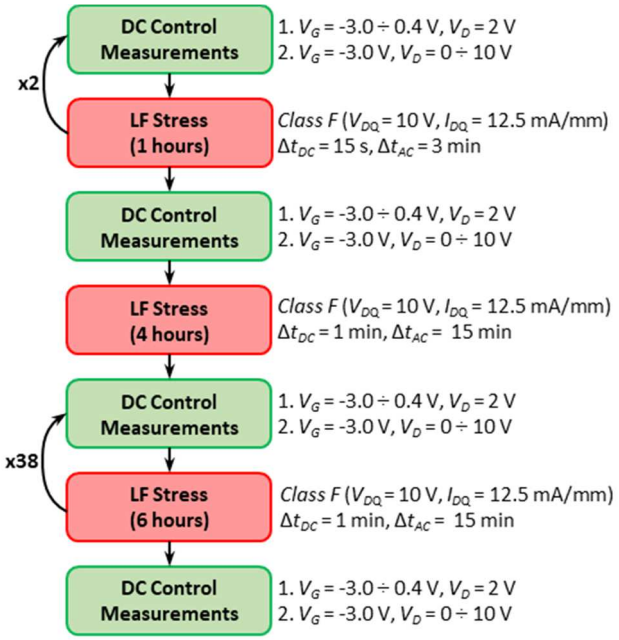

Figure 1. Measurement procedure adopted for the experiment. Δt_{DC} and Δt_{AC} are the sampling times for the DC and AC quantities adopted during each stress session.

The entire stress procedure has been divided into several sessions, whose duration and data sampling times have been set according to the expected rate of degradation of the transistor. Some DC control measurements have been interleaved between the stress sessions to monitor the degradation progression over different parameters, i.e., the I_D-V_G and I_G-V_D trans-characteristics.

3 Measurement Results

In Fig. 2, we report the load line evolution during the stress. The reduction of the maximum current and the increase of the knee voltage due to the device degradation is clear. It results in the reduction of the output power delivered by the transistor, as reported in Fig. 3. From the initial 2.45 W/mm, the output power decreases to about 2.1 W/mm, with a reduction of 14.2 %. In Fig. 4, we report the

average gate current measured during the LF stress. The sensibility of this parameter to the device degradation is highlighted by the large variation of its value. Starting from an initial value of -0.16 mA/mm, it reaches -1.61 mA/mm after the 234-h stress, with an increase (in magnitude) of more than 900%. Such a large change can be explained by looking at the gate current waveform evolution during the measurement in Fig. 5. This quantity, directly accessible as a result of the LF operation, shows the reverse conduction of the Schottky junction, which becomes more and more pronounced as the degradation of the transistor increases.
In Fig. 6, we report the DC drain current at V_G = 0 V and V_D = 2 V monitored using the control measurements. The variation of this parameter agrees with the previous results, showing a reduction from 782 mA/mm to 748 mA/mm (-4.3 %).

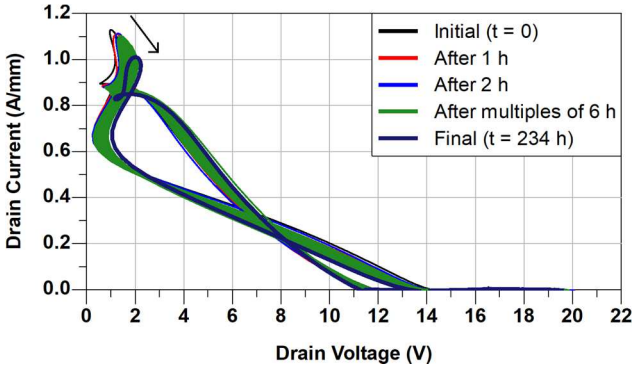

Figure 2. Evolution of the load line during the stress measurement. The arrow indicates increasing time.

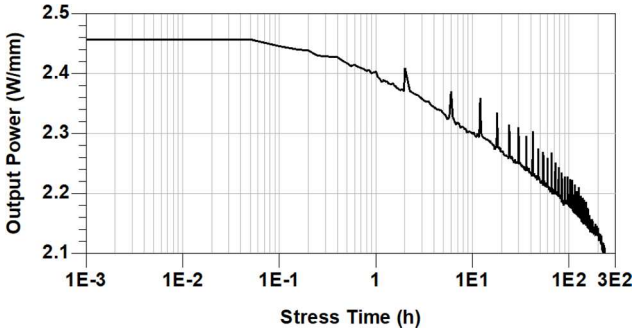

Figure 3. Output power measured during the LF stress procedure.

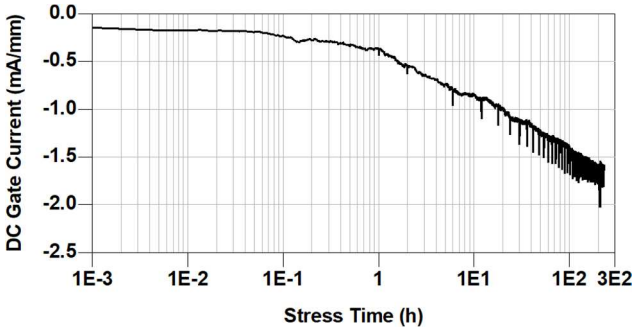

Figure 4. Average gate current measured during the LF stress procedure.

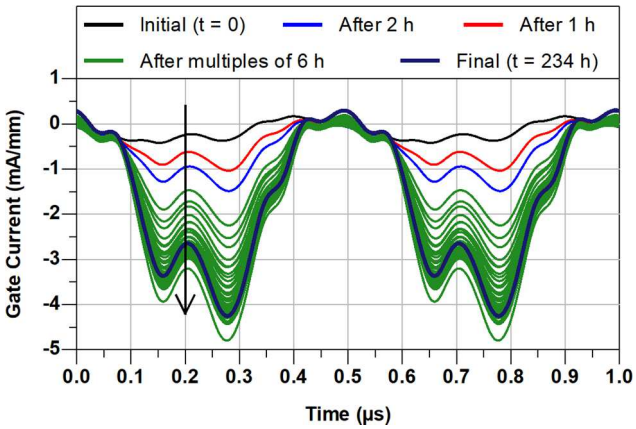

Figure 5. Evolution of the gate current waveform during the LF stress measurement. The arrow indicates increasing time.

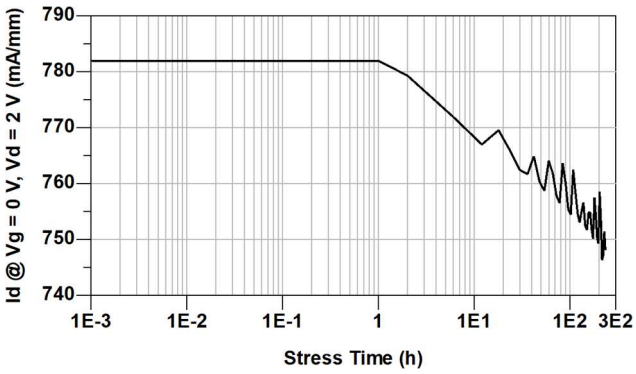

Figure 6. Variation of the DC drain current at V_G = 0 V and V_D = 2 V.

4 Conclusions

We have used a LF time-domain load-pull setup for characterizing the degradation of a microwave transistor. The capabilities of the setup allow an accurate analysis of the device degradation under realistic operating conditions by monitoring parameters hidden when using other measurement techniques.

6 Acknowledgements

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5 References

1. W. Sun, C. Lee, P. Saunier, S. A. Ringel, and A. R. Arehart, "Investigation of trapping effects on AlGaN/GaN HEMT under DC accelerated life testing," *IEEE Int. Rel. Physics Symp.*, 2016, pp. CD-3-1-CD-3-6.
2. A. Chini, V. Di Lecce, M. Esposto, G. Meneghesso, and E. Zanoni, "RF degradation of GaN HEMTs and its correlation with DC stress and I-DLTS measurements," *Eur. Microw. Integrated Circuits Conf.*, 2009, pp. 132-135.
3. A. Raffo, G. Bosi, V. Vadalà and G. Vannini, "Behavioral modeling of GaN FETs: a load-line

approach," *IEEE Trans. Microw. Theory Techn.*, **62**, 1, January 2014, pp. 73-82.
4. A. Raffo, et al., "Analysis of the gate current as a suitable indicator for FET degradation under nonlinear dynamic regime," *Microelectronics Reliability*, **51**, 2, February 2011, pp. 235-239.