

Design and realization of NavIC Timing receiver for precise ground applications

Suresh Dakkumalla*, Rajath Sadasivan, Prem Ranjan Dubey, Aakanksha Avnish Bhardwajan, Akash B, and T Subramanya Ganesh

ISRO Telemetry Tracking and Command Network, Peenya, Bangalore-560058

Abstract

A timing receiver is a specialized receiver which solves and provides for time. A dual-band (L5 and S1) NavIC receiver for precise timing applications has been designed, developed and realized. This development includes the design of a RF front end circuit and an AGC which carries out the signal conditioning and down conversion of the NavIC RF signals to IF. The baseband circuit, based on Xilinx FPGAs, carries out the demodulation of the navigation data after the CDMA signal is recovered from noise through narrow correlator technique. Acquisition and tracking loops have been implemented in the digital portion of the receiver. One of the novel features of the receiver is the use of a Kalman filter based steering algorithm to steer the internal oscillator to the NavIC system time, hence producing precise and stable timing outputs with just a Rubidium oscillator inside the receiver. The performance of the receiver is comparable to the existing GNSS based timing receivers.

1 Introduction

Navigation with Indian Constellation (NavIC) is a regional satellite navigation system based on seven GSO satellites and broadcasts civilian navigation signals in dual band, i.e. L5 and S1. The reference time for NavIC network is generated through an ensemble of highly precise and stable ground atomic clocks which is also traceable to UTC (NPLI) or Indian Standard Time. The accuracy and stability of the ground based timing facility is realized by a receiver on ground through the navigation signals.

There are several ground applications which require accurate time and frequency traceable and synchronized to a standard reference, such as UTC. Such applications include, but are not limited to, TTC ground stations for LEO satellites, power grids, financial sector and logistics network. At present, in India, all these areas employ GPS based receivers to achieve the level of accuracy needed in their respective areas.

Meeting these requirements is a timing receiver, a specialized receiver, which solves and provides for time. This receiver is different from a positioning receiver since unlike a positioning receiver, a timing receiver generally

knows its position very accurately and has to solve only for time.

A NavIC Timing Receiver has been designed and developed which supports precise timing requirements without the need for an expensive atomic clock. This receiver processes the raw pseudoranges to obtain the receiver clock offset with respect to the NavIC system time. It, then, employs a suitable steering algorithm to steer the internal oscillator to the NavIC system time such that the difference between the NavIC system time and the time generated by receiver is better than 40 ns (2σ) for any yearly time interval. This accurate output is available in various formats such as 10 MHz, 1 PPS, IRIG and NTP. [1]

This paper dwells on the design and development aspects of a NavIC based Timing receiver. The authors have been able to achieve comparable performance with the similar GNSS based receivers available in the industry.

2 Building blocks of NavIC Timing receiver

The receiver can be divided into the following major blocks:

- Antenna and antenna subsystem (out of the scope of this paper)
- Dual-band RF to IF Down converter circuit
- Baseband Processor circuit and firmware

Figure 1 depicts the top-level diagram of the receiver.

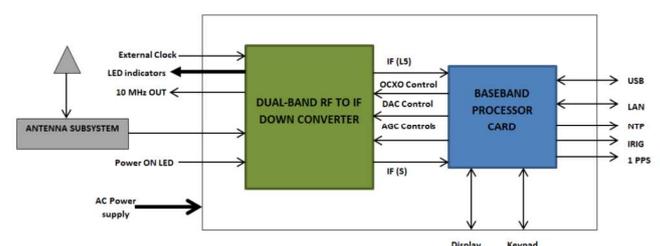


Figure 1. Top level block diagram of NavIC Timing receiver

2.1 Dual-band RF to IF Down converter circuit

The NavIC signals are buried under the thermal noise floor. The dual-band RF front end circuit is responsible for the signal conditioning and down-conversion to IF

level in order for a faithful Analog-to-digital conversion by the ADC. An Automatic Gain Control (AGC) circuit ensures that any change at the antenna input does not affect the input to ADC. In other words, AGC decides the quantization levels of the ADC by maintaining the ratio between the maximum quantization threshold and standard deviation of noise. Three bits of ADC output are used for further processing by the digital output.

Figure 2 shows the top-level building blocks of the RF front end.

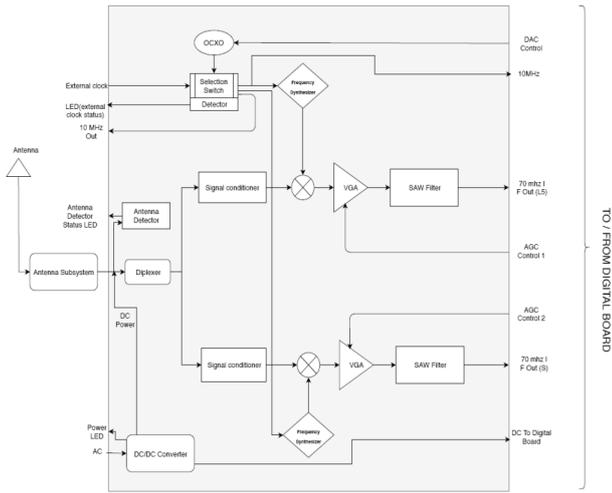


Figure 2. RF to IF down converter circuit

2.2 Baseband processor circuit and firmware

The digital card has been designed using a Xilinx family FPGA and SOC chips. The acquisition and tracking loops have been implemented in the baseband processor card [2, 3, 4]. Figure 3 and 4 depict the simulation outputs of acquisition and tracking loops implemented for the NavIC Timing receiver.

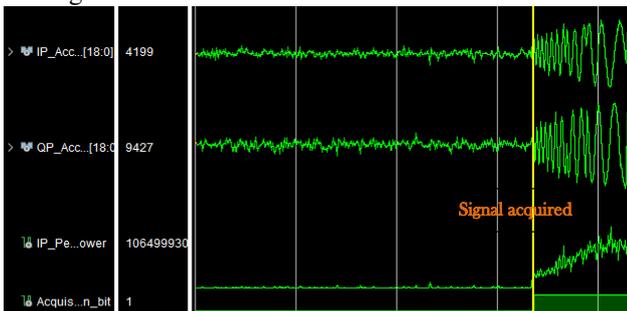


Figure 3. Output of acquisition loop

The digital part is also responsible for the data demodulation, measurement generation, carrier-to-noise computation [5] and realization of system time. Once the system time is realized, the phase and frequency offset of internal oscillator is computed and the receiver calculates the command values for the oscillator. Lastly, the receiver generates the logs and measurement files needed by the

user. The firmware of the receiver has been written in VHDL and C.

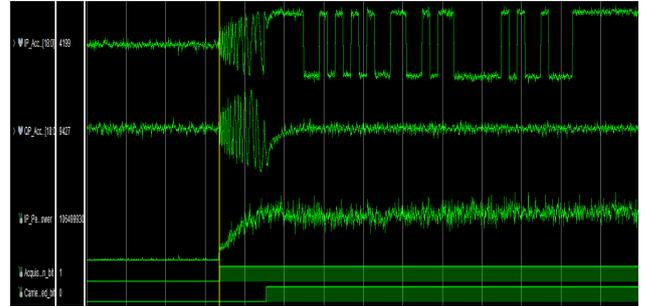


Figure 4. Output of tracking loop

3 Performance specifications

The receiver was designed with the following specifications as target:

- Realizing the NavIC System Time with an accuracy of 40 Nano-seconds (2σ).
- The accuracy of time offset measurements shall be better than 5 nanoseconds.
- The short term stability of the frequency output shall be better than $5e-12$ Allan Deviation (ADEV).
- The long term stability of the frequency output shall be better than $8e-15$ ADEV.

4 Features of NavIC Timing receiver

The following features have been implemented in the receiver to increase the robustness of the receiver:

- Capability to load a new PRN code into the receiver. This capability is especially useful as NavIC constellation is expected to expand in future. This feature ensures that firmware upgrade is not required in case of any addition or deletion of a satellite into the constellation and such events can be handled by a simple user configuration.
- Kalman filter based steering algorithm. This algorithm also known as Linear Quadratic Gaussian (LQG), maintains an optimal balance between the accuracy and stability of the final output.
- Configuration as a Time transfer receiver. The receiver has been designed in such a way that it can easily be configured as a time transfer receiver. This too does not call for a firmware upgrade and only a configuration change.

5 Achieved performance

The receiver was evaluated on two major specifications, namely, ADEV of the output signal and the offset of 1PPS

generated by the receiver and the NavIC PTF. The results are shown in Figure 5 and 6.

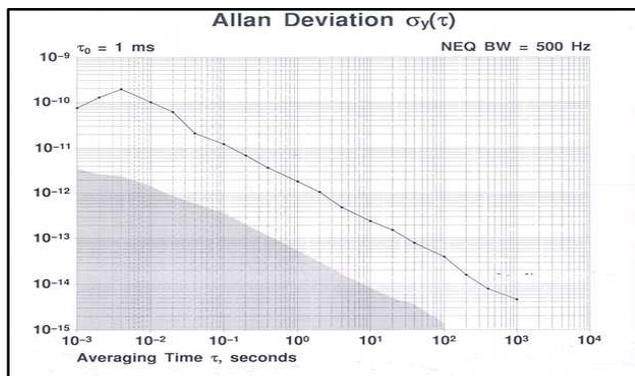


Figure 5. Allan deviation of 10 MHz output of NavIC Timing receiver

As can be seen from Figure 5, the receiver exceeds the specifications of frequency stability in both short term and long term.

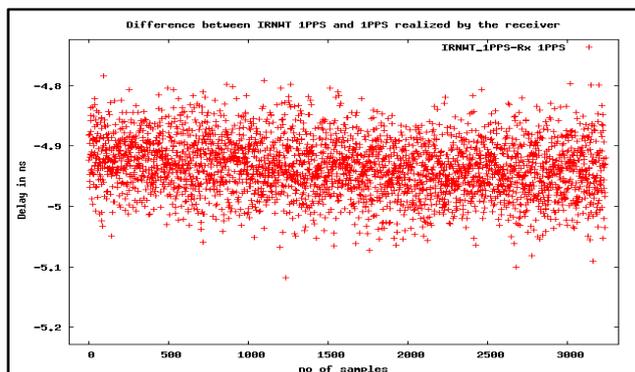


Figure 6. Offset between 1PPS realised by NavIC receiver w.r.t NavIC system time

The absolute mean offset between receiver generated time and NavIC system time was 5 ns with a standard deviation of 0.2 ns.

6 Acknowledgements

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