Abstract

The ‘TALON’ architecture has been proposed by Canada’s National Research Council (NRC) for the SKA Phase 1 Square Kilometre Array (SKA1) ‘Mid’ telescope. It is required for the Square Kilometre Array (SKA) correlated data stream to be reduced to a much smaller bandwidth stream, containing raw antenna visibilities for the mid-frequency sub-bands. The capability includes processing up to 20 samples per second, handling 16 such streams. The architecture targets unprecedented processing requirements of the SKA1_Mid Correlator & Beamformer (CBF) segment of the SKA1 ‘Mid’ telescope. The TALON line contains 16 TALON LRUs and 8 SX LRUs for the SKA1 ‘Mid’ telescope, with each LRU consisting of one Intel Stratix 10 FPGA, 26 DDR4 DIMM modules, 4 100GE QSFP28 ports and 48 GB/s bi-directional optical channels. The hardware, firmware, software and power and cost were designed to meet requirements of the SKA1_Mid.CBF segment.

1. Introduction

The ‘brain’ of the SKA is the SKA radio telescope, where the SKA ‘Mid telescope’ hosts the SKA1_Mid Correlator & Beamformer (CBF) segment of the SKA1 ‘Mid’ telescope. The CBF segment is responsible for generating the antenna visibility data for the input bands, which is then fed into the SKA Data Processing System (DPS) for further analysis.

2. The TALON Architecture

The TALON architecture has been proposed by Canada’s National Research Council (NRC) for the SKA Phase 1 Square Kilometre Array (SKA1) ‘Mid’ telescope. It is required for the SKA’s correlated data stream to be reduced to a much smaller bandwidth stream, containing raw antenna visibilities for the mid-frequency sub-bands. The TALON architecture targets unprecedented processing requirements of the SKA1_Mid Correlator & Beamformer (CBF) segment of the SKA1 ‘Mid’ telescope. The TALON line contains 16 TALON LRUs and 8 SX LRUs for the SKA1 ‘Mid’ telescope, with each LRU consisting of one Intel Stratix 10 FPGA, 26 DDR4 DIMM modules, 4 100GE QSFP28 ports and 48 GB/s bi-directional optical channels. The hardware, firmware, software and power and cost were designed to meet requirements of the SKA1_Mid.CBF segment.
Figure 1. A simplified version of the TALON Engine architecture for SKA1-Mid.CBF. This diagram shows the distribution of channelized data for V/LBIs, PSS and PST beamforming, and imaging. The channelized data is distributed to the MX LRU, with each TALON LRU handling 1/32 of the total bandwidth. Note that some functionality is embedded in each of the FPGAs in the MX LRUs. This is the first stage of the processing. For all observing modes, the PSS and PST streams are steered to the FHX, where gain setting and delay corrections are performed. Coarse and fine delay corrections are performed prior to VLBI beamforming, except for VLBI beamforming, which is carried out by four TALON ENGINES, both PSS and PST beamforming and post-processing in the LRUs with delay measurements provided by the PSS and PST beamforming instrumentation polarization corrections for continuum/spectral line mode and zoom mode imaging. For line mode and zoom mode imaging or pulsar phase binning mode or calibration, solutions for VLBI search, channelization for PSS and PST, and PST beamforming are packaged and sent via 100GE (Giga bit Ethernet) links to a TALON ENGINE, both PSS and PST beams are fed back to the PST Engine via two 100GE links. For all eight antennas handled by the SX LRUs, the two polarization components of the channelized data are transmitted through a single 100GE link to a TALON ENGINE. Each SX LRU handling 1/8 of the total bandwidth contains 1/32 of the SKA1-Mid.CBF. PST beams generated by the SKA1-Mid.CBF are up to 1500 with up to 2.5GHz bandwidth in Bands 3, or 8 PST beams in Bands 4 and 5. From XBF ENGINE, the cross-link with SX LRUs is used to control the team of telescopes, and these servers also apply delay corrections to PSS and PST data. In SKA1-Mid, these servers communicate with each other using two Ethernet links. All hard-wired links between the Mid.CBF through the F-ENGINE to 8 TALON-LRUs. TALON-X SRU, 8 TALON-LRUs, and 50 Sub-racks are required to perform the same processing. This is the first stage of the processing. For all observing modes, the PSS and PST streams are steered to the FHX, where gain setting and delay corrections are performed. Coarse and fine delay corrections are performed prior to VLBI beamforming, except for VLBI beamforming, which is carried out by four TALON ENGINES, both PSS and PST beamforming and post-processing in the LRUs with delay measurements provided by the PSS and PST beamforming instrumentation polarization corrections for continuum/spectral line mode and zoom mode imaging. For line mode and zoom mode imaging or pulsar phase binning mode or calibration, solutions for VLBI search, channelization for PSS and PST, and PST beamforming are packaged and sent via 100GE links to a TALON ENGINE, both PSS and PST beams are fed back to the PST Engine via two 100GE links. For all eight antennas handled by the SX LRUs, the two polarization components of the channelized data are transmitted through a single 100GE link to a TALON ENGINE. Each SX LRU handling 1/8 of the total bandwidth contains 1/32 of the SKA1-Mid.CBF. PST beams generated by the SKA1-Mid.CBF are up to 1500 with up to 2.5GHz bandwidth in Bands 3, or 8 PST beams in Bands 4 and 5. From XBF ENGINE, the cross-link with SX LRUs is used to control the team of telescopes, and these servers also apply delay corrections to PSS and PST data. In SKA1-Mid, these servers communicate with each other using two Ethernet links. All hard-wired links between the Mid.CBF through the F-ENGINE to 8 TALON-LRUs. TALON-X SRU, 8 TALON-LRUs, and 50 Sub-racks are required to perform the same processing.
3. TALON LRUs

Each of the TALON LRU supports several monitor and control subsystems. The TALON LRU contains 2 DDR4 DIMM modules, 4 100GE QSF P28 ports, and 11,721 multipliers. Each supporting a 64-bit wide transfer rate of 2400 MT/s.

The FPGA contains 2.8 million LEs, 11,520 18×19 bits multipliers and internal memory blocks. The SX280 FPGA has 2.8 million LEs, 11,520 18×19 bits multipliers and internal memory blocks. The SX280 FPGA contains 64 26G 12 bit wide transfer paths. Each port can be configured as a 100GE link or four 100GE link or 100GE link. Each DDR stack has memory bandwidth of up to 128 GB/s and 512 GB/s total memory capacity. The SX280 FPGA contains the High Bandwidth Memory (HBM) blocks with Density up to 128 GB/s.

The main difference between the FPGA and the MX210 FPGA is that the MX210 FPGA contains the High Bandwidth Memory (HBM) blocks whereas the SX LRU contains 4 26G 12 bit wide transfer paths. Each port can be configured as a 100GE link or four 100GE link or 100GE link. Each DDR stack has memory bandwidth of up to 128 GB/s and 512 GB/s total memory capacity. The SX280 FPGA contains the High Bandwidth Memory (HBM) blocks whereas the MX210 FPGA contains the High Bandwidth Memory (HBM) blocks.

Each TALON LRU contains 2 DDR4 DIMM modules, 4 100GE QSF P28 ports, 11,721 multipliers and internal memory blocks. The SX280 FPGA has 2.8 million LEs, 11,520 18×19 bits multipliers and internal memory blocks. The SX280 FPGA contains 64 26G 12 bit wide transfer paths. Each port can be configured as a 100GE link or four 100GE link or 100GE link. Each DDR stack has memory bandwidth of up to 128 GB/s and 512 GB/s total memory capacity. The SX280 FPGA contains the High Bandwidth Memory (HBM) blocks whereas the MX210 FPGA contains the High Bandwidth Memory (HBM) blocks.

These include JTAG and Intel M20k SERDES transceivers.
4. Summary and Future Work

The Canadian NRC and MDA collaboration has proposed the TALON architecture for the SKA1_Mid.CBF. This architecture features hardware, firmware, software and mechanical designs to meet the functional and non-functional requirements. The hardware design for the TALON architecture mainly consists of two LRUs; TALON-SX that contains a Stratix-10 SX2800 FPGA and TALON-MX that contains a Stratix-10 MX2100 FPGA with HBM memory blocks. In addition, each of these LRUs contain 2 DDR4 DIMM modules, 4 100GE QSFP28 ports and 48 26 Gbps bi-directional optical channels that connect to a custom optical-backplane. Up to 7 TMAC/s of processing capability, 512 GB/s of memory bandwidth and 1.648 Tb/s of I/O capacity can be facilitated by each LRU. The PCBs for the two LRUs are currently being designed at the DRAO. The engineering samples of Stratix-10 SX2800 FPGA are currently available from Intel. The first prototypes of the TALON-SX LRU are expected to be delivered by the middle of 2017.

5. Acknowledgements

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6. References