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Side-Lobe Reduction with a GaN Active Antenna Technique

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Abstract

This work aim at a low side-lobe GaN active antenna for microwave power transfer. In this study, a 5.8 GHz GaN amplifier with a harmonic-treatment circuit for high efficiency is designed and fabricated. The output power of this amplifier is controlled by the drain-bias-voltage levels which contribute the amplitude adjustment of array-antenna elements. The RF-output power and power-added efficiency (PAE) reduction of 2.81 dB and 3.63 point are confirmed at reducing the drain voltage to 35 V from 55 V. This amplitude difference reduces the side-lobe level of 9.45 dB at comparing the same amplitude and phase condition in a 1×4 circular-patch array-antenna simulation.

1 Introduction

Long-range microwave power-transfer (MPT) systems such as space solar power satellite (SSPS) require the high-power active array-antenna technologies. The compatibility of MPT with communication systems and the improvement of electro-magnetic interference (EMI) programs of MPT are important topics. The low side-lobe antenna approach are expected for one of the solution of these problems.

In the array-antenna operation, the suitable amplitude distribution for each element reduces the side-lobe level is known [1], [2]. In conventional study, the low side-lobe array antennas with a non-uniform power-divider network based on these techniques are reported [3], [4].

In this work, the low side-lobe antenna is realized by a GaN-based active array-antenna approach. The amplitude of each antenna elements are tuned by the drain-bias voltage of amplifier, which provide a reconfigurable characteristics for the side-lobe level. In this paper, the characteristics of designed and fabricated GaN amplifier is demonstrated and the calculated array-antenna patterns based on the amplifier output are reported.

2 Amplifier Design and Fabrication

A 5.8-GHz GaN amplifier as shown in Fig. 1 is designed by RF-circuit simulator (AWR, Microwave Office). This circuit is designed on Arlon AD1000 substrate ($\varepsilon_r = 10.2$, $\tan\delta = 0.0023$, and 0.8-mm thickness). In this amplifier design, the harmonics are treated for improving the efficiency.

Figure 2(a) and 2(b) show the photographs of top view of the fabricated amplifier and the mounted GaN HEMT chip (Sumitomo Electric, SG0601C). The GaN HEMT is operated with a 55-V to 35-V drain bias and −2.5-V gate bias conditions, which provide AB class.

The measured characteristics of output RF power and PAE at each drain-bias condition are illustrated in Fig. 3(a) and 3(b). According to Fig. 3, the measured maximum output power is 39.33 dBm (8.57 W) at 26.43-dBm input and 55-V drain-bias condition. In addition, the maximum PAE of 59.58 % is measured at 24.52-dBm input and 40-V drain-bias condition. Comparing results at 55-V and 35-V drain-bias conditions, 2.81-dB (1.91-times) maximum output-power difference is confirmed, which provide 3.63-points PAE difference and 14.30-degrees phase deference. This phase difference is measured by a high-power setup of PNA-X Network Analyzer (Keysight, N5242A).

3 Antenna Pattern Calculation

The 1×4 circular patch-array antenna as shonwn in Fig. 4 is designed by 3D-EM simulator (CST, Microwave Studio). This antenna is designed on Nippon Piller Packing NPC-F260A ($\varepsilon_r = 2.55$, $\tan\delta = 0.0018$, and 1.6-mm thickness).

The calculated antenna-radiation patterns are illustrated in Fig. 5. According to Fig. 5, the antenna gain to front distance and side-lobe level at same amplitude and phase input for each element are 13.39 dBi and 0.57 dBi, respectively. On this other hand, the front-distance gain and side-lobe level at providing 1.91-times amplitude and 14.30-degrees phase shift for ANT2 and ANT3 in Fig. 4 are 12.89 dBi and −8.97 dBi, respectively. Comparing to same amplitude and phase condition, the front-direction gain and side-lobe level of 0.50 dB and 9.54 dB are reduced. In this condition, the

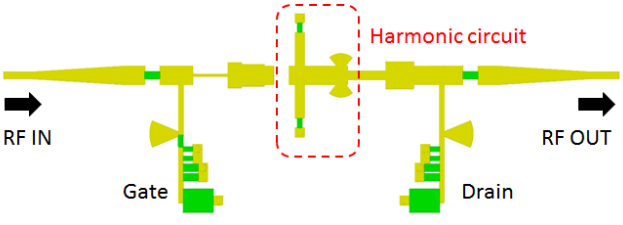
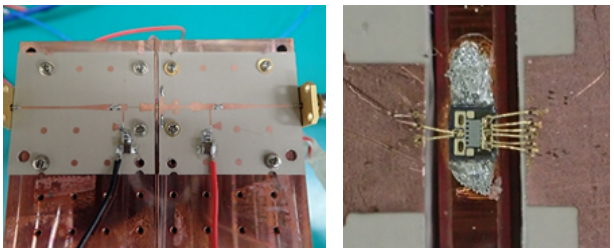


Figure 1. Designed amplifier layout.



(a) (b)

Figure 2. Fabricated amplifier: (a) top view of amplifier and (b) mounted GaN HEMT chip.

first null point is vanished, which is caused by the 14.30-degrees amplifier phase shift.

4 Conclusions

In this work, the low side-lobe antenna pattern is calculated, which is based on the fabricated GaN amplifier outputs. This 9.54 dB side-lobe level reduction is realized with low amplifier PAE reduction about 3.63 points. In future work, the number of antenna elements are increased and the feasibility of low side-lobe array antenna with a excitation distribution based on the GaN active-antenna approach is studied.

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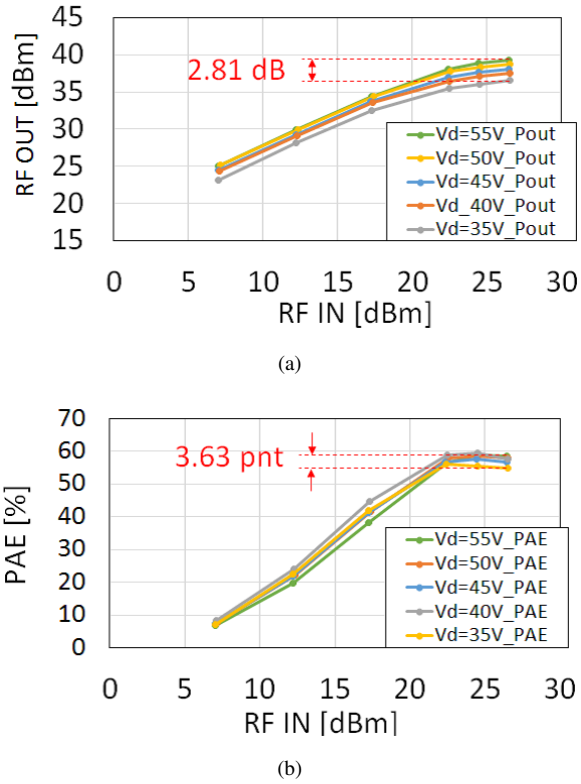

Figure 3. Measured amplifier characteristics: (a) RF out characteristics and (b) PAEs.

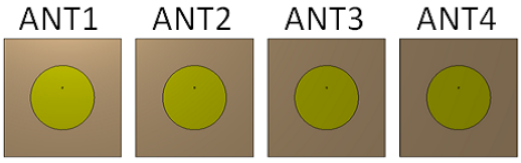

Figure 4. Designed 1×4 circular patch array antenna.

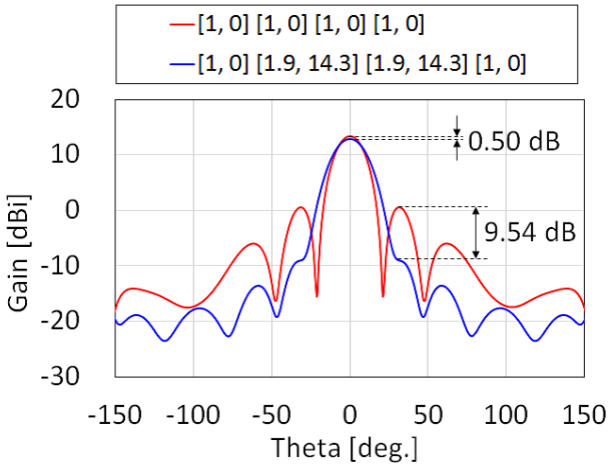

Figure 5. Calculated antenna radiation patterns.