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A Broadband High-Efficiency Doherty Power Amplifier with Continuous Inverse Class-F Design

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Abstract

This paper presents a broadband Doherty power amplifier (DPA) design with two continuous Class-F-1 matching circuit eliminating offset line in carrier way to increase the bandwidth and efficiency. By employing this compact and highly efficient design method, a DPA working at 2.0 GHz~2.6 GHz is designed and implemented for verification. With continuous wave (CW) measurements, the experimental results show the maximum output power of 43.8dBm and 75% drain efficiency for this DPA. At 6dB back-off power range, higher than 50% efficiency is presented over 500MHz. Moreover, 40 MHz long term evolution (LTE) modulated signals are applied for and digital pre-distortion (DPD) to evaluate its linearization performance. At an average output power around 34 dBm operated at 2.15 GHz and 2.55 GHz, lower than -50 dBc adjacent leak power ratio (ACLR) can be achieved.

1. Introduction

Broadband and highly efficient issues have always been the key points in PA designing. To the non-constant envelope signals in high-speed data transmission system, DPA is proposed as an effective solution to provide high efficiency at back-off power level corresponding to peak-to-average power ratio (PAPR) of the modulated signals. Many published researches focused on improving the efficiency of DPA at low output power level [1]-[6], but most of the DPAs are limited as narrow band operation and cannot be used in future broadband or multi-band communication systems.

To meet the requirement in broadband application, different DPA design strategies have been presented to mitigate the frequency limitation. In [4] and [7], it is shown that bandwidth of the DPA can be enhanced by overcoming the λ/4 impedance inverter and offset line problems. So this design proposes a frequency extension strategy which eliminating offset line in carrier way and replacing λ/4 impedance inverter with Chebyshev transformer. To achieve the broadband highly efficiency, harmonic-tuned operational principle of continuous Class-F-1 is both applied in two sub-amplifiers. For demonstration, a broadband DPA is implemented at 2.0~2.6GHz with maximum efficiency 75%~61% and 6dB back-off efficiency 64%~45%. Especially, efficiency higher than 50% is obtained over 500MHz frequency band.

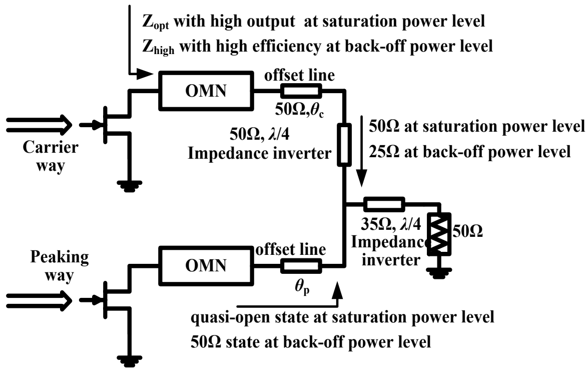


Figure 1 Modification of the SRFT for output matching procedure

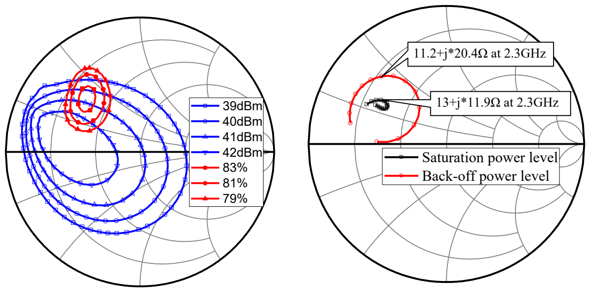
2. Broadband and Highly Efficient Design Method

2.1 Bandwidth improvement without offset line and impedance inverter

As shown in Figure 1, carrier amplifier in DPA is matched to optimum impedance (Zopt) at the saturation power level and high efficiency impedance(Zhigh) at back-off power level by output matching network (OMN), offset line and λ/4 impedance inverter. For the peaking amplifier, offset line is also inserted to provide quasi-open state at back-off power level. To enhancing the bandwidth, offset line and impedance inverter in DPA topology should be eliminated. It is to say the OMN of carrier amplifier had better to be capable of transforming 50Ω and 25Ω to Zopt and Zhigh simultaneously.

In this design, a PA device of CGH40010 is applied and the load-pull procedure is carried out to illustrate the output power and efficiency contours of this PA. As shown in Figure 2 (a), the load-pull result exports that the impedance presenting high efficiency at back-off power level will have an increased reactance component. So fundamental impedance varying around 9.6+j*10.6Ω is selected over 1.7GHz~2.8GHz for optimum value and impedance of 13.2+j*24.7Ω is selected to maintain a high efficiency at the back-off power level.

Using the SRFT design method in reference [2], the two-port network is constructed for saturation and back-off power level both. By applying this OMN circuit in the carrier amplifier, offset line and the λ/4 impedance inverter can be omitted.



(a) (b)

Figure 2 (a)The load-pull simulation results. (b)The simulated impedance of the OMN

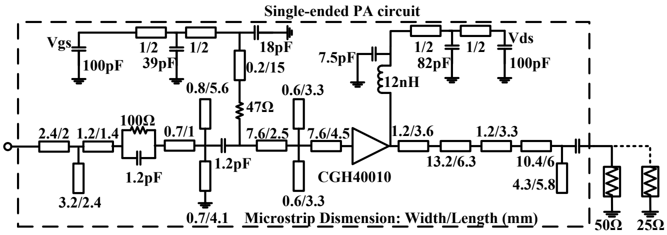


Figure 3 Single-ended continuous Class-F^{-1} PA as sub-amplifier in DPA

2.2 Modified SRFT and Continuous Class-F^{-1} Design

In order to obtain a highly efficient performance for the DPA, continuous Class-F-1 mode is utilized in the carrier and peaking amplifier operation. From the load-pull results, harmonic impedances of the PA device are chosen as -j*199Ω and -j*36Ω to support an open and short state at the second and third harmonic frequency. Combining with the modified SRFT procedure, stop-band frequency parameter sweeping is introduced in the above synthesis and harmonic impedances are examined at the corresponding harmonic frequencies [8].

After getting the OMN by SRFT, it needs to be connected with actual PA device model and optimized for a better performance at the two power levels transformation. The post-optimized schematic is shown as Figure 3. To verify this no offset line design strategy, simulation for the OMN of the carrier amplifier is implemented at saturation power level and back-off power level terminating with 50Ω and 25Ω terminals respectively. The simulated impedance trajectory is shown in Figure 2 (b) and well impedance transformation is produced by this OMN.

2.3 Chebyshev low-pass impedance transformer

In this DPA design, the 35Ω λ/4 impedance inverter is replaced with a short-step Chebyshev impedance transformer centered 2.5GHz with 40% fractional bandwidth and 2:1 transforming ratio. This transformer can transform the 50Ω terminal to 25Ω in a broad bandwidth without the frequency dispersion of λ/4 impedance inverter.

Then, the impedance transformer and two single-ended PAs, are assembled together to construct the DPA circuit.

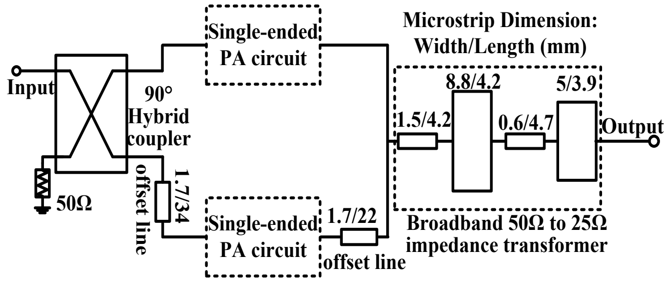


Figure 4 Schematic of the proposed broadband DPA

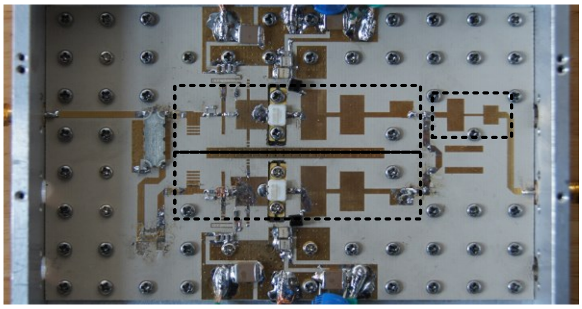


Figure 5 Photograph of the designed broadband DPA

Offset line is inserted in peaking way to make it present quasi-open state at the back-off power level. And another 50Ω transmission line is also used in front of the peaking amplifier to compensate the phase delay between two ways. Final topology of this proposed broadband DPA is illustrated in Figure 4.

3. Fabrication and experimental results

To verify this frequency extension design strategy with no offset line in carrier way, DPA with two CGH40010 devices is fabricated on the RF35 substrate with a dielectric constant of 3.5 and thickness of 30mil. The implemented DPA working at 2.0~2.6GHz is shown in Figure 5. Large-signal and modulated signals measurement are both applied to this DPA.

3.1 Large-signal measurements

For bias condition of the DPA, carrier amplifier is biased at -3.2V with quiescent current of 50mA and peaking amplifier is biased at -5.5V. Drain voltage are both 28V.

CW is utilized to measure efficiency and gain character of this DPA, which reaches a 28% fractional bandwidth over 2.0~2.6GHz. As shown in Figure 6, the maximum output power is obtained within 43.8~41.7dBm and efficiency varies from 61.4~75%. At 6dB back-off power level, the measured efficiency is higher than 50% at 2.0~2.5GHz and ranges from 45% to 64% over entire bandwidth. The gain character is within 10dB~15.6dB in the working band.

3.2 Modulated-signal measurement

The LTE signals are also excited to this broadband DPA to evaluate its modulated characteristic. 40HMz two-carrier LTE signal with 7.8dB PAPR is applied to this broadband DPA. Adopting DPD program to this DPA, well-linearized ACLR of the output signals which is lower

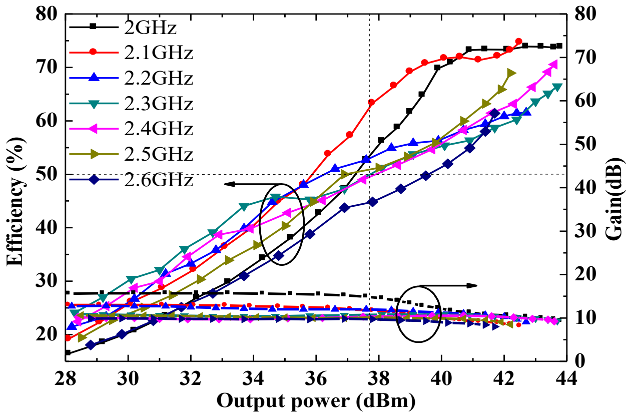


Figure 6 Measured drain efficiency and gain character over 2.0GHz~2.6GHz

TABLE I
LINEARIZATION PERFORMANCE OF THIS DPA WITH LTE SIGNAL

Paverage (dBm)	F(GHz)	ACLR Without DPD (dBc)	ACLR With DPD (dBc)	Eff (%)
34	2.15	-23.3/-25.0	-50/-51.1	49.0%
35	2.55	-25.3/-25.9	-51.9/-52.6	37.6%

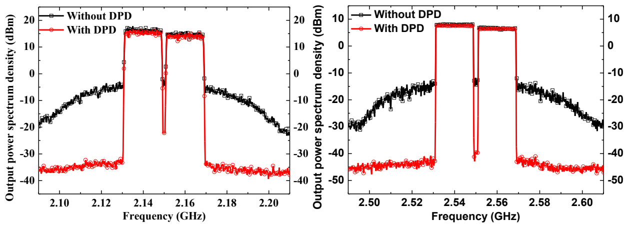


Figure 7 Measured output power spectrum density with and without DPD program at 2.15GHz and 2.55GHz

than -50dBc are obtained at 2.15GHz and 2.55GHz respectively. As illustrated in the Table I, the measured output power spectrum density around 34dBm and 35dBm with efficiency of 49.0% and 37.6% is obtained verifying its satisfaction for wireless communication application. The measurement is plotted in the Figure 7. For comparison, summary of some published broadband DPA is listed in Table II.

4. Conclusion

This paper presents a broadband DPA design which eliminates the λ/4 impedance inverters and offset line in the carrier way. High efficient continuous Class-F-1 mode is utilized for carrier and peaking amplifiers to enhance the efficiency of this broadband DPA. A highly efficient broadband DPA is designed and implemented over 2.0~2.6GHz reaching a 28% fractional bandwidth. Compared with other state-of-art broadband DPA performance, this proposed DPA presents the highest efficiency character of 61.4~75% and 45~64% at the saturation and back-off power level. 40MHz LTE signals with DPD are also applied at 2.15GHz and 2.55GHz to evaluate its linearity performance. After DPD linearization,

TABLE II
PERFORMANCE SUMMARY OF HARMONIC-CONTROLLED PA

Ref	F(GHz)	BW (%)	DE at Pmax (%)	DE at 6dB OBO (%)	P(dBm)	Gain (dB)
[1]	2.2~3.0	30.8	52~68	30~53	40~42	5.5~8.7
[3]	3.0~3.6	18.2	56~65	38~54	43~44	7.5~12.8
[4]	0.8~1.2	40	50.8~78.5	30.3~40.1	40.2~42.9	10.8~14.8
[6]	1.7~2.4	36.3	53~72	43~59	39~41*	10~11.2
This work	2.0~2.6	28	61.5~75	45~64	41.7~43.8	10~15.6

*Extracted from the Figure of reference.

ACLR of lower than -50dBc are achieved by this DPA. It predicts the satisfaction of this DPA in wireless communication system and also demonstrates this highly efficient broadband DPA design method.

5. Acknowledgements

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6. References

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