VSR5 Optical 4×10Gbps Converter IC and 12×10Gbps VCSEL Optical module Design

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Abstract

This paper demonstrates a 4×10Gbps VSR (Very Short Reach) converter IC in STM-256/OC-768 applications, which meets the requirements of OIF-SFI5-01.0 and VSR5-01.0 agreements. The converter performs 16×2.5Gbps ~ 4×10Gbps electronic signals transformation. All of the conversion functions are realized in an FPGA. In addition, a 12×10Gbps optical VCSEL driver is fabricated by 0.18μm CMOS technology and the VCSEL optical module is packaged.

Key words: VSR5, SFI5, Converter IC, Parallel Optical Link, FPGA, VCSEL

1. Introduction

In these years, the development of high-speed transmission systems has resulted in a strong demand for bandwidth between large scale integrations (LSIs) in high-performance computers and router systems[1]. Vertical-cavity surface-emitting laser (VCSEL) transceivers dominate the short-reach optical market, from serial Ethernet and Fiber-channel transceivers to parallel transceivers and active optical cables for high-performance computing and switch/routers[2]. This paper presents an unexpansive STM-256/OC-768 converter IC in VSR (very short reach) application. The VSR interface utilizes the 850nm short wave VCSEL-based parallel transmission technology.

2. Functional Overview

As shown in Fig.1, the block diagram of VSR5 is a bi-directional interface.

The SERDES-Framer Interface 5 (SFI-5) is an electrical interface between STM-256/OC-768 framer and serializer/deserializer interfaces. The 4×10Gbps parallel optical interface is an MTP/MPO connector with four-channel Multi Model Fiber (MMF) cable to transmit the STM256/OC-768 frame range up to three hundred meters. The converter takes part in 16×2.488 ~ 4×10Gbps data rate conversion. Therefore, a convergence of 40Gbps bandwidth is achieved using optical modules in duplex direction.

3. VSR5-1 Converter IC

The block diagram of the converter IC in the VSR5-1 four channel array configuration is illustrated in Fig. 2.

In the TX direction, the converter logic firstly receives 16×2.488Gbps and a deskew (TXDSC) data signal from an OC-768 pattern generator. The converter recovers clock and data from each SFI-5 channel, then demuxes the SFI-5 signals by 1:16 to deskew logic. The deskew logic eliminates skews between the 16 data lanes using information contained in the DSC channel. The STM-256 framer locates A1A2 delimiter in STM-256 data frames and performs basic word alignment. The framed 16-channel data is scrambled, then it is encoded by 64B/66B to reassemble the 4 channels of data into SFI-5 interface signal and re-maps the STM-256 framing bytes.

In the RX direction, the converter receives 4×10Gbps signals from the optical module. The deserializer performs equalization and clock and data recovery (CDR). Then the converter aligns individual channels by each channel frame delimiters to compensate for any inter-channel skew that may occur due to propagation delay between these channels. Finally, the converter decodes 64B/66B to reassemble the 4 channels of data to SFI-5 interface signal and re-maps the STM-256 framing bytes.
3.1 SFI-5 deskew

The function of the deskew logic is to recognize the framing and header bytes in the TXDSC channel, and to identify the start of the reference data that is replicated from each of TXDATA channel.

Where there is a match, the skews between TXDATA and TXDSC is found. According to SFI-5 agreements, 11 unit intervals (UI) of wander is allowed including mechanical and routing mismatches in 16 data lanes, as well as temperature and power changes and so on. The deskew logic runs at 155.52MHz, so it is suitable to be implemented in FPGA. Another approach is that the working speed is 312.5MHz and FIFO control logic is adopted [5-6]. Reference [7] uses a 7-bit shift register and a 64-bit compare window. Compared with the method, our approach consumes lower power supply and simplifies FIFO control logic. Therefore, a 1:16 demultiplexer is needed in every data lane. It receives 17 lanes (16 data and DSC) of 2.5Gbps data on 16 bit wide 155.52Mbps buses. Each lane’s data has arbitrary bit position within the 16-bit bus.

Firstly, the DSC_frame_sync logic aligns the TXDSC data at byte boundaries by delimiter A1A2 and generates a channel ID signal. Meanwhile, each incoming 16-bit TXDATA is combined with the lower 15 bits of the data word from the previous cycle, and fed into a 16-port MUX module. Then, the data enters a slide-window detector, which will generate a 4-bit signal that indicates each lane skew position from 0 to 15-bit. Finally, the selector and output MUX will select the deskewed data according to channel ID and skew position in each channel, so that the output data can be precisely aligned on the byte boundary.

Moreover, the SFI-5 deskew logic serves two purposes: 1) to transfer all 17 data lanes which have individual clocks to a common master clock derived from 155.520MHz clock generated by CDR and 2) to absorb any wander with respect to each other or to the common transmit clock. The deskew logic can compensate for 11 bits of static skew and 21 bits of dynamic wander/jitter, which meets OIF agreements.

3.2 OC-768 framer

OC-768 framer exams the A1A2 transition in the incoming data. Once the transition is found, the data words can be shifted in time corresponding to the byte boundaries of the incoming data. In this application, the 16×2.488Gbps deskewed SFI-5 data stream is 1:16 demuxed into frame alignment logic, which equals to demux the OC-768 data stream by 1:256 ratio. So, the A1A2 boundary will be arbitrary in any 1/256 position of the incoming data frame. Conventional framing approaches operate in serial or parallel manner to search frame synchronous code (FSC) A1A2 [7-10]. However, with the increment of data bus width, these strategies impose strict timing constraint on the related logic circuits, and in turn, lead to substantial increasing in the frame search logic design complexity.

If 768 A1 in an OC-768 data stream are divided into data groups by each 256 bit width, there are at least 23 same data segments (24 same data segments at most). So, the XOR result of current segment and the previous segment should be equal to zeros. Once the first A2 arrives, the XOR result of current segment and the previous segment will not be all zeros. The first 1 in the XOR result indicates the boundary of A1 and A2. While the first 1 after 23 consecutive non-zero segments appears, the dichotomy search logic could locate the position of the first 1, namely the boundary of A1 and A2. Take, for example, Fig. 3 demonstrates one position of disordered A12 (as …BDBD8A0A0A….). If 256 bits just before A12 transition and 256 bits of A12 transition are operated XORs, the first 1 in XOR results corresponds to the A12 boundary. Moreover, it is very important that there are no two consecutive zeros after the first 1 in XOR result.

The XOR results of current 256 bit data and the previous cycle will be fed into a dichotomy search module as shown in Fig. 5. Each two middle bits are “ORed” and 8 select signals will be generated in turn.

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Figure 3. An example of XOR result indicates A12 transition

Therefore, a dichotomy search algorithm logic will perform word alignment and OC-768 de-frame. Fig.4 demonstrates the OC-768 framer block diagram.

Figure 4. Dichotomy Search Module Block Diagram

The XOR results of current 256 bit data and the previous cycle will be fed into a dichotomy search module as shown in Fig. 5. Each two middle bits are “ORed” and 8 select signals will be generated in turn.

Figure 5. Dichotomy search module
According to the combination of 8 bits select signal, frame select logic chooses 384 bits combined with the current 256 bits and lower 128 bits of the data word from the previous cycle, as is revealed in Fig. 6. Compared with traditional framer logic, the complexity of the dichotomy frame alignment circuit is cut down from N stage to \( \log_2 N \) stage, where N is the demux ratio, which boosts up the circuit operating speed and lowers circuit complexity greatly.

4. Optical Module design

The drivers for VCSEL array must essentially be able to provide a fast modulation current into the laser diode, as well as a bias current. The 12-channel VCSEL driver array chip is implemented by SMIC 0.18\( \mu \)m CMOS technology. One channel common-cathode VCSEL driver circuit diagram is shown in Fig.7, which consists of pre-amplifier stage and output stage. The input stage consists of three-stage cascade circuit to pre-amplify input signal and expand the bandwidth. To speed up fall time in laser driver, \( C^3A \) (Capacitively Coupled Current Amplifier) structure is adopted in output stage. There are three control terminals: \( V_{mod} \) adjusting modulation current, \( V_{bias} \) controlling bias current and \( V_{IH} \) adjusting VCSEL current for test.

5. Test results

The VCSEL driver is fabricated by 0.18\( \mu \)m CMOS technology. The consumed power per channel of the VCSEL driver is about 120mW while delivering 5mA bias and 10mA modulation current. Tested with an Advantest D3186 pulse-pattern generator, and an Anritsu wide band oscilloscope. Eye diagrams produced by each of the 12 VCSEL drivers at a data rate at 10Gbps PRBS pattern with input amplitude of 500mVpp were recorded in Fig. 10.
equalization at RX in serial loopback mode. The error detector logic counts error bits and a bit error rate (BER) of lower than $1 \times 10^{-12}$ has been obtained.

**Figure.11** VSR5 4×10Gbps test platform

### 6. Conclusion

We have presented the design of a VSR5 4×10Gbps VSR converter IC compliant with OIF VSR5-01 agreements. It functions as a "gear box" to convert 16×2.5-4×10Gbps electric signal. A 12-VCSEL optical module is packaged with self-made 12×10Gbps VCSEL driver, which is fabricated in 0.18μm CMOS process. Test results show that the VCSEL optical module meets OIF agreements. Due to the short distances application, it is a less costly alternative than current OC-768 short reach solutions.

### 7. Acknowledgement

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### 8. References

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